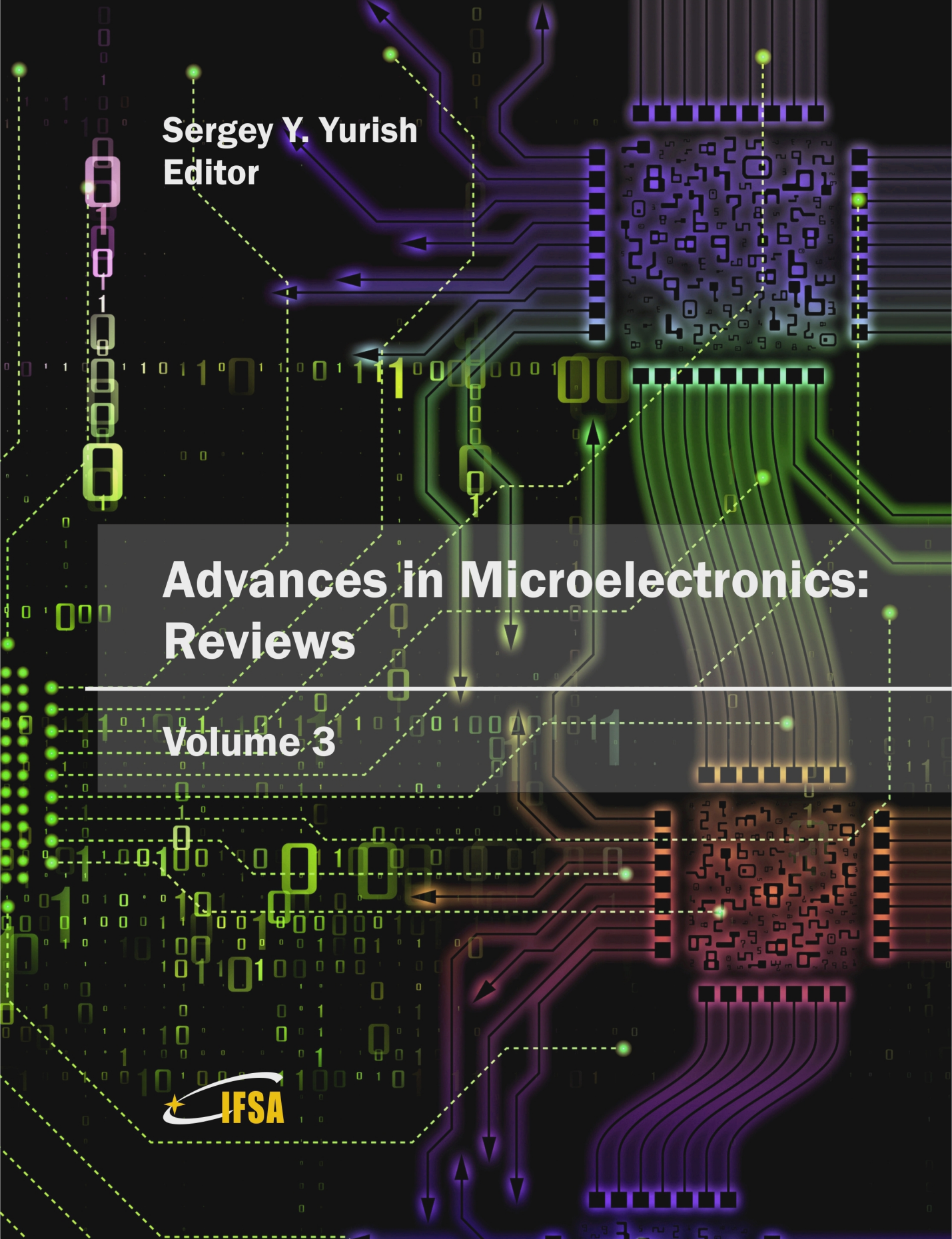
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Preface

The 3rd volume continues the popular open access Book Series on '*Advances in Microelectronics: Reviews*'. But as usually, it is not a simple set of reviews. Each chapter contains the extended state-of-the-art followed by new, unpublished before, obtained research results. The 1st and 2nd volumes from this Book Series have been published in 2017 and 2019 years accordingly.

Written by 40 contributors from academy and industry from 9 countries (Austria, China, Japan, Mexico, Russia, Slovak Republic, Spain, Thailand and Ukraine) the book contains 10 chapters from different areas of microelectronics: MEMS, semiconductors and various microelectronic devices.

Chapter 1 is devoted to organic electronics materials, devices, and applications. First, the charge transport phenomenon in organic materials is explained, and methods for charge transport evaluation are briefly described. Afterwards, organic electronic devices such as organic field-effect transistors, organic light-emitting devices, and organic solar cells are introduced and explained.

Chapter 2 describes one alternative to mitigate the electronic waste issue next years, where reconfigurable conduction mode in semiconductor devices is suggested to demonstrate how emergent functional devices might be driven by using scalable circuit technologies encouraged on recyclability actions into the electronics´ industry.

Chapter 3 presents a comprehensive approach to modeling and simulation of degradation phenomena affecting the reliability of modern nano-scaled interconnects. The dependence of interconnect lifetimes on length, thickness, and the diffusivities of the cap layers obtained by simulation are discussed in relation to experimental results.

Chapter 4 discuss the analytical models of process induced random variation of FGMOSFET. In the technological aspect, some of these models are dedicated to the above 100 nm FGMOSFET where the others are oriented to the nanometer FGMOSFET. Mathematically, some of them are statistical models where the rests are probabilistic ones.

Chapter 5 describes the Effective Young's modulus of electrodeposited gold for design of movable components in MEMS devices. The evaluation is conducted by a non-destructive resonance frequency method. Specimens used in the evaluation are pure gold micro-cantilevers prepared by electrodeposition and lithography. An increase in the effective Young's modulus is observed as the width of the micro-cantilever varied from 10 to 25 micrometer.

Chapter 6 is devoted to electrophotonic seamless circuits. This includes their basic components, namely the light source, the waveguide and the photodetector, all in silicon. Especial emphasis is placed on a novel integrable silicon photosensor, presenting the

physics and mathematics involved in it. Computational simulations corroborating the developed model are presented.

Chapter 7 describes different technologies for fabrication of nanodevices with aluminium superconducting tunnel junctions. The main building block of our devices is superconductor-insulator-normal metal-insulator-superconductor (SINIS) structure - one of the promising types of subTHz detectors. The progresses in theoretical modeling, experimental studies, and fabrication technologies is presented. Such technologies were also used for fabrication of aluminium SIS junctions and SQUID amplifiers.

Chapter 8 discusses a fully integrated differential impulse radio transmitter for ultra-wideband (UWB) applications. The fifth-derivative Gaussian pulse generator is implemented using a 0.18-μm CMOS process with low power consumption and low circuit complexity.

Chapter 9 describes the revealed ferromagnetic properties in diluted magnetic semiconductors which were Co-, Mn- and Fe-doped ZnO layers prepared by printing. The magnetization was found to be maximal in ZnO:Fe_3+ layers, about two times higher than in ZnO layers doped with Co_2+, Mn_2+ and Fe_2+ ions. On the basis of comprehensive studies of layers by various methods, the physical nature of the most important properties of the layers was established.

Chapter 10 contains the review of the Time-to-Digital Converters (TDC) state-of-the-art technology. The aim of the chapter is to help readers understand the principle and development trend of TDC. The concepts and investigations presented in this book chapter mainly originate from research results of peers all over the world.

I shall gratefully receive any notices, comments and suggestions from readers to make the next volume of '*Advances in Microelectronics: Reviews*' interesting and useful.

Dr. Sergey Y. Yurish
Editor

IFSA Publishing *Barcelona, Spain*

Chapter 1
Organic Electronic Materials and Devices

Michal Micjan and Martin Weis

1.1. Introduction

Human society made great progress in the last century because of science and technology. Various fields of technology improved the quality of human life, and one of the key roles had the dawn of electronics. As a leading representative of semiconducting materials, silicon is the inherent part of all electronic devices today and represents state-of-the-art electronics.

On the other hand, material science and research in the field of electronics are focused on alternative materials such as organic semiconductors. An organic semiconductor is a broad family of organic molecular materials that exhibit specific properties similar to inorganic semiconductors. Interestingly, molecular materials show only weak forces between the molecules, giving new deposition methods. The low-temperature evaporation in a vacuum is applicable for various small molecules, whereas "wet technologies" using organic material solubility in solvents are popular for large molecules and polymers. The thin-film fabrication technology is not a unique property of these materials; organic semiconductors exhibit semiconducting properties even without any doping, and the doping process only suppresses semiconducting properties. Hence, the organic semiconductors do not represent only alternative semiconducting materials, but it is also an exciting challenge for electronics and device physics.

The very first success in the field of organic electronics was metal-insulator-semiconductor (MIS) diode using polyacetylene and polysiloxane as organic semiconductor and insulator, respectively [1]. This pioneering work in 1983 demonstrated the possibility of organic material application in electronics. Three years later, researchers Tsumura, Koezuka and Ando from Mitsubishi Chemical company published fabrication of organic field-effect transistor (OFET) based on polythiophene as organic semiconductor [2]. However, the effective mobility of free charge carriers reached a level of only 10^{-5} $cm^2/V.s$, it was an exceptional success that opened a new field and inspired

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many research labs. The report on the first organic solar cell had been published by Tang in 1986 [3], and one year later, the first organic light-emitting diode (OLED) had been reported by Tang a Van Slyke [4]. It is interesting to note that Eastman Kodak's private company has fabricated both the first organic solar cells and OLED devices. These excellent achievements stand for the beginning of the new age in electronics, applying organic materials for electronic devices. In contrast to inorganic semiconducting materials, organic molecular materials have many variabilities in structure, an almost unlimited number of derivatives can be synthesised. Hence, after first success with well-known organic materials, organic chemistry and material science focused on designing novel materials with improved electrical properties. The first devices used insoluble polymers cross-linked directly on the substrate; however, the "holy grail" of the industry was soluble semiconducting materials [5] that can be deposited using printing technologies such as inkjet printer or various roll-to-roll depositions. Since the solution-based technologies may strongly reduce the fabrication costs, the low-cost deposition was a driving force for the applied research. Although organic semiconductors have been envisioned as potential candidates for future electronics, many research labs had doubts about the market's impact, and the research progress was only very slow. Therefore, we can state that the next milestone was Gilles Horowitz's work [6], which used the common approach used in the field of semiconductor physics to explain OFETs. It must be emphasised that this work did not use any new concept, and certain parts are even incorrect since they are based on the assumptions on material doping. Nevertheless, this work inspired many researchers to extend their study on organic materials and also, the private companies made large investments in the applied research. Furthermore, in the '70s has been established the second important class of organic materials, conjugated polymers, also denoted as synthetic metals. The successful synthesis and controlled doping of conjugated polymers by Alan G. MacDiarmid, Alan J. Heeger, and Hideki Shirakawa were honoured with the Nobel Prize in Chemistry in the year 2000.

During the next two decades, the research papers demonstrated novel organic materials' capabilities, suggested new device designs and deposition technologies. As a result, organic electronics have been established as a new interdisciplinary field comprising material science, organic chemistry, physics, and electronics. The fundamental research was a strong basis for applications. OLED devices have been fabricated in the matrix; thus, the OLED displays were introduced as a competitor of liquid crystals displays (LCD). The OSC already reached an efficiency better than 13% [7], which is more than comparable with amorphous silicon or polycrystalline silicon solar cells. The new field already had certain success on the market. OLED displays are used not only for television sets but also for mobile devices because of low power consumption and great performance. Also, the OLED lighting recently found its opportunity on the market and start to have commercial success.

The broad range of organic electronics applications encourages researchers for novel approaches in material design, characterisation methods, or fabrication technology. Organic electronics technology promises low-cost devices and other advantages such as transparency, flexibility, etc. Hence, we can expect that application will hit the market mostly in the following areas:

- OLED displays and lighting: OLED displays already reached higher quality and lower price than LCDs. Cheap and energy-efficient OLED lighting with a very natural spectrum is a plausible alternative to inorganic LED lighting. In addition, the flexibility offers mechanical resistance;
- Photovoltaics: low-cost materials are already now the suitable replacement of inorganic solar cells used for daily applications;
- Memories and logic circuits: low-cost fabrication and flexibility are key points for smart packaging (especially RFID tags) and the internet of things (IoT) devices;
- Medical electronics and sensors: the growing interest in monitoring an individual's health state has raised a need for flexible sensors, wearable electronics, and smart systems that organic electronics devices can provide.

Although all envisioned ideas make organic electronics a promising candidate for future electronic devices, complex circuits based on organic transistors are still under development and did not reach the level required by industry. The research progress based on material science is similar to OLED or organic solar cell devices; however, a deep understanding of charge transport phenomena is needed to achieve greater electrical properties. It has been found that the semiconducting properties have a different microscopic origin than the inorganic materials, even though the macroscopic behaviour is sometimes almost identical. Interestingly, in contrast with his previous ideas, also Gilles Horowitz comments that "organic semiconductors" can be a misleading term and suggests calling these materials "organic semi-insulators", but it is too late for such a correction [8]. Organic semiconductors belong to the broad family of dielectric materials, and their properties range from insulating up to semiconducting.

This book chapter makes a brief introduction to organic electronics materials and devices. First, the charge transport phenomenon in organic materials is explained, and methods for charge transport evaluation are briefly described. Afterwards, the organic electronic devices are introduced and explained: (i) Organic field-effect transistors; (ii) Organic light-emitting devices, and (iii) Organic solar cells.

1.2. Charge Transport Phenomenon in Organic Semiconductors

Organic semiconductors are carbon-based materials that exhibit specific electronic properties of their inorganic counterparts; however, there is a huge discrepancy between them in the structure that rules the charge transport's undelaying physics. The inorganic semiconductors are consist of specific atoms ordered in atomic crystal with mutual covalent bonds. In the case of organic semiconductors, the atoms are covalently bonded only inside of the molecule, whereas the molecules have van der Waals intermolecular bonding, and they are ordered in molecular crystal. As a result, the more significant separation between the molecules does not provide the mechanical flexibility, solubility in organic solvents; however, it also leads to the weaker delocalisation of electron wavefunction that affects the charge transport. Furthermore, in the case of organic

materials, we always meet significantly lower order. The small molecules are primarily polycrystalline, and long-chain polymer materials have mostly amorphous structure.

The molecular structure of organic semiconductors with a small number of atoms leads to the unique energy band structure in contrast with "infinite" crystalline solids. While the electrons of a single atom are allowed to occupy several well-defined energy levels, the interaction of multiple atoms leads to the energy level splitting to avoid degenerated (multi-state) level. Solid-state physics teaches us that infinite crystals are the cause of the fine structure denoted as an energy band, as illustrated in Fig. 1.1. In inorganic semiconductors, the highest-filled energy band called the valence band, and the lowest unoccupied energy band is marked as the conduction band. The upper edge of the valence band and the lower edge of the conduction band are separated by the energy gap where no states are allowed. The limited number of atoms in a single molecule leads to separated energy levels, where each atomic orbital splits into several discrete molecular orbitals. Similar to the infinite crystals, we define the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) energy levels, Fig. 1.1. Again, the HOMO and LUMO energy levels are separated by the energy gap of forbidden states.

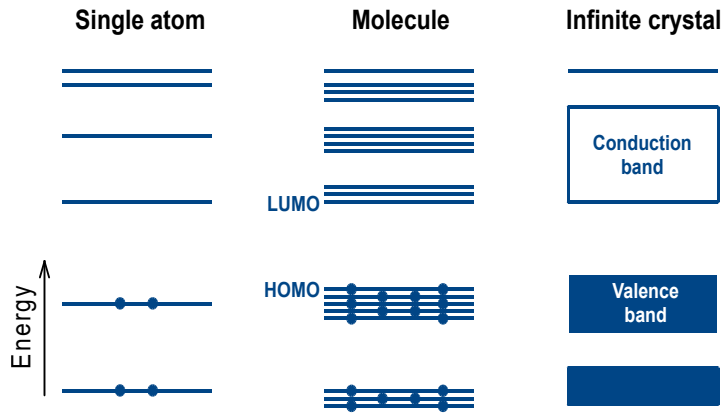


Fig. 1.1. Simplified energy band structure of a single atom, the molecule, and the infinite crystal.

Even though the isolated single molecule has a well-defined energy level structure, the mutual interaction between molecules cannot be neglected in molecular solids. Due to lack of order, the molecular solids are polycrystalline or even amorphous. The disorder induces the broadening of the energy levels [9-11], and the density of states (DoS) can be often approximated by a Gaussian distribution, see Fig. 1.2.

The degree of order in molecular solids rules the charge carrier transport mechanism in organic semiconductors. Hence, we can distinguish the most common levels of order as follows: (i) crystalline, (ii) crystalline with defects (*e.g.* polycrystalline), and (iii) amorphous. The crystalline molecular solids show the band-like transport [12-14]. Already a minor disorder causes the distribution of states, see Fig. 1.3, which creates shallow states close to the HOMO (or LUMO) level.

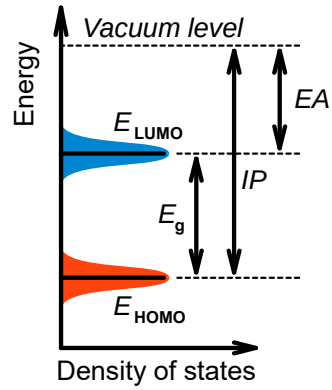


Fig. 1.2. The energy levels in organic semiconductor solids. Energy levels HOMO and LUMO are broadened due to intermolecular interaction. The ionisation potential (IP) is the energy required to remove one electron from the HOMO level, while the electron affinity (EA) stands for the energy of adding one electron from the vacuum level to the LUMO level.

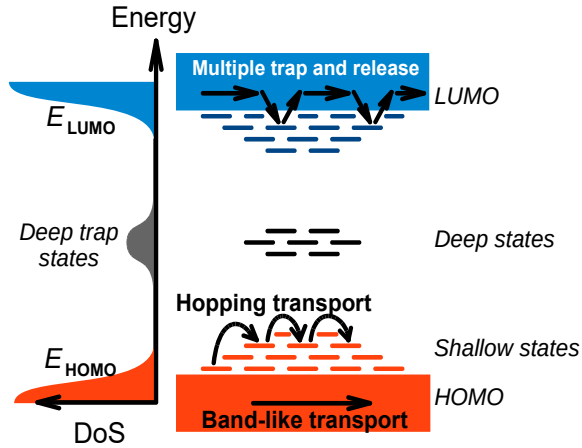


Fig. 1.3. The density of states and schematic spatial and energy diagram of organic semiconductor with trap states in the energy gap.

Consequently, the charge trapping takes place, and multiple trap-and-release model can describe the charge transport [15-17]. In the highly disordered molecular systems, the charge transport happens due to the hopping between localised states [18-21].

Let's have a deeper insight into the charge transport mechanisms. Ideal crystals have always been envisioned as the most critical requirement for scattering-free charge transport. Interestingly, already in the '80s, researchers succeed in the growth of single crystals of naphthalene and perylene [22-24]. The electron and hole mobilities obtained by the time-of-flight method reached a level as high as 400 $cm^2/V.s$ in the low-temperature region where the scattering due to thermal lattice vibration is suppressed, Fig. 1.4.

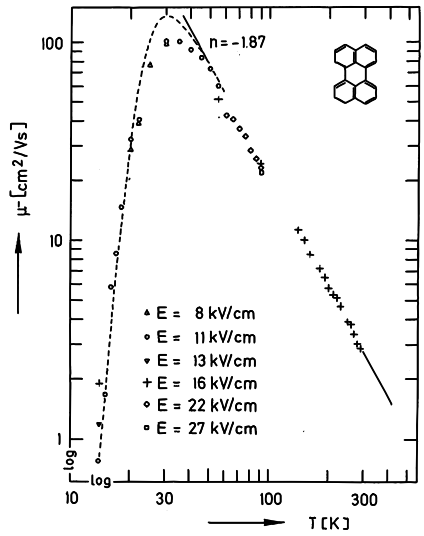


Fig. 1.4. Increase of the electron mobility in high purity single-crystalline α-perylene. In the log μ vs. log T, plot straight lines indicate an inverse power law temperature dependence, $\mu \propto T^{-n}$, indicative of band transport with acoustic phonon scattering. At the lowest temperatures, multiple shallow trapping limited transport is dominant. Reprinted with permission from N. Karl, K.-H. Kraft, J. Marktanner, M. Münch, F. Schatz, R. Stehle, H.-M. Uhde, Journal of Vacuum Science and Technology A, Vol. 17, 1999, 2318. Copyright 1999, American Vacuum Society.

Such great value cannot be obtained in the presence of charge trapping or hopping transport. Note that the increase in carrier mobility with decreasing temperature follows power-law temperature dependence, $\mu \propto T^{-n}$, with the power of about 3/2, indicating the band transport with acoustic phonon scattering. Hence, single-crystal devices have been used to demonstrate the occurrence of band-like transport properties.

Before we start with the explanation of charge traps we need to move onto the DoS description. In an ideal crystal, the DoS at the band edge has delocalised (extended) states with a shape of a lying parabola, DoS$\propto E^{1/2}$, where E is the energy of the electronic state. Hence, the band edge is well defined and sharp. In the case of disordered semiconductors, the band edges cannot be precisely estimated. The band-tail states follow the Gaussian distribution or exponential distribution as depicted in Fig. 1.5.

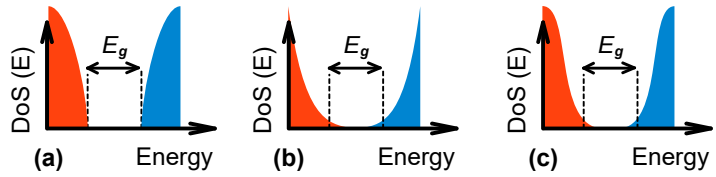


Fig. 1.5. The density of states distribution energy of (a) ideal crystal semiconductor, or polycrystalline/amorphous organic semiconductor assuming, (b) exponential or (c) Gaussian distribution for band tail states.

The Gaussian disorder model has been introduced by Bässler [26] for organic materials as follows

$$DoS(E) = N_0(2\pi\sigma^2)^{-1/2}\exp\left(-\frac{(E-E_{\text{HOMO}})^2}{2\sigma^2}\right), \quad (1.1)$$

where N_0 is the number of states per uni volume, and σ stands for energy disorder, implying that all states are localised. On the other hand, Vissenberg and Matters [27] proposed exponential shape of DoS

$$DoS(E) = \frac{N_0}{\mathrm{k}T_0}\exp\left(-\frac{E-E_{\text{HOMO}}}{\mathrm{k}T_0}\right), \quad (1.2)$$

where k is the Boltzmann constant and T_0 is the temperature parameter indicating the width of the exponential distribution. Even though there are many experimental results, there is no widely accepted model due to deviation from both approximations. Depending on the material, a single Gaussian, an exponential, or a combination of both functions is used [28-30].

It should be noted that the band tail electronic states localised within the bandgap serve as charge trapping states. In other words, trap states may have discrete levels and quasi-continuous energy distribution. As a result, the Gaussian or exponential band tails represent shallow trap states of an organic semiconductor. Trap states stand for the energetically favourable localised states; hence, the charge carrier detrapping time (reciprocal value of the attempt-to-escape frequency) can be even in the range of seconds. As a result, the effective value of the free charge carriers is drastically reduced. In the case of multiple shallow trapping with multiple thermal releases, the transport can be described by introducing a reduced average "effective mobility" μ_{eff}. Since this parameter includes reduced carrier density, it is a thermally activated material property.

Till now, we discussed the charge transport in single-crystal or polycrystalline organic semiconductors; however, amorphous organic semiconductors are a wide family of polymer-based materials that can be assumed as strongly disordered systems. Charge transport in such disordered organic semiconductors is carried out as hopping within a positionally random and energetically disordered system of localised states [30-32]. Even though the very pioneer work on hopping transport in organic solids was done by Bässler [26], the hopping transport in disordered semiconductors has been introduced by Mott in 1968 [33]. The variable range hopping transport has specific temperature dependence of the conductivity

$$\sigma(T) = \sigma_0\exp\left(-\left(\frac{T_0}{T}\right)^{\alpha}\right), \quad (1.3)$$

where T_0 is the characteristic temperature representing the effective energy barrier to hopping of charge carriers between localised states. The power exponent α is equal to $1/(1+D)$, where D is the system's dimensionality. In other words, the power coefficient α equal to 1/2 stands for 1D charge transport, while α of 1/4 represents the charge hopping in all three dimensions [34-36].

The charge transport in organic semiconductors directly affects the electrical conductivity, the charge carrier concentration and mobility. Since there is no direct method to evaluate the mobility, it is assumed the effective mobility, which also includes the deviation of ideal carrier concentration. A number of methods have been proposed to estimate the effective value of mobility, such as:

- Time-of-flight (ToF) method;
- The space-charge-limited-current (SCLC) method;
- Charge carrier extraction by linearly increasing voltage (CELIV);
- The impedance spectroscopy method;
- The organic field-effect transistor (OFET) method.

Each approach has its own limitation, required approximations, and measurement conditions; hence, effective mobilities' obtained values are not fully comparable.

The time-of-flight (ToF) technique introduced by Kepler [37] uses a dielectric layer sandwiched between two electrodes where one of them is semi-transparent. If we use a short laser pulse to generate a charge carrier sheet near one electrode, the charge sheet will drift towards the other electrode due to the applied electric field. The transient current corresponds to the temporal change of the charge on the electrode generated by the approaching charge carrier sheet. As a result, the current starts to decay at the transit time t_{tr}, when the charge carrier sheet arrives at the electrode, Fig. 1.6. Hence, the mobility μ can be evaluated as

$$\mu = \frac{d^2}{V}\frac{1}{t_{\mathrm{tr}}}, \tag{1.4}$$

where d is the dielectric film thickness, and V is the applied voltage. The film thickness is usually required to be more than 1 μm to record the transit time. Note that a similar approach has also been used with electronic pulse applied on the OFET device [38-40], and it is often denoted as electronic time-of-flight (e-ToF).

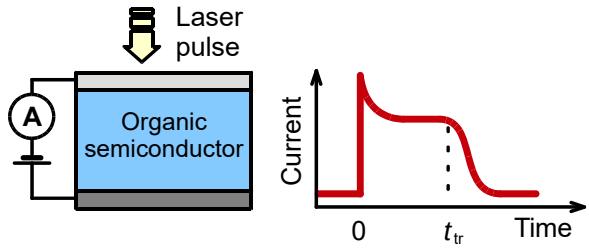


Fig. 1.6. The time-of-flight setup and the ideal current measurement for non-dispersive transport.

The space-charge limited current (SCLC) technique also uses the sandwich structure to extract the mobility from the steady-state current measurements [41]. If we assume a

single-carrier device (i.e. charge transport of only electron or only holes) with Ohmic contacts, the electric current density J follows the Mott-Gurney law

$$J = \frac{9}{8}\varepsilon\mu\frac{V^2}{d^3}, \tag{1.5}$$

where ε is the dielectric constant of the dielectric layer. Even though the SCLC technique has been widely used for organic diodes, the mobility analysis is strongly influenced by the presence of traps [42, 43]. In details, in the low-voltage region, the current response is ohmic, $J \propto V$, whereas the higher voltage causes accumulation of the charge carriers in the dielectric film, and the further current injection is prohibited due to electric field compensation of the space-charge in the device. There the current follows the square of the voltage, where $J \propto V^2$; however, mobility is still affected by the trapping. Once the voltage rises over trap-filled-limit voltage, the current abruptly rises, $J \propto V^n$ where $n = 2$, all the traps states are filled, the charge carriers flow through the device like in the trap-free material, and again the SCLC conditions are satisfied, $J \propto V^2$. Note that the log-log scale of current-voltage dependences is widely applied since the power dependences are linear, and the power exponent represents the slope of the current as depicted in Fig. 1.7.

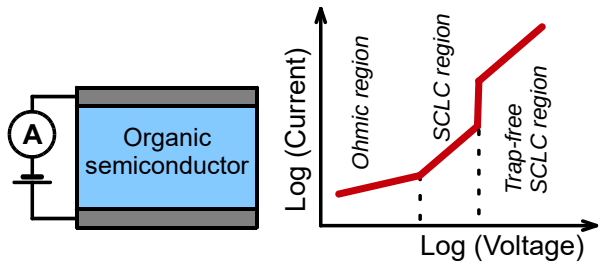


Fig. 1.7. The SCLC setup and the current-voltage dependence in log-log scale.

The charge carrier extraction by linearly increasing voltage (CELIV) is another technique applied for dielectric films sandwiched between electrodes. The main idea of CELIV is the extraction of the charge carriers present in the dielectric film by the applied external voltage. When the ramp voltage is applied with a slope of $\beta = V/t_{\mathrm{pulse}}$, the recorded current consists of the displacement current, $J_0 = \varepsilon_0\varepsilon_{\mathrm{r}}\beta/d$, and the current due to extraction of the dominant charge carrier present in the device, ΔJ [44-46], see Fig. 1.8. The mobility can be evaluated using numerically estimated correction factors as

$$\mu = \frac{2d^2}{3At_{\mathrm{max}}^2(1+0.36\Delta J/J_0)}, \tag{1.6}$$

where t_{max} corresponds to the time of maxima current density, see Fig. 1.8. The main limitation of the CELIV technique is that there is no possibility of distinguishing holes and electrons in ambipolar systems such as OLEDs or organic solar cells. It is also required a sufficiently high concentration of free charge carriers in the organic

semiconductor. In the case of low carrier concentration, continuous or a short light pulse illumination can be applied to photo-generate carriers, the so-called photo-CELIV technique.

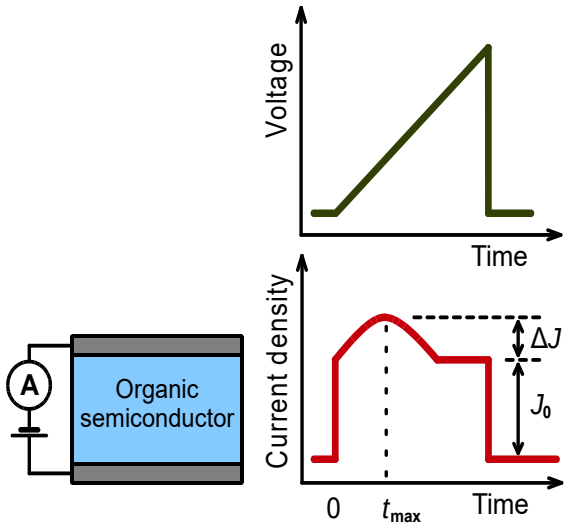


Fig. 1.8. The CELIV setup and the temporal dependence of the voltage ramp and recorded current density.

The impedance spectroscopy (or admittance spectroscopy) has also been proposed to evaluate organic electronics devices' charge transport properties. In details, the small-signal V_{ac} is superposed on the voltage offset V_{dc} to probe the frequency-dependent response. The determination of mobility using impedance spectroscopy is based on a single-carrier injection SCLC model [47, 48]. At high frequencies where the oscillation period probe signal is shorter than the transit time, the carriers injected by the probe signal cannot reach the steady-state space-charge distribution, which results in the observation of geometrical capacitance. Note that the mobility can be evaluated using the transit time in SCLC conditions [49] as follows

$$\mu = \frac{4}{3}\frac{d^2}{V_{\mathrm{dc}}}\frac{1}{t_{\mathrm{tr}}}, \tag{1.7}$$

The transit time can be clearly estimated from maxima of the negative differential susceptance $-\Delta B$, since it is related to the frequency as

$$t_{\mathrm{tr}} = 0.72\frac{1}{f_{\mathrm{max}}}, \tag{1.8}$$

as it is shown in Fig. 1.9. A similar approach has also been applied to OLEDs [50], organic solar cells [51], and OFETs [52].

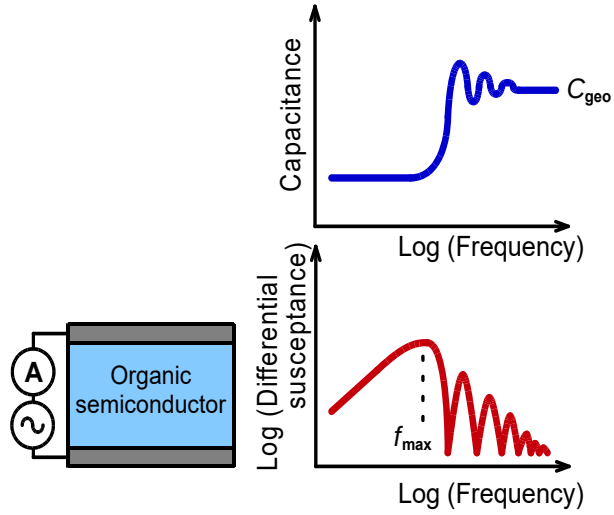


Fig. 1.9. The impedance spectroscopy setup and the frequency dependence of the capacitance and negative differential susceptance $-\Delta B$.

The organic field-effect transistor (OFET) mobility is a very important parameter since the charge transport in the OFET device occurs at the organic semiconductor/gate insulator interface. Since the high density of accumulated charge carriers and high electric fields make outstanding interface transport, the mobility is often denoted as the "field-effect mobility". The charge accumulation and transport across the channel region can be modelled in the saturated region using gradual channel approximation [53-55]; hence, the drain-source current I_{ds} is a linearly dependent on the gate-source voltage V_{gs} and follows relation

$$I_{\mathrm{ds}} = C_{\mathrm{g}}\mu\frac{W}{2L}\left(V_{\mathrm{gs}} - V_{\mathrm{th}}\right)^2, \tag{1.9}$$

where C_{g} is the capacitance per unit of area, V_{th} is the threshold voltage, W and L are channel width and channel length, respectively. As a result, the field-effect mobility can be estimated from a slope as

$$\mu = \frac{2L}{WC_{\mathrm{g}}}\left(\frac{\partial I_{\mathrm{ds}}^{1/2}}{\partial V_{\mathrm{gs}}}\right)^2, \tag{1.10}$$

as depicted in Fig. 1.10. Considering straightforward evaluation of the field-effect mobility, the OFET technique is used as a benchmark for a mobility evaluation. It should be mentioned here that the field-effect mobility estimation is burdened with error originating in the imperfect ohmic contacts, short-channel effect, or electric-field dependence (the Poole-Frenkel effect).

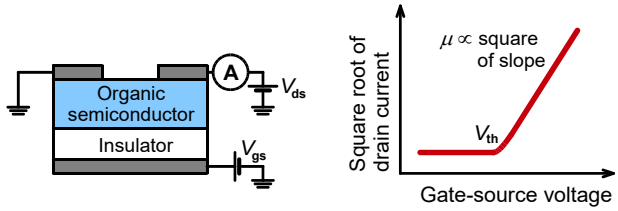


Fig. 1.10. The OFET setup and output characteristic used for the field-effect mobility evaluation.

1.3. Organic Field-Effect Transistor (OFET)

1.3.1. History of OFET

The first transistor was discovered in 1947 in Bell Laboratories in the USA. For the discovery of the transistor, its inventors received the 1956 Nobel Prize in Physics. The original idea behind the creation of a field-effect transistor (FET) originated in the mid-1920s. The first concept of the metal-oxide-semiconductor field-effect-transistors (MOSFET) was demonstrated finally in 1960 [56]. Later in 1977, scientists MacDiarmid, Heeger and Shirakawa published the electrical conductivity of the polymer polyacetylene (PA), and in 2000 gained the Nobel Prize in Chemistry [57]. The last milestone on the way to the first organic transistor was 1986 when scientists Tsumura, Koezuka and Ando succeeded in developing the first field-effect transistor using polythiophene as a semiconductor layer [2]. The transistor structure of the first organic field-effect transistor (OFET) as well as its output and transfer characteristics, are shown in Fig. 1.11.

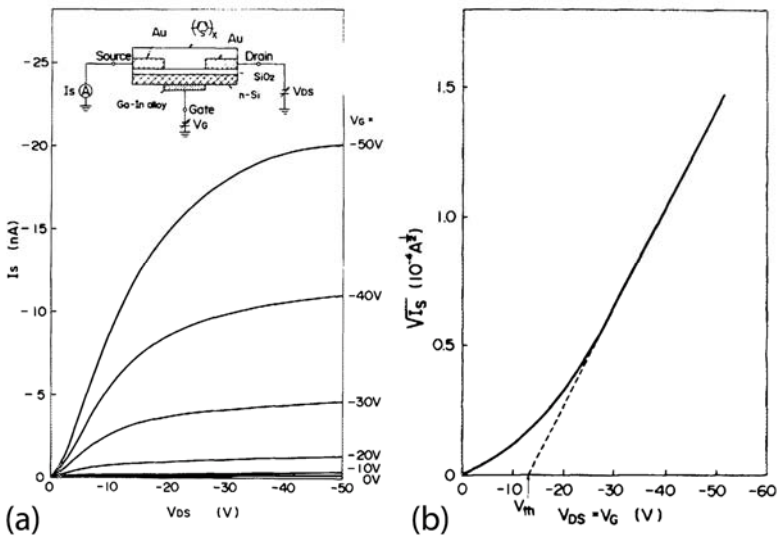


Fig. 1.11. (a) Output and transfer characteristics of the first OFET using polythiophene as a semiconductor layer. Reprinted from A. Tsumura, H. Koezuka, and T. Ando, *Applied Physics Letters*, Vol. 49, 1986, 1210, with the permission of AIP Publishing.

Even though the first OFET device was discovered in 1986 [2], there was an abrupt and rapid evolution of OFET devices and related materials. Fig. 1.12 illustrates the timeline of the research progress. In 80's has been introduced well-known materials such as poly(3-hexylthiophene-2,5-diyl) (P3HT) and sexithiopene (6T) [58, 59]. Very first devices were very uncomplicated and utilized an inorganic gate insulator layer. The first polymer gate insulator was proposed in 1990 and applied CYEPL, PVA, PVC, PMMA, PSt polymers [60]. Pentacene is a famous semiconductor nowadays, but its journey began in 1991 [61]. Interestingly, all these devices exhibited *p*-type conductivity, and the electron conductive materials were beyond the scope of organic electronics. The *n*-type OFET device was reported in 1994 by Brown *et al.* and used TCNQ as an active layer [62]. The most well-known *n*-type semiconductor, fullerene C_{60}, was suggested one year later, in 1995 [63]. Since fullerene was a very perspective material with relatively high electron mobility, various applications were introduced, such as *pn* heterostructures [64]. Besides fullerene C_{60} other fullerene-based materials were characterized in the next years [65]. Also, modification of the gate insulator or injection electrodes took place in the late '90s [66]. Surprisingly, the holy grail of microelectronics, the single-crystal semiconductor, was accomplished in 2003 using rubrene [67]. Although the electron properties were significantly better, the research remained focused on polycrystalline devices. In the same year, the tetracene-based organic light-emitting transistor (OLET) shined a light [68]. Among aromatic rings, the thienoacenes and thiophene benzene fused compounds such as DNTT and BTBT were introduced in OFET devices in 2006-2007 [69, 70]. Almost immediately, they began popular due to the high effective mobility. The first 8-bit processor deposited on the flexible substrate was demonstrated in 2012 to illustrate the capability of the technology [71]. Later, the novel organic semiconductors and optimization of deposition techniques lead to the hole and electron mobility as high as 52.7 and 27.8 $cm^2/V.s$ [72, 73].

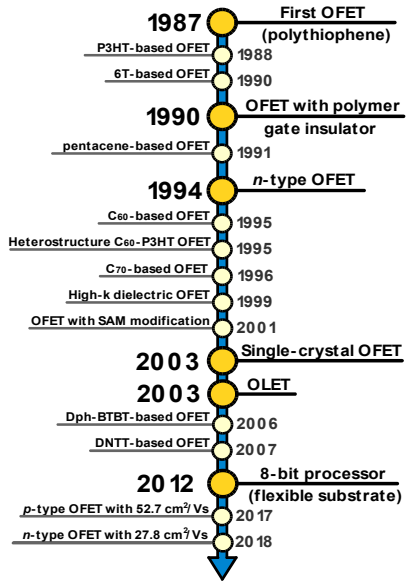


Fig. 1.12. The timeline of OFET evolution.

1.3.2. How the OFET Works?

The structure of OFET is very similar to thin-film transistors based on inorganic materials in the metal-oxide-semiconductor structures (MOSFET). The three-dimensional geometry of the most common and fundamental structure, known as top contact – bottom gate organic field-effect transistor, is depicted in Fig. 1.13. OFET in this structure consists of two thin-film layers – dielectric and organic semiconductor layer and three metal electrodes – source, drain and gate. The active charge-transport layer consists of a thin-film organic semiconductor with source and drain electrodes. The conductive channel in the OFET device is created in the organic semiconductor layer, especially at the semiconductor/gate insulator interface. The gate insulator layer can be fabricated of organic as well as inorganic materials. The most important is to satisfy the requirements on low leakage currents (*i.e.* gate insulator must have a high electrical resistance). Source and drain electrodes are mainly formed of metal layers. The electrode deposition can be done by the thermal evaporation in a vacuum, the printing techniques (*e.g.* inkjet printing or screen printing), or even by mechanical lamination.

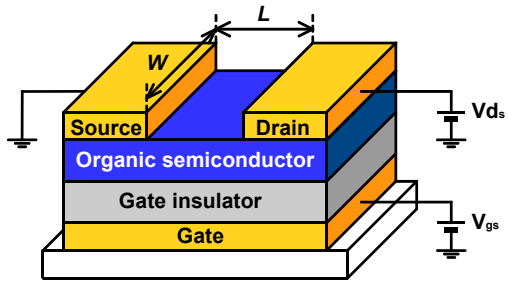


Fig. 1.13. Schematic drawing of the OFET structure in a top contact – bottom gate configuration.

The conductive channel is formed between the source and drain electrodes through an organic semiconductor if the appropriate voltage is applied to the gate electrode. In the case of OFET devices, the channel length L between the source and drain electrodes is usually in the order of hundreds of micrometres, whereas the width W is greatly larger and varies from millimetres to centimetres. In general, the channel/width length is limited by the fabrication technology, *i.e.* dimensions of the shadow mask used during the metal evaporation or printing resolution [8, 74]. The gate electrode potential controls the accumulation layer on the semiconductor/gate insulator interface that is crucial for the current flow between the source and drain electrodes. Hence, OFET can be used in a wide range of electronic systems as a switching device. The fundamental relations describing the current-voltage characteristics of OFET are identical to the already known Shockley's equations describing the metal-oxide-silicon field-effect transistors (MOS FETs) [53].

Regarding the applied gate-source voltage, we recognise several regions in the current-voltage characteristics. If the gate-source voltage V_{gs} is greatly lower than the threshold voltage V_{th}, the OFET device is closed, and only a low level of the off-current is observed. Increasing the gate-source voltage V_{gs} will its value approaches the threshold

voltage, the device is in the *subthreshold region*, and it is starting to turn on. The current is very low, but it rises in an exponential way. Above the threshold region, $V_{\mathrm{gs}} > V_{\mathrm{th}}$, the conductive channel is formed between the source and drain electrodes; however, due to the low electric field, it is still limited by the bottleneck denoted as pinch-off, and the drain-source current is conserved even though the drain-source voltage V_{ds} is increased. Since the output current is saturated, we recognise this voltage region as a *saturated* one. The increase of gate-source V_{gs} voltage greatly above drain-source voltage V_{ds} gives a rise of the highly conductive channel, and the organic semiconductor exhibits Ohmic behaviour. Considering linear current dependence on the applied voltage, the Ohmic character, the voltage region is identified as a *linear* one. Furthermore, the drain-source current dependence on the drain-source voltage represents the output current reliance; hence, it is named the *output characteristic*. On the other hand, the drain-source current dependence on the gate-source voltage demonstrates the transfer nature of the switching device; therefore, it is recognised as a *transfer characteristic*.

To express the nature mentioned above of OFET devices is used the gradual channel approximation proposed by Shockley. This theory approximates the charge transport in one dimension, assuming the separation of the source-drain electrodes greatly larger than the gate-source electrode separation. In other words, it requires channel length greatly larger than the film thicknesses (organic semiconductor and gate insulator films). Subsequently, if the conductive channel is formed (linear region) the drain-source current I_{ds} can be expressed as

$$I_{\mathrm{ds}} = \frac{WC_{\mathrm{g}}}{L}\,\mu\left(V_{\mathrm{gs}} - V_{\mathrm{th}} - \frac{1}{2}V_{\mathrm{ds}}\right)V_{\mathrm{ds}}, \tag{1.11}$$

where C_{g} and μ stand for the material parameters, namely the gate insulator capacitance per unit of area and the charge mobility in an organic semiconductor, respectively. The gate capacitance includes material properties and geometry of gate insulator layer, $C_{\mathrm{g}} = \varepsilon_0\varepsilon_{\mathrm{r}}/d$, where $\varepsilon_0\varepsilon_{\mathrm{r}}$ and d are the dielectric constant and the thickness of the gate insulator. It also means that with the reduction of dielectric insulator thickness or the rise of relative permittivity, the capacity increases and the drain-source current also grows up. It should be noted here that this relation is valid for the high gate-source voltage only, $V_{\mathrm{ds}} < V_{\mathrm{gs}} - V_{\mathrm{th}}$, whereas for low gate-source voltages (saturated region), $V_{\mathrm{ds}} > V_{\mathrm{gs}} - V_{\mathrm{th}}$, the relation is simplified,

$$I_{\mathrm{ds}} = \frac{WC_{\mathrm{g}}}{2L}\,\mu\,(V_{\mathrm{gs}} - V_{\mathrm{th}})^2 \tag{1.12}$$

The output and transfer characteristics, Fig. 1.14, offer the possibility of extracting the basic parameters of the transistor. The material parameters related to the organic semiconductor, especially the mobility and the threshold voltage. The mobility can be evaluated from the transfer characteristics by modifying the equation (1.12) as follows

$$\mu = \frac{2L}{WC_{\mathrm{g}}}\left(\frac{\partial I_{\mathrm{ds}}^{1/2}}{\partial V_{\mathrm{gs}}}\right)^2 \tag{1.13}$$

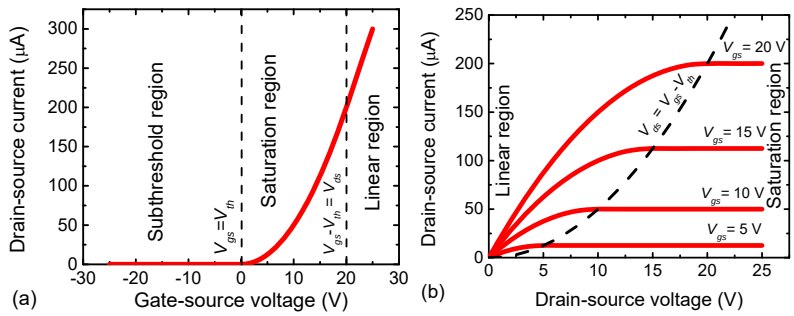


Fig. 1.14. Typical (a) transfer, and (b) output characteristics of OFET. Basic operation regions are also denoted.

Demonstration of the threshold voltage and mobility evaluation is shown in Fig. 1.15 (a). Another parameter describing the transistor's quality as the switching device is the ratio of the output currents in the on-state and the off-state, so-called on/off ratio (see Fig. 1.15 (b)). It defines the difference between the open and closed channel and plays a key role in logic circuits or active matrix display organic light-emitting diode backplanes. Even though the OFET devices cannot offer mobility as high as silicon-based FETs, the channel can be properly closed, and the on/off ratio usually reaches the level from 10^5 up to 10^8. The channel transconductance is used to evaluate conductive channel properties from the transfer characteristic

$$g_{\mathrm{m}} = \left(\frac{\partial I_{\mathrm{ds}}}{\partial V_{\mathrm{gs}}}\right)_{V_{\mathrm{ds}}} \tag{1.14}$$

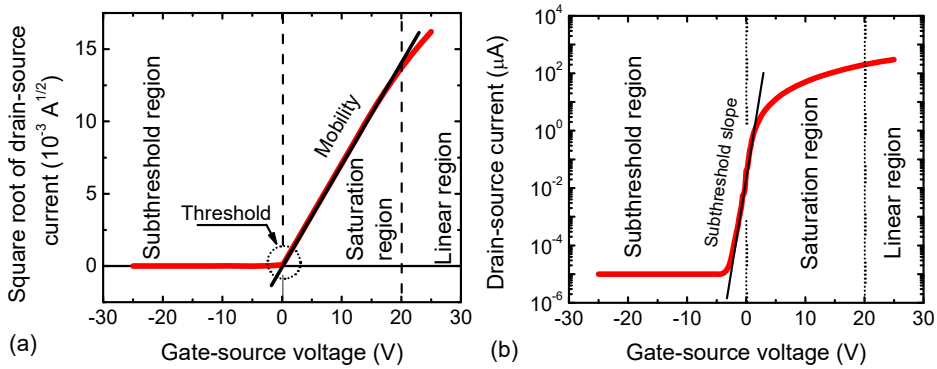


Fig. 1.15. Other plots of the output characteristics. (a) Square-root plot for estimation of the mobility and the threshold voltage in the saturated region; (b) Semi-log scale for evaluation of the subthreshold slope in the subthreshold region.

Especially, it is a powerful tool in the subthreshold region, where the current rises exponentially, Fig. 1.15 (b). In details, the semi-log scale of the output characteristic in

the subthreshold region is linear, and the subthreshold slope can be estimated. The subthreshold slope expresses how abrupt is the transition from the off-state to the on-state. Notably, the subthreshold slope's reciprocal value, the so-called subthreshold swing, is commonly used since it clearly describes the voltage required to increase the current by one decade (V/dec).

1.3.3. OFET Architecture

The OFET device architecture is distinguished in accordance with current flow and the electrode geometry. Since the OFET devices are thin-film structure deposited on the planar solid substrate, the current flow can be in the plane of the substrate, the horizontal architecture, or in the normal direction, the horizontal architecture.

1.3.3.1. Horizontal Architecture

Top contacts

Top contact geometries are defined by the deposition of source/drain contacts on the top of the organic semiconductor layer. In other words, the organic semiconductor is deposited on the substrate, and source/drain electrodes are formed subsequently. The bottom electrode can be situated under the organic semiconductor, the top contact – bottom gate geometry, or above the organic semiconductor, the top contact – top gate geometry, see Fig. 1.16.

The device geometry selection defines a requirement on the electrode fabrication technology to avoid organic semiconductor damage. There are various common options for the gate electrode materials, such as metals or metal oxides. Metal layers provide high conductivity, while the metal oxide (*e.g.* indium tin oxide or doped zinc oxide) offer optical transparency. If the gate electrode is deposited as a continuous layer, the pattering technique, like laser ablation or photolithography, is necessary. For organic semiconductor testing, the highly doped silicon wafer with thermal oxide is applied as a gate electrode with a gate insulator layer even though this approach has no industrial application.

The advantages of this geometry are relatively simple fabrication and significantly lower contact resistance due to the penetration of the metal used for the electrodes into the organic semiconductor layers. The second approach, the top contact – top gate geometry, is based on the deposition of the organic semiconductor layer directly on the substrate. The source and drain electrodes deposited on the organic layer are covered with a gate insulator layer. Finally, the gate electrode is formed on the top, Fig. 1.16 (b) [75, 76]. Although the top contact – top gate needs more complex design and fabrication technology limitations, it offers an advantage of device encapsulation.

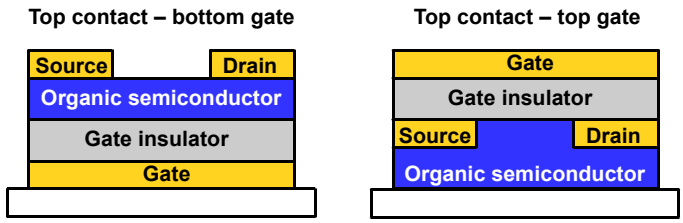


Fig. 1.16. The OFET horizontal architectures with top contact – bottom gate or top contact – top gate geometry.

Bottom contacts

In the bottom contact geometry, the source and drain electrodes are deposited prior to the organic semiconductor, Fig. 1.17. The obvious advantage of this geometry is the possibility of fine electrode patterning technique application. In details, the photolithography process can be utilised to fabricate devices with short channels without the risk of organic semiconductor degradation. On the other hand, the bottom contacts lead to greatly higher contact resistance as well as nonlinear dependence of the drain-source current at low drain-source voltages. This phenomenon causes nonlinear series resistance between the source and drain electrodes [77]. Similar to the top contact approach, also here, we meet the possibility of the top gate geometry [78].

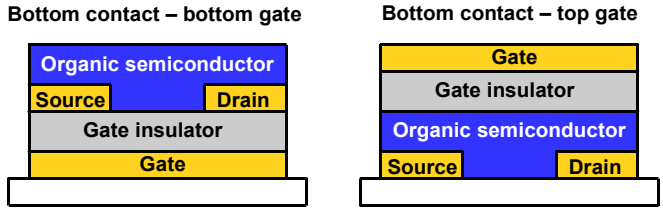


Fig. 1.17. The OFET horizontal architectures with bottom contact – bottom gate or bottom contact – top gate geometry.

1.3.3.2. Vertical Architecture

Till now, we discussed OFET devices with charge transport in the plane of the substrate, the horizontal geometry. Another alternative design offers the charge transport in the normal direction, the vertical architecture. Therefore, the channel length is in a sandwich-like structure defined by the thickness of the organic semiconductor layer that separates the source and drain electrodes. Here, the gate electrode is located between the source and drain electrodes or beside the channel. The advantages of vertical architecture are short channels offering fast devices and large electrode areas providing high output current [79]. Various designs of OFET with vertical architecture have been proposed in the last two decades, see Fig. 1.18.

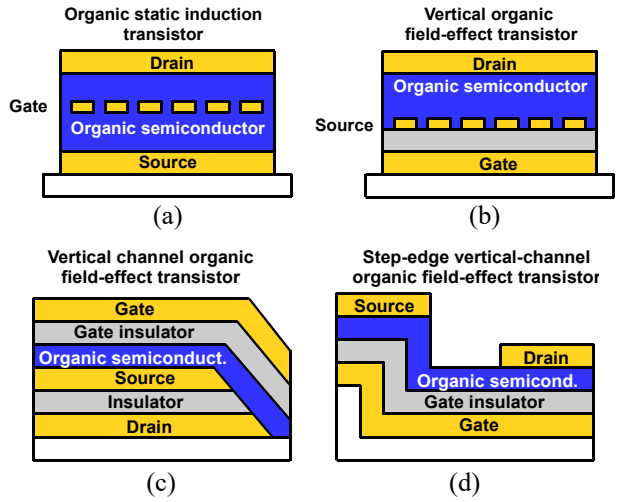


Fig. 1.18. Vertical structures of organic transistors: (a) Organic SIT; (b) Vertical OFET; (c) Vertical-channel organic field-effect transistor; (d) Step-edge vertical-channel organic field-effect transistor.

Organic static induction transistor (OSIT)

This type of vertical OFET geometry was first proposed by Kudo [80] as an analogy to an inorganic SIT transistor. In this design, the charge carriers are transported through an organic semiconductor layer sandwiched between the source and drain electrodes, while the current is controlled by a grid-shaped gate electrode located in the centre of the organic semiconductor layer, as shown in Fig. 1.18(a). However, due to the resulting leakage currents at higher gate-source voltages and the extremely low on/off current ratio, this geometry is not widely used. The uncomplicated structure of OSIT and the absence of a gate insulator allows us to create a transistor easily, even on a flexible substrate. This means that OSIT can be produced by a thermal evaporation deposition (PVD) in a single run, without the need of breaking the vacuum [80].

Vertical organic field-effect transistor (VOFET)

Vertical OFET device consists of two parts: the diode (source/organic semiconductor/drain) and the capacitor (source/insulating layer/gate), whereas the source electrode is common for diode and capacitor, Fig. 1.18(b). For correct function must be fulfilled two main conditions: (i) high capacity of the capacitor and (ii) non-continuous or patterned source electrodes. The very first devices used a non-continuous metal layer as a source electrode [81], whereas later, the patterned grid structure was used. As a result, the vertical OFET in such a structure behaves like a diode where the injection electrode can be expanded by the application of gate-source voltage [82, 83].

Vertical-channel organic field-effect transistor

A key feature of a vertical-channel OFET is the short length of the channel, which is defined by the thickness of the gate insulator layer located between the source and drain

electrodes, similar to horizontal OFET architecture. After deposition of the source and drain electrodes, between which is deposited a dielectric layer, the entire layer is chemically patterned or stamped in the design of a letter V. Subsequently, a layer of organic semiconductor, a second insulator layer and a gate electrode are deposited. These layers copy the previously patterned surface morphology, as shown in Fig. 1.18(c). The resulting channel length is usually around 1 μm, while the shorter channel would suffer an increased leakage current breaking through the dielectric layer between the source and drain electrodes [84, 85].

Step-edge vertical-channel organic field-effect transistor (SVC OFET)

This device geometry is also known as the three-dimensional OFET, is created on a patterned substrate to create a sharp edge, Fig. 1.18 (d). Subsequently, the gate electrode, the dielectric layer and the organic semiconductor are deposited. In the last step, the top electrodes, source and drain, are formed by deposition of the metal under an inclined angle; hence the shadow defines the channel region. In this approach, the edge of the substrate serves as a shadow mask, whereas the channel is formed along the sidewall of the edge [86].

1.3.4. Materials

1.3.4.1. Substrates

Even though there are many types of OFET substrates, we can divide them into two major categories: organic (polymer) and inorganic substrates. Typical examples of polymer substrates are polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polyethylene (PE) and polyimide (PI). Polymer substrates are flexible and lightweight. Some polymers such as PEN, PET, and PI also have sufficient thermal resistance, so these are suitable as substrates of OFETs. On the other hand, inorganic substrates such as glass, quartz, and silicon wafer excel over polymer substrates by their high melting point, lower surface roughness and lower diffusivity of chemicals or air. Substrate such as heavily-doped silicon (Si) wafer is widely used as gate electrodes for organic semiconductor testing [87].

1.3.4.2. Insulator Layer

Even though the organic semiconductor had been applied in organic field-effect transistor from the early beginning, the organic gate insulators did not reach an acceptable level, and inorganic insulators were applied for early-stage devices. The first polymer insulator layer applied in the OFET device was used in 1990 [60, 88]. Since 1990, a large number of different insulating materials have been investigated. Material research has focused on inorganic, organic, or organic-inorganic hybrid materials to create high-capacity thin layers with low leakage currents. The second requirement was simple deposition and compatibility with organic semiconductors or metal electrodes. The gate insulator layer in the OFET device is mostly sandwiched between the gate electrode and the organic

semiconductor. This structure creates two interfaces (gate electrode/gate insulator and gate insulator/organic semiconductor) with different requirements. Furthermore, it is necessary to cover the gate electrode perfectly to avoid high leakage current via pinholes.

The gate insulator/organic semiconductor interface quality is equally, if not more important, because a conductive channel is formed at this interface; therefore, the insulating layer also affects the mobility. Another critical parameter is the capacity per unit area because it determines the drain-source current and operating voltage [89]. The quality of the conductive channel is also influenced by the interface roughness, the surface energy, as well as the interface charges [90]. The organic semiconductor is deposited directly on the gate insulator layer in most OFET devices. The gate insulator layer affects the arrangement of the semiconductor close to the interface. Therefore, the molecular alignment of organic semiconductor is critical for high-performance OFETs [91]. The basic parameters for choosing the suitable dielectric layer are dielectric constant, low-leakage current, deposition method and air stability. The dielectric materials used in OFET must be a sufficient insulator with a specific electrical resistance above 10^8 Ω.cm. Their air stability is also a very important factor. The solvent in which the material is soluble must not etch the semiconductor layer after deposition of the gate insulator layer. Another requirement is sufficient adhesion to the substrate and homogeneity of the deposition layer. A great advantage is also compatibility with flexible substrates. From an application point of view, dielectric materials must also meet other specific requirements, which include a low cost of material and low production costs for the manufacture of devices and circuits of organic electronics [92].

Inorganic insulator materials

In the current generation of inorganic integrated circuits, the most common material is SiO_2 (most often created by thermal oxidation of silicon), which is the most widely used inorganic material suitable for the dielectric layer of thin-film transistors. Despite its relatively low dielectric constant (ε_r = 3.9) and a significant tunnelling current through thin films. In organic electronics, SiO_2 is commonly used to produce OFET in analysing and testing new organic semiconductors. Other standard inorganic dielectric materials include alumina (Al_2O_3) or tantalum oxide (Ta_2O_5) [92]. Other commonly used insulating materials are ceramics based on barium zirconate titanate (ε_r = 17.3) and strontium titanium barium (ε_r = 16), and with pentacene as a semiconductor layer, devices achieved mobility more than 0.3 cm^2/V.s at an operating voltage less than 5 V. Barium titanate ($BaTiO_3$) is also one of the most commonly used compounds, which is the subject of a long-term study for its interesting ferroelectric and piezoelectric properties in the high-temperature range. Similarly, the group of materials based on compounds of lead (Pb), zirconium (Zr) and titanium (Ti) - $PbTiO_3$ and $PbZrO_3$ achieves excellent dielectric and piezoelectric properties than $BaTiO_3$ [92].

Organic insulator materials (polymers)

The main motivation to look for organic insulator alternatives compared to thermal oxide is to significantly reduce the production cost and achieve the mechanical flexibility of the devices. Polymers used as insulator materials are very attractive for use in electronics.

They have relatively good insulating properties, while thin layers can be deposited by uncomplicated and inexpensive methods, such as spin-coating, dip-coating, printing techniques, *etc*.

The most commonly used polymers (Fig. 1.19) include polyethylene (PE), polypropylene (PP), poly(vinylphenol) (PVP), polystyrene (PS), poly(methyl methacrylate) (PMMA), poly(vinyl alcohol) (PVA), poly(vinyl chloride)) (PVC), poly(vinylidene fluoride) (PVDF) and poly(tetrafluoroethylene) (PTFE). Another way to form a polymer insulator layer is to monomer deposition in a vacuum directly on the surface of the gate electrode with a molecular cross-linking after deposition. An example of this technology is poly-para-xylylene (parylene), where pyrolysis of a para-xylylene dimer generates radicals which polymerise on the substrate at room temperature to create an insulator layer [92].

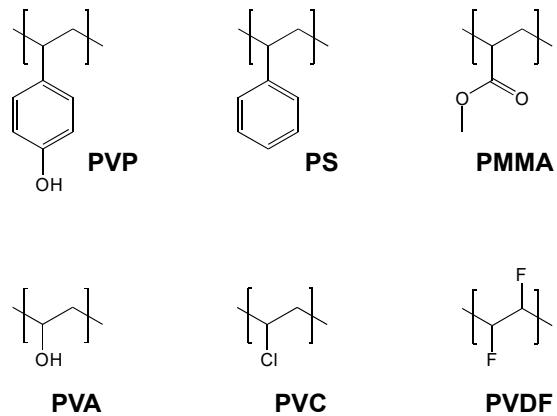


Fig. 1.19. Molecular structures of PVP, PS, PMMA, PVA, PVC, and PVDF.

1.3.4.3. Semiconductor Layer

In the case of organic semiconductors, we start from the intrinsic properties of organic materials. Note that both types of charge carriers, electrons and holes, can be transported in organic semiconductors, but in most cases, one type of charge carriers has significantly higher mobility than the other one (the usual difference is 3 to 8 orders of magnitude). It should be mentioned here that the organic semiconductors are used without further doping; therefore, the type of conductivity is determined by the mobility. According to the mobility, we recognise organic semiconductors as *p*-type, *n*-type semiconductors. If the mobility is comparable, we refer to the materials as ambipolar materials [93]. The *n*-type (*p*-type) organic semiconductors have significantly higher mobility of electrons (holes) than holes (electrons). Ambipolar materials have comparable values of electron and hole mobility and can transport equally both types of charge carriers, electrons and holes.

In contrast to inorganic semiconductors, organic semiconductors have a negligible concentration of intrinsic free charge carriers, and almost all free charges come from the

injection electrode. Therefore, the choice of source/drain electrode significantly affects the concentration of free charge carriers in the organic semiconductor and thus plays an important role in determining the conductivity type of the semiconductor. In other words, even an ambipolar organic semiconductor will exhibit only one type of conductivity if we choose an injection electrode that will provide a continuous injection of one type of charge carrier, while for the other type, it will act as a barrier electrode.

Pentacene is the most popular and researched semiconductor material in organic electronics nowadays. Pentacene is a polyaromatic hydrocarbon consisting of five aromatic benzene nuclei (Fig. 1.20). The thin polycrystalline layer acts as a *p*-type semiconductor and can be used to fabricate OFET [94]. Despite its popularity, it also has its disadvantages, as it is insoluble and can be deposited only by thermal evaporation [95]. Although various materials with significantly higher mobility are already known, their frequent use in various experiments is not only due to the relatively low production cost, but this material often also serves as a reference organic semiconductor. Since the major disadvantage of pentacene is its insolubility in organic solvents, its modification with the triisopropylsilylethynyl (TIPS) functional group has also been proposed to increase pentacene solubility [96, 97]. The material treated in this way can be deposited from the solution. Another important group of materials with a *p*-type conductivity are materials using thiophene groups. A typical representative of this group is sexithiophene [59] a representative of the oligothiophene family. On the other hand, a typical representative of polymers in this group is poly(3-hexylthiophene-2,5-diyl) (P3HT), which has found not only its irreplaceable role in organic photovoltaics but also finds application in organic transistors [58]. One of the specific materials with relatively high mobility is rubrene, a tetraphenyl derivative of tetracene [67]. Another family of *p*-type organic semiconductors are phthalocyanines, a popular research subject in the 80s and 90s of the last century. The most commonly used derivative is copper phthalocyanine (CuPc). Despite its low mobility, it is still of interest for sensory or photovoltaic applications [98]. Examples of *p*-type organic semiconductors are shown in Fig. 1.20. Fig. 1.21 illustrates a typical organic semiconductor with *n*-type conductivity [99]. Fullerene (C_{60}) is the best known and most studied organic semiconductor with *n*-type conductivity. Although these materials are widely used in organic photovoltaics, the preparation of electronic devices is quite demanding due to their low stability and sensitivity to oxygen or humidity.

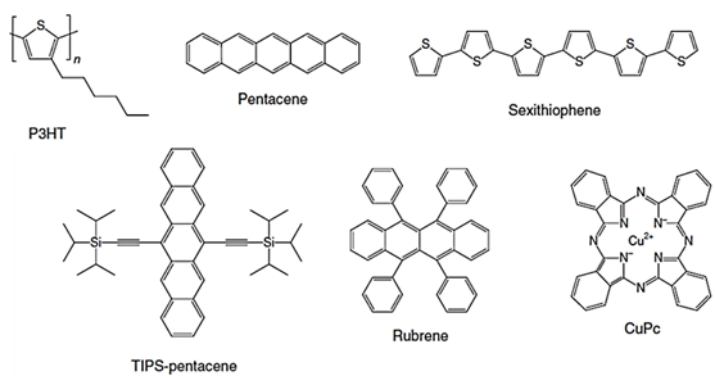


Fig. 1.20. Molecular structures of selected organic *p*-type semiconductors.

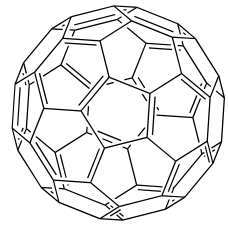


Fig. 1.21. Molecular structure of typical organic *n*-type semiconductors.

Fused benzene-thiophene organic semiconductors have been increasingly investigated in recent years. One of the basic structures of these molecules is benzothieno (3,2-b) (1)-benzothiophene (BTBT), consisting of a thiophene group and two benzene nuclei [100]. Xie *et al.* fabricated flexible BTBT-based OFETs on a plastic PET, and the corrected highest and average mobilities were up to 18.3 and 13.2 $cm^2/(V.s)$, respectively [101]. Many derivatives of BTBT organic semiconductors have been proposed and designed to be highly soluble, to achieve high stability and high mobility. Another group of organic semiconductors based on thienothiophenes combined with diacene are dinaphtho(2,3-b: 2 ', 3'-phthieno (3,2-b) thiophene (DNTT). According to recent studies, OFET devices using DNTT as a semiconductor layer showed mobility of free charge carriers in the range of 9.9-13.02 $cm^2/V.s$ [102, 103]. Another interesting thiophene-rich heteroacene is dibenzothiopheno(6,5-b: 6 ', 5'-f)thieno(3,2-b)thiophene (DBTTT), which is based on an increase in intermolecular charge transfer through a strong S-S interaction. [104]. The molecular structures of organic semiconductors with high mobility of free charge carriers are shown in Fig. 1.22.

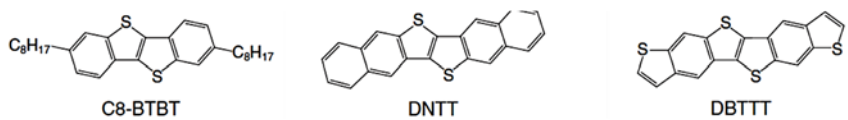


Fig. 1.22. The molecular structures of organic semiconductors with high mobility.

1.3.4.4. Electrodes

The energy difference between the work function of metal source/drain electrodes and the HOMO level of the *p*-type organic semiconductor (LUMO level in the case of *n*-type organic semiconductor) determinates the injection barrier. The injection barrier at the metal electrode/organic semiconductor interface influences the injection of charge carriers. Therefore, choosing the appropriate metal used to manufacture the source and drain electrodes is the most important parameter of its work function as listed in Table 1.1. The metals used to manufacture the contacts thus depend on the type of organic semiconductor. Gold (Au), platinum (Pt), silver (Ag), or copper (Cu) are often used for *p*-type semiconductors because they are metals with high work function. However, gold is the most common choice for *p*-type for OFETs due to its high work function and stability.

The work function of Au is about 5 eV, and the energy level of HOMO of most of the *p*-type of organic semiconductor is also close to this level, which means that can be formed Ohmic contact between Au and *p*-type organic semiconductor. Adding a thin layer of nickel on the substrates improves the adhesion of the gold on the oxide. Alternative non-metallic materials such as conductive conjugated polymer PEDOT:PSS or graphene have also been tested [105-109]. For the *n*-type semiconductor are used mainly metals with low work function, such as calcium (Ca), samarium (Sm), barium (Ba), or magnesium (Mg). Note that the selection of electrode material has a great impact on the contact resistance level [111].

Table 1.1. Comparison of the work function most commonly used materials to fabricate the source and drain electrodes [106-110].

Material	Work function (eV)	Material	Work function (eV)
Gold (Ag)	5.1	Magnesium (Mg)	3.7
PEDOT:PSS	5.0	Calcium (Ca)	2.9
Copper (Cu)	4.65	Samarium (Sm)	2.7
Silver (Ag)	4.3	Barium (Ba)	2.5

1.3.5. Selected OFET Application

1.3.5.1. Controls Circuits

Low-frequency (OLED backplanes)

The most envisioned application of OFETs is the utilisation in the backplane of active-matrix OLED (AMOLED) displays and to replace the amorphous silicon (a-Si) or low-temperature polysilicon (LTPS). In contrast to a-Si or LTPS, organic semiconductors are deposited at low temperatures and also offers the possibility of the plastic substrate or printing techniques. A great advantage is also the high transparency of these devices (compared to a-Si or LTPS 20 % to 80 %) [112]. A disadvantage is a low mobility, but recently progress on organic semiconductor shows a significant increase in semiconductor mobility to sufficient levels [73]. Several companies are working nowadays on OFET-based displays, *e.g.* Mattrix Technologies, FlexEnable, Polyera or SmartKem [112].

High-frequency (RFID)

One of the potential applications of OFET is the passive RFID (Radio Frequency IDentification) tag. Passive RFID tags consist of an antenna and microchip, which represents the separate functions of the circuit. Standard microchips used in RFID tags are based on silicon technology. At present, the production price of RFID is circa 0.1-0.2 €, but it is too high for mass use in low-cost products. In the future, can using of conductive polymers to replace the metal antenna and silicon microchip to replace with OFET in mass production. The price of manufactured RFID tags can be decreased to about 0.01-0.02 €.

This cost reduction would allow mass use for all types of products. Today, it is possible to use metal or nanoparticle materials to manufacture RFID antennas, whereas it can be achieved the required frequencies (13.56 MHz or even 433 MHz – 960 MHz). However, the fabrication of antenna using conductive polymers is still a great challenge. The second challenge is the manufacture of high-frequency of OFETs to replace inorganic microchip. Many research labs around the world are trying to develop the high-speed transistors necessary for RFID tags. As already mentioned, the main motivation is low-cost fabrication due to printing technology. In the future, RFID tags can be with printing technology applied to every product and can replace the widely used optical barcode. Fig. 1.23 illustrates inductively-coupled passive 64-bit organic RFID tag operating at a 13.56 MHz and magnetic field strength under level required by the ISO standards [113].

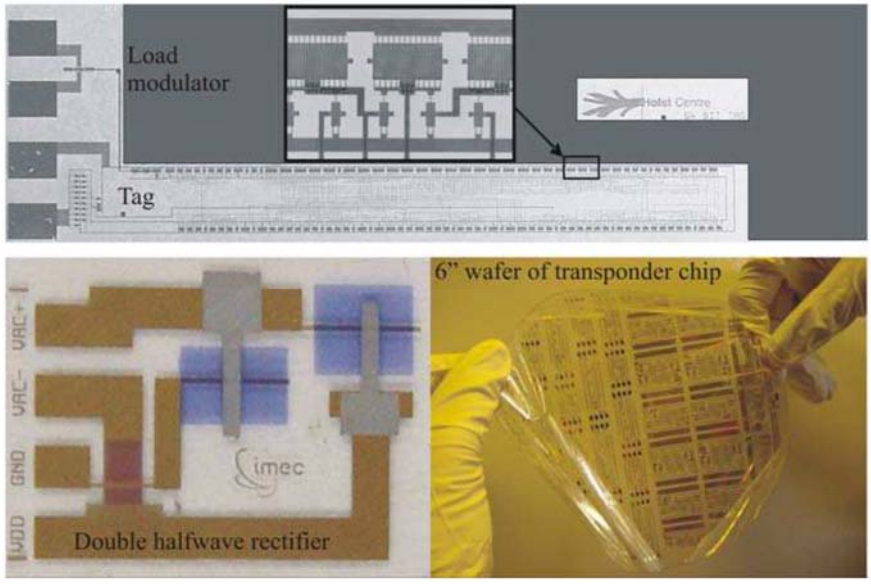


Fig. 1.23. Pictures of the transponder foil and the load modulator foil (top), the double halfwave rectifier foil (bottom left) and the 6" wafer full of transponder chips (bottom right). © 2010 Kris Myny, Soeren Steude, Peter Vicca, Monique J. Beenhakkers, Nick A. J. M. van Aerle, Gerwin H. Gelinck, Jan Genoe, Wim Dehaene, and Paul Heremans. Originally published in Radio Frequency Identification Fundamentals and Applications under CC BY-NC 4.0 license. Available from: 10.5772/175.

1.3.5.2. Non-volatile Memories

Organic non-volatile memories are classified into three types based on (i) Resistors; (ii) Capacitors, and (iii) Transistors. In this section, we will describe memory devices based on transistors. An organic ferroelectric field-effect transistor (OFeFET) is an organic field-effect transistor with ferroelectric thin-films as a gate insulator. The ferroelectric layer is capable of two reversible polarisation states that can be switched by an electric field higher than the coercive field. In 2002, Katz *et al.* reported

nonferroelectric OFET device with a floating gate structure [114]. The first ferroelectric *p*-channel OFET based on organic MXD6 and pentacene was demonstrated in 2004 [115].

The first ferroelectric n-channel OFET was introduced in 2004 [116]. Th. B. Singh *et al.* demonstrated an organic non-volatile memory device based on OFETs using a polymeric electret as a gate dielectric. In 2005, Naber *et al*. successfully demonstrated non-volatile FET memory device, based on [poly(vinylidene fluoride–trifluoroethylene)] P(VDF-TrFE) as the ferroelectric insulating layer and poly[2 -methoxy -5 -(2′ -ethylhexyloxy) -p -phenylenevinylene] (MEH-PPV) as the conducting channel [117]. So far, PVDF-TrFE is one of the most promising organic ferroelectric (insulating) material for non-volatile memories. Because PVDF-TrFE offers important properties, for example, reversible polarisation, short switching time, and good thermal stability [118-120]. Xu *et al.* developed a high performance low-voltage operating flexible FeOFET non-volatile memory based on poly(vinylidene-fluoride-trifluoroethylene-chlorotrifluoroethylene) and poly(styrene) P(VDF-TrFE-CTFE)/ PS dielectric. As a result, a flexible FeOFET non-volatile memory with mobilities up to 0.2 cm^2/V.s and P/E (**P**rogramming and **E**rasing) voltages of ±10 V reliable switching endurance over 150 cycles, as depicted in Fig. 1.24 [121].

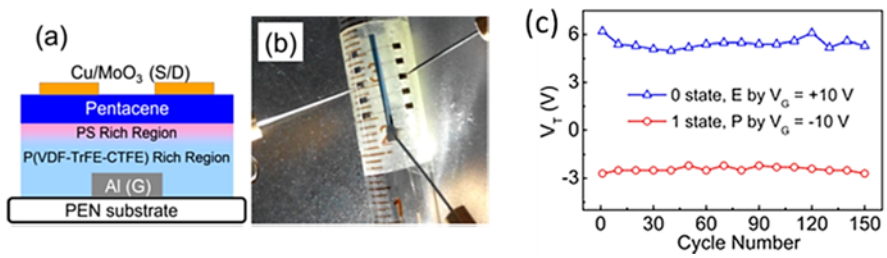


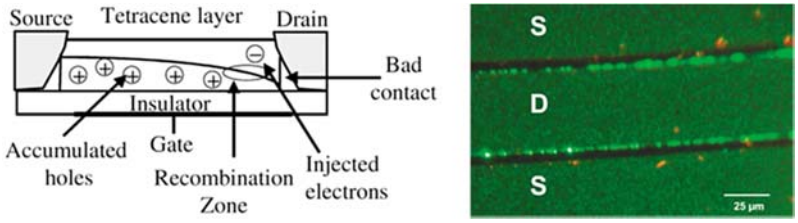
Fig. 1.24. (a) The structure schematic and (b) the photograph of the flexible Fe-OFET NVMs in a bending state (c) V_T in binary 1 and 0 states as a function of the cycle number of applied cyclic P/E voltages. Reprinted from M. Xu, L. Xiang, T. Xu, W. Wang, W. Xie, D. Zhou, Applied Physics Letters, Vol. 111, 2017, 183302, with the permission of AIP Publishing.

Due to non-destructive readout, low power consumption, light-weight, and rewritability, are OFeFETs highly attractive for research with the aim of commercial application. OFeFETs are promising for non-volatile memories devices because of the reversible polarisation switching mechanism. In the future, after solving all the challenges for the preparation of high-performance devices, OFeFETs fabricated on plastic substrates will be suitable for flexible electronics applications.

1.3.5.3. Lighting Devices (OLET – Organic Light-Emitting Transistor)

Most organic semiconductors can effectively transport only holes or only electrons. However, a specific family of organic semiconducting materials offer comparable mobility of electrons and holes, the ambipolar behaviour. Note that even though the ambipolar semiconductor is applied in the OFET structure, the type of charge transported

across the channel depends on the applied voltage. In other words, the charge transport may be done by a single charge carrier (electron or hole) or both kinds of carriers simultaneously. In the case of ambipolar transport, the electron-hole recombination can take place in the channel region. As a result, the light is emitted. Devices with this ability of operation are denoted as organic light-emitting transistors (OLETs). In basic classifications, the OLETs are classified into two categories unipolar or ambipolar OLETs [122]. The function of the OLET consist of two principal, first one is the switching part from OFET, and the second one is the light-emitting part from OLED [123]. The OLET has been envisioned for application in optical information technology. First OLET devices were introduced in 2003 by Hepp *et al*. In this work, researchers report the observation of light emission from an OFET based on a vacuum deposited tetracene thin film as illustrated in Fig. 1.25.



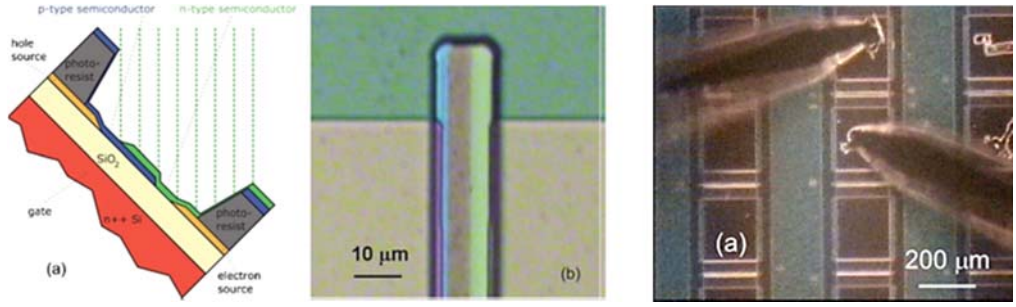
(a) (b)

Fig. 1.25. (a) Structure of OLET, and (b) Image of the electroluminescence from a tetracene OLET. Reprinted figure with permission from A. Hepp, H. Heil, W. Weise, M. Ahles, R. Schmechel, H. von Seggern, Physical Review Letters, Vol. 91, 2003, 157406. Copyright 2010 by the American Physical Society.

This devices of OFET with structure top contact-bottom gate was a unipolar *p*-type device [68]. It should be noted here that unipolar OLETs have an emissive zone close to the electrode due to the significantly unbalanced electron and hole mobilities. On the contrary, the ambipolar devices with comparable electron and hole mobilities have the emissive zone in the channel region. In addition, the position of the emission zone (the zero potential position) can be finely tuned by the applied voltage. [124]**.** In 2006, De Vusser *et al.* proposed the structure of OLET that involves a *pn*-junction consist of a *p*-type material with low electron affinity and an *n*-type material with high electron affinity in the channel region [125]. This was achieved by angled thermal deposition of the two materials. Recombination of electrons and holes in these devices takes places where *p*- and *n*-type materials overlap with green light emission, as illustrated in Fig. 1.26.

The co-evaporation of *p*- and *n*-type semiconductor was proposed by Rost *et al*. to achieve OLET device using PTCDI-$C_{13}H_{27}$ and α-quinquethiophene (α-5T) [124]. Interestingly, the light modulation by the drain-source current was possible. A later study by Loi *et al*. found that the light emission depends on the material ratio [126]. It has been reported that the excess *p*-type semiconductor, α -5T, causes light suppression even though ambipolar transport is present. This phenomenon has been attributed to the quenching of PTCDI-$C_{13}H_{27}$ excitons. On the other hand, the excess of *n*-type semiconductor,

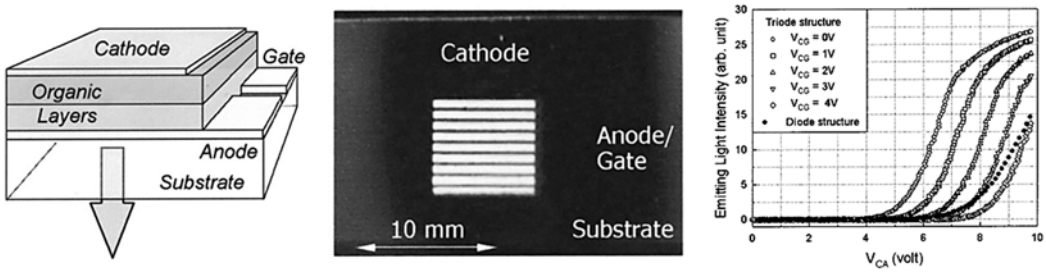
PTCDI-$C_{13}H_{27}$, the unipolar electron transport accompanied with the light emission was observed. Hence, the optimum light emission conditions require a balanced ratio of both semiconductors.



(a) (b) (c)

Fig. 1.26. (a) Schematic illustration of the *n*-type semiconductor deposition; (b) and (c) microphotograph of the device. Reprinted from S. De Vusser, S. Schols, S. Steudel, S. Verlaak, J. Genoe, W. D. Oosterbaan, L. Lutsen, D. Vanderzande, Paul Heremans, Applied Physics Letters, Vol. 89, 2006, 223504, with the permission of AIP Publishing.

Another classification of OLETs is for (a) planar OLETs and (b) vertical OLETs, and so far, we discussed planar types only. The vertical types of OFET have already been mentioned above. The coupling of organic vertical static induction transistor (OSIT) and OLED has been proposed for light-emitting devices for flexible displays with low operation voltage and high brightness [127]. Park and Takezoe fabricated top-gate-type OLET with organic multilayers in 2004, Fig. 1.27(a, b) [128]. They observed the luminance-voltage (L – V) characteristics of the OLET for different cathode-gate voltages as shown in Fig. 1.27(c).



(a) (b) (c)

Fig. 1.27. (a) Structure of the OLET; (b) Image of the OLET; (c) *L–V* curves of the OLET. Reprinted from B. Park and H. Takezoe, *Applied Physics Letters*, Vol. 85, 2004, 1280, with the permission of AIP Publishing.

The spin-off company of the University of Florida, Mattrix Technologies (previously nVerPix), introduced AMOLET based mono-colour (green) 320×240 2.5" display in

2016. Their solution is based on Carbon Nanotube Vertical OLET (CN-VOLET) reported in 2011 [129-132]. The AMOLET display consists of a drive transistor, storage capacitor and OLED layers integrated into a single, vertically stacked organic light-emitting transistor, Fig. 1.28. In 2019, Mattrix Technologies announced that it had closed its Series A financing round, with $3 million in investment from Samsung Ventures and JSR Corporation [133]. Power efficiency, reliability, lifetime, and mobility show the potential of OLET technology as suitable to flexible and low-cost active-matrix display. The potential of AMOLET technology is compatibility with a flexible sheet and low-cost manufacturing.

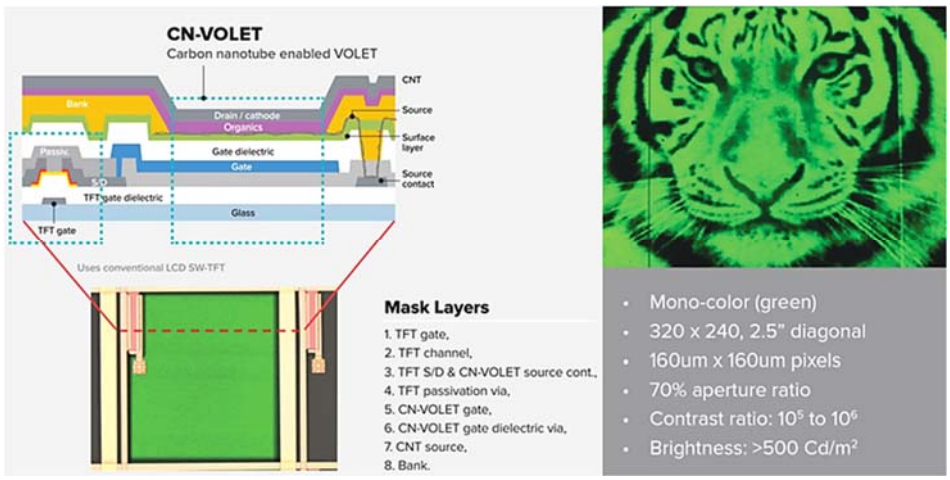


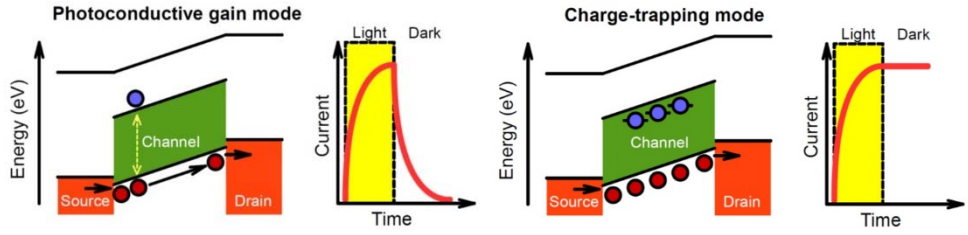
Fig. 1.28. Structures of CN-VOLET (Carbon nanotube enabled VOLET) and AMOLET based mono-colour (green) 320×240 2.5" display. Mattrix Technologies, 2021, https://www.mattrixtech.com/mattrix-technology.

1.3.5.4. Sensors

The OFET devices can be applied for other sensors such as temperature [134], pressure [135], gas [136], or light [137]. Especially photosensitive application of OFET devices attracts a lot of attention. Organic phototransistors typically exhibit higher responsivity than photodiodes because the current generated by photons is amplified by gate voltage modulation without increasing noise.

Although organic phototransistors based on organic polymers or small molecules have been reported already, their photoresponsivity was not enough for commercialization in comparison with inorganic counterparts. Hence, widely available materials for the fabrication of high-performance phototransistors are acutely needed in order to further the practical applications of organic optoelectronic devices. Possible routes include the incorporation of secondary materials such as quantum dots (*i.e.* semiconducting nanoparticles), graphene, and organic dye molecules in the base films as light absorbers or charge transport material. The additives can be mixed with an active layer (organic semiconductor) or with a gate insulator, depending on the fabrication technology.

Phototransistors can operate as a photoconductor as shown in Fig. 1.29 (a) for a *p*-type device (hole transporting). The transverse field created by the gate electrode assists the spatial segregation of photogenerated electron-hole pairs. However, since both source and drain contacts are hole-selective, the photogenerated electron stays in the channel while the photogenerated hole is extracted at the drain. The accumulation of electrons in the channel results in a shift in threshold voltage, causing more holes to be injected in order to compensate for the negative charge of electrons. New holes will be injected into the channel at the source electrode until a recombination event occurs between an injected hole and the photogenerated electron. If the transit time of a hole across the device (τ_{tr}) is less than the lifetime of the electron (τ_{life}), then multiple holes can be injected into the channel of the phototransistor for a single photogenerated electron–hole pair. This phenomenon, known as photoconductive gain G, can result in EQEs well over 100 % since $G = \tau_{\mathrm{life}}/\tau_{\mathrm{tr}}$. The response time of phototransistors in the photoconductive regime is usually limited by the lifetime of the minority carrier and not the comparatively fast transit time of the majority carrier. Consequently, devices that exhibit high photoconductive gain cannot operate as quickly as a photodiode with the same transit time. Nevertheless, organic phototransistors operating as photoconductor are sensitive photodetecting devices suitable for image sensors. Recently it has been achieved on benzothiophene-based (C8-BTBT) OFET photoconductive gain more than 10^7 under weak UV light exposure [138], making organic phototransistors as sensitive as a photomultiplier tube (PMT), but with a driving voltage of tens of times lower than that of PMTs.



(a) (b)

Fig. 1.29. (a) Hole (red) and electron (blue) movement in a hole-transporting phototransistor with photoconductive gain and the dynamic response shown to the right; (b) Charge carrier movement in the same phototransistor but operating in a long-term charge-trapping regime and the dynamic response shown to the right.

Phototransistors can also operate in a charge-trapping regime in which photogenerated electrons (in a hole-transporting device) become lodged in deep trap states in the channel of the device, as shown in Fig. 1.29 (b). This trapping also results in a shift in the threshold voltage of the phototransistor during normal transistor bias sweeps, even after the illumination has stopped. The lifetime of these trap states may even be as long as days. These electrons can be de-trapped through a large gate bias, effectively resetting the phototransistor. Hence, organic phototransistors operating in charge-trapping mode with exceptionally long trap state lifetimes are sometimes referred to as non-volatile optical

memory devices. It should be noted here that optically switchable molecules can also be used for memory devices, although there is a change of the conductivity due to the increase/decrease of effective mobility rather than the free carrier concentration.

FET-based gas sensors were demonstrated as early as 1975 by Lundstrom [139]. In its simplest form, a FET consists of two electrodes (the source and the drain), connected by a semiconductor sensing layer as the channel, and a gate electrode located typically at the back of the substrate. When a drain-source voltage is applied, a current passes through the channel region, whose charge carriers can be modulated by applying a gate voltage. This provides additional means to control the current response in the sensing layer upon interacting with a gas. The signal can be simple, the change in the output current, or it can be more sophisticated parameter such as the threshold voltage or subthreshold swing. Since the organic transistors usually exhibit an on/off ratio in the range from 10^6 up to 10^8, they can be applied as extremely sensitive sensing devices. As a result, organic phototransistors can be employed for light-induced switches (memories), light-triggered amplification, detection circuits, as well as highly sensitive image sensors. Recently, photoresponsive OFETs have also been exploited to design different logic circuits [140] with the advantage of having input signal either purely optical or a combination of electrical and optical.

The OFET-based gas sensor is working at room temperature. It can be sensitive to oxidative gases (such as NO_2, NO, O_2, Cl_2) and reductive gasses (NH_3, H_2S, CO, H_2) [141]. The organic semiconductors with *p*-type conductivity (hole-dominated transport) are the majority applied in organic semiconductor gas sensor. For this class of semiconductor, exposure to oxide gases will normally increase the conductivity. In contrast, exposure to reductive gases will yield a reverse response. In the last decades, numerous *p*-type organic molecules were employed in gas sensors, including phthalocyanines (*e.g*. CuPc), pentacene and its derivative TIPS-pentacene, thiophene and derivatives (*e.g*. P3HT), as well as other organic semiconductors. Especially photosensitive application of OFET devices attracts a lot of attention. Organic phototransistors typically exhibit higher responsivity than photodiodes because the current generated by photons is amplified by gate voltage modulation without increasing noise.

1.4. Organic Light-Emitting Diode (OLED)

1.4.1. Introduction

Since the first introduction of an organic light-emitting diode (OLED) in 1987 by Eastman Kodak [4, 142], OLED technology has constantly improved till now as illustrated in Fig. 1.30. First OLED devices have been based on small molecules and exhibited low efficiency. However, already in 1990, the Cavendish Laboratory at Cambridge University reported a polymer OLED paper in Nature [143]. Surprisingly, TDK company demonstrated of first active-matrix OLED (AMOLED) display just a few years later, in 1996 [144]. Even though AMOLED displays were introduced very early, the first

commercial OLED devices used the passive matrix (PMOLED) driven display in the car audio system by Pioneer in 1996/1997, Fig. 1.31 (a) [145]. Later, in 2003, Eastman Kodak company implemented a 2.2″ AMOLED display with a resolution of 512×218 pixels to the digital camera, Fig. 1.31 (b) [144]. It should be noted here that even though the polymer-based OLEDs were reported in 1990, commercial devices were introduced to the market much later, in 2002, by Philips [146-147]. Till now, we discussed small displays only. The OLED television was a great challenge and beyond the capabilities of early-stage technology. The pioneer in the field of OLED televisions was the Japanese company Sony that released the world's first 11″ and 3 mm thin OLED TV (XEL1) in 2007 [148]. It was just a beginning of a long and successful journey of OLED TVs. It should be mentioned here that Lumiotec developed the first commercial OLED panels for lighting applications in 2011 [148]. The flexible and bendable application have been envisioned from the early beginning, but the complex fabrication technology required further optimization. The first commercially curved 5.7″ Full HD super flexible AMOLED was demonstrated in Samsung Galaxy Round in 2013 [149]. A few years later, in 2015, the first bendable LG TV panel was shown [149]. However, it took the next five years, in 2020, to introduce the world's first rollable 65″ OLED TV by LG Electronics, Fig. 1.31(c) [150]. Today, the professional and lay public focuses on flexible smartphones of brands such as Samsung (Galaxy Fold), and Huawei (Mate X), Royale (FlexPai), as well as the foldable notebook of Lenovo and Intel (ThinkPad X1 Fold), depicted in Fig. 1.31(d) [151]. In addition, optical transparency had been offered for specific applications such as smart windows but with no commercial application. Only recently, in 2019, LG display started mass production of 55″ Full-HD transparent OLED panels.

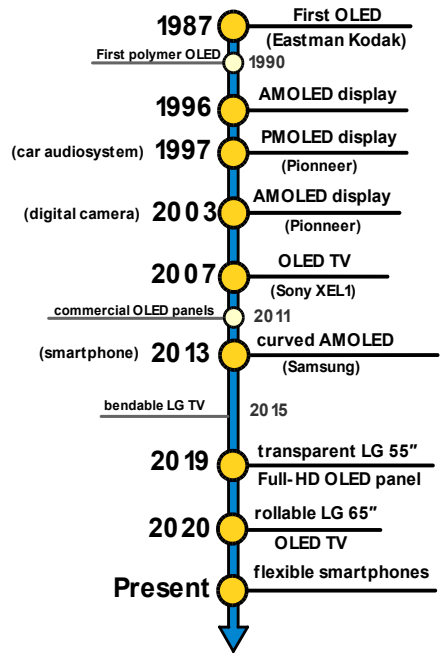


Fig. 1.30. The timeline of OLED evolution.

Fig. 1.31. Photographies of selected OLED commercial applications: (a) Car audio system by Pioneer; (b) Kodak digital camera LS633; (c) Rollable 65″ OLED TV by LG Electronics, and (d) Lenovo notebook ThinkPad X1 Fold.

1.4.2. What is an OLED?

The OLED device is typically a multilayer device that consists of organic layers sandwiched between two electrodes where at least one electrode is semi-transparent at the emission wavelength. Application of the voltage induces both electrons and holes injection into the organic layers. The charges migrate across the device and form an exciton in the emissive layer. The electroluminescence is observed when these excitons relax radiatively to the ground state. Proper selection of electrodes and organic materials, as well as the design of the energy band diagram, play a crucial role in achieving high-efficient OLED devices.

1.4.3. Structures and Materials

In recent years, a lot of research has been performed with the aim to create the most efficiently materials, structures and devices. The OLED device consists of organic layer(s) sandwiched between two electrodes where at least one of them must be transparent at the emission wavelength. Even though the OLED principle is very straightforward, there are many requirements to achieve highly efficient electroluminescence. The organic layer where the radiative recombination takes place should have ambipolar nature. However, the efficient and balanced supply of both electrons and holes requires additional organic layers. The very first devices had two organic layers where one layer had unipolar nature, whereas the second layer, the emissive layer, was ambipolar [4]. In other words, one layer served as a hole transport layer, while the other one served as an electron transport layer

and emissive layer simultaneously. Note that ohmic contacts are required for smooth charge injection and suppression of contact-limited conditions. It should be noted here that the energy difference between the work function of the cathode electrode and the LUMO energy level of the organic layer represents the electron injection barrier. In the same way, the energy difference between the work function of the anode and the HOMO energy level stands for the hole injection barrier. The hole injection (or electron injection) layers are applied to suppress the injection barrier. Suppose the LUMO energy level of the electron injection layer is designed in between the cathode work function and the LUMO energy level of the electron transport layer. In that case, the energy cascade is formed, and the barrier is suppressed. This design provides sufficient charge injection and transport across the device. As a result, the OLED device with high efficiency requires complex and sophisticated energy band diagram design, as illustrated in Fig. 1.32.

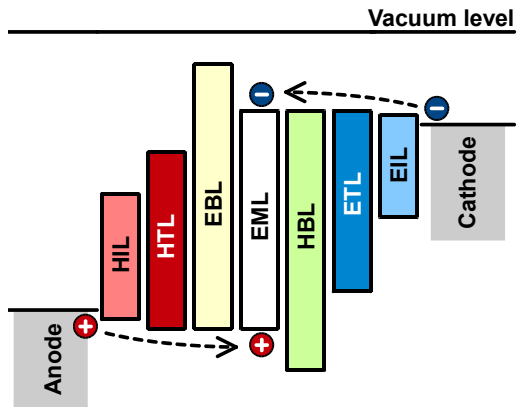


Fig. 1.32. The energy band diagram of the complex OLED device.

Anode – The most commonly used material for this layer is indium tin oxide (ITO), is the transparent conductive oxide. The great advantage of ITO is the optical transparency, high conductivity, suitable work function of about 5 eV, and uncomplicated patterning. On the other hand, it requires vacuum-based fabrication technologies such as sputtering for thin-film deposition; hence, the low-cost and large-area fabrication method is still needed.

HIL – The main purpose of the hole injection layer is to decrease the energy barrier between the anode electrode and HTL. That means that it greatly influences increases of charge injection to interface and finally improves the devices' energy efficiency. In an ideal case, the HOMO energy level of HIL should be in between the work function of the anode and the HOMO energy level of HTL. The material suitable for HIL usually does not exhibit high mobility; therefore, the layer thickness is designed in few nanometers only.

HTL – Hole transport layer provides charge transport into the emissive layer. There is a huge family of suitable materials used for this purpose. The typical representative is N, N'-Bis(naphthalen-1-yl)-N,N'-bis(phenyl)-2,2'-dimethylbenzidine (NPD), see Fig. 1.33.

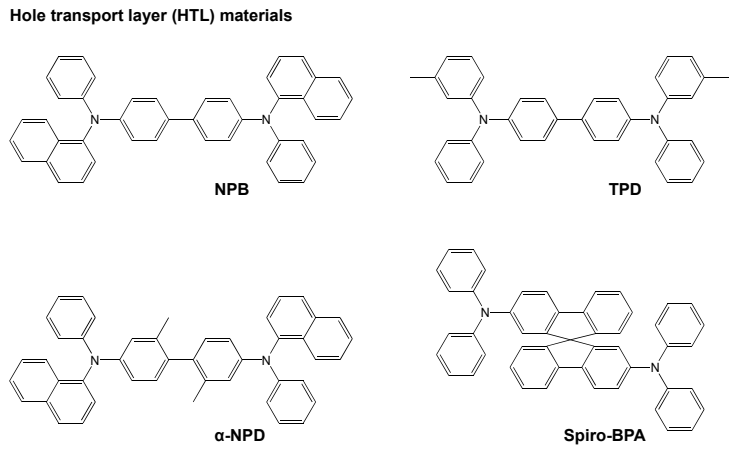


Fig. 1.33. The molecular structures of selected typical materials for hole transport layer (HTL): N, N'-Bis(naphthalen-1-yl)-N,N'-bis(phenyl)-benzidine (NPB), N, N'-Bis(3-methylphenyl)-N,N'-bis(phenyl)-benzidine (TPD), N, N'-Bis(naphthalen-1-yl)-N,N'-bis(phenyl)-2,2'-dimethylbenzidine (α-NPD), and 2,2'-Bis(N,N-di-phenyl-amino)-9,9-spirobifluorene (Spiro-BPA).

ETL – Electron transport layer helps to transport electrons into the emissive layer. Some materials, such as 4,7-Diphenyl-1,10-phenanthroline (Bphen) shown in Fig. 1.34, exhibit "exciton complex" (exciplex) formation. In other words, the exciton is formed at the interface by a hole in one material and an electron from another material. Exciplex formation provides lower efficiency of OLED device; however, it offers emission with a wavelength corresponding to the energy difference between HOMO energy level of *p*-type material and LUMO energy level of *n*-type material.

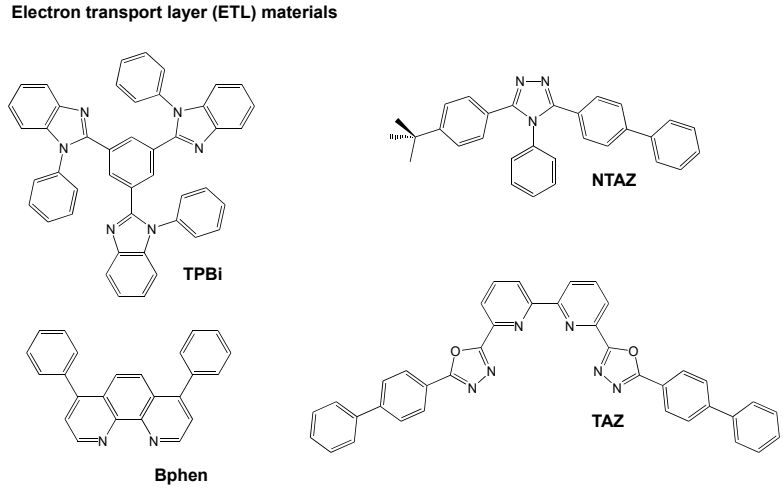


Fig. 1.34. The molecular structures of selected typical materials for electron transport layer (ETL): 2,2',2" -(1,3,5-Benzinetriyl)-tris(1-phenyl-1-H-benzimidazole) (TPBi), 4,7-Diphenyl-1,10-phenanthroline (Bphen), 4-(Naphthalen-1-yl)-3,5-diphenyl-4H-1,2,4-triazole (NTAZ), and 3-(4-Biphenyl)-4-phenyl-5-tert-butylphenyl-1,2,4-triazole (TAZ).

EML – The material for the emissive layer should have ambipolar nature and high recombination efficiency. Note that in many cases, this layer is combined with an ETL. The typical representative of the emissive layer is Tris(8-hydroxyquinolinato)aluminium (Alq3).

EIL – Electron injection layer decreases the energy barrier between the cathode and ETL. Interestingly, the most suitable materials are low-work-function inorganic compounds such as Lithium fluoride (LiF) or Cesium carbonate (Cs_2CO_3), see Fig. 1.35. Since these materials have extremely low mobility and behave such as insulators, the thickness of only a few nanometers is required. The very thin and discontinuous layer provides a modification of the interface's effective work function without suppressing the current conduction.

EBL/HBL – The OLED structure may also contain additional electron- and/ or hole-blocking layers. The role of the blocking layers is to force the charge carriers to recombine in the emission layer. The HOMO energy level of HBL should be greatly deeper than the HOMO energy level of EML to provide a high energy barrier and charge accumulation in EML. On the other hand, the HBL must have a LUMO level comparable with ETL to avoid electron suppression. The typical thicknesses of these layers are about 10 nm.

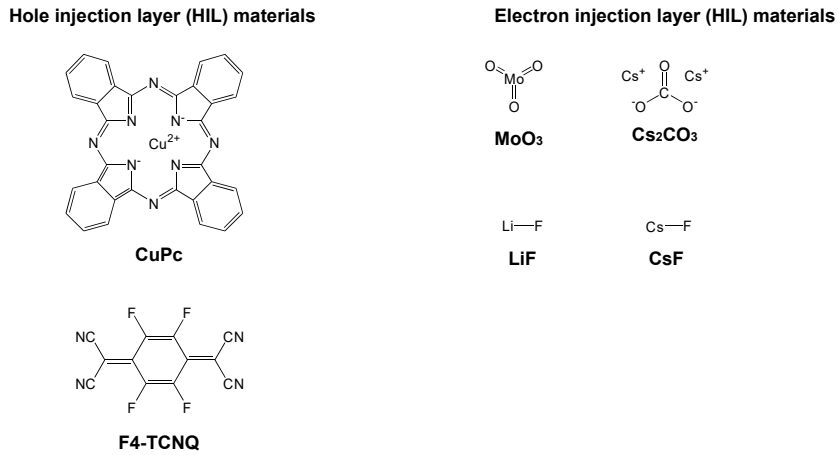


Fig. 1.35. The molecular structures of selected typical materials for hole injection layer (HIL) or electron injection layer (EIL): Copper phthalocyanine (CuPc), 2,3,5,6-Tetrafluoro-7,7,8,8,-tetracyano-quinodimethane (F4-TCNQ), molybdenum trioxide (MoO_3), Cesium carbonate (Cs_2CO_3), Lithium floride (LiF), Cesium floride (CsF).

1.4.4. Applications

1.4.4.1. OLED Displays

The main applications of OLEDs are the displays for smartphones, wearables, and TVs. An OLED display consists of four parts: (i) Substrate – the material that supports the

OLED display; (ii) Backplane - the electronics that drive the OLED display; (iii) Organic layers – organic materials placed between a cathode and an anode; (iv) Encapsulation – a final barrier preventing negative effects of the ambient environment. There are two fundamental types of OLED displays based on the control, AMOLED (Active-Matrix OLED) and PMOLED (Passive-Matrix OLED). Differents between PMOLED and AMOLED display is that PMOLED is driven sequentially, one line at a time, and AMOLED display is driven by a thin-film transistor (TFT) array. That means that PMOLED is cheaper and easier to fabricate, and AMOLED display is more expensive but with high-resolution for large-area devices (smartphone or TVs).

OLED TVs

As stated above, Sony company introduced the world's first OLED TV (XEL1) in 2007 [148]. Even though Sony was a pioneer, it did not continue in OLED technology. Hence, LG and Samsung started selling curved and flat OLED TVs in 2013 [144]. Surprisingly, Samsung later withdrew from the OLED TVs market even though the smartphone display fabrication was very successful. Today, LG Display is the only commercially OLED TV panels producers. OLED display from LG uses an oxide-TFT backplane based on indium gallium zinc oxide (IGZO) and WRGB front plane. The utilization of WRGB offers a relatively high production yield and low fabrication costs; however, it causes a shorter lifetime of devices and lower efficiency in comparison with direct emission OLED displays, *i.e.* RGB. As mentioned above, LG Electronics also introduced the world's first rollable 65" OLED TV in 2020 [150]. There are other OLED TVs producers, for example, BOE and China-Star (CSoT). In 2019 BOE demonstrated an 8K 55" OLED TV with a coplanar Oxide TFT backplane and top-emissive structure, produced using an inkjet printing technique. The inkjet printing technology is very promising for OLED TV production. It has been reported in 2021 that CSoT aims to introduce printed OLED TVs in 2024. The total investments for the new fab are estimated as high as 6.8 billion USD [112].

Smartphones, laptops, monitors and wearables

Since 2009, the AMOLED display market had grown from about $500 million to around $30 billion in 2020. The biggest producer of AMOLED display designed for smartphones and wearables is Samsung Display. Currently, all major companies of the smartphone industry have used AMOLEDs in their premium and mid-range phones. Besides Samsung, there are several other producers of AMOLED display, for example, LG Display, BOE, Truly, Visionox and Everdisplay. The current trend in the OLED industry is to focus on flexible and foldable displays. The first foldable smartphone Samsung Galaxy Fold, with a 7.3″ Infinity Flex AMOLED display, was introduced to the market in 2019 [151]. Other applications are tablets, laptop displays and OLED monitors. In 2019-2021, Samsung, Everdisplay and BOE began producing AMOLEDs display for the laptop market. In 2020 Lenovo introduced the first foldable laptop, the ThinkPad X1 Fold [151]. In the laptop market, Asus and Eizo have adopted a 4K display from Japan's JOLED company to create premium monitors. Smartwatches and fitness bands are another interesting application of OLED technology. Currently, there are several wearables

product used AMOLED display, for example, Samsung Galaxy Watch 3, Galaxy Fit 2, Apple Watch Series 6, Xiaomi Mi Watch, Huawei Band 3 pro, or Vivo watch, *etc*. [112].

1.4.4.2. OLED Lighting

OSRAM company introduced the first OLED lamp in 2008 [152]. Only one year later, in 2009, Philips started to offer OLED panels under the Lumiblade brand [153]. The most significant advantage of OLED lights compared to conventional lights is that they can be flexible or transparent. This means that OLED technology offers more application options compared to LED or CFL (Compact fluorescent lamp) lights. In the future, we will be able to meet with OLED lights placed on a window or ceiling. However, today the biggest problem of OLEDs is still the high price and therefore, the big challenge is to reducing production costs with new manufacturing technologies and processes.

1.4.4.3. Automotive

The use of OLED in the automotive industry can be divided into two parts OLED car lighting and dashboard display. The first commercial OLED device in automotive was PMOLED display in-car audio system by Pioneer in 1996/1997 [145]. Today, OLED dashboard displays are used almost exclusively in premium cars such as the Cadilac Escalade, Audi e-tron or Mercedes S-Class. Transparent OLEDs are also predicted to be used for head-up displays (HUDs), which are not yet commercially deployed. The first serially produced car with OLED tail lights made by OSRAM was Audi TT RS Coupe in 2016. Since then, OLED taillights have been used in several premium models, for example, Mercedes-Benz S-Class 2018 (designed by LG Display) or Audi Q5/SQ5 2021 (designed by Hella). Nevertheless, it will take several more years before OLED lighting will be used in more affordable cars for the general public [112].

1.5. Organic Solar Cells

The generation of excess charge carriers causing additional voltage is known as the photovoltaic effect. In details, the photovoltaic effect takes place in semiconductor materials where illumination by photons with an energy greater than the energy gap excites electrons from the valance band to the conduction band. Excess charges are known as photogenerated charge carriers. These photogenerated electrons and holes need to be extracted by appropriate electrodes. The electronic devices that exhibit photovoltaic effect are denoted as solar cells.

There is a long journey of the solar cells from the origin up to nowadays. Crystalline and polycrystalline silicon-based solar cells are known as the first generation of solar cells. Since the high-cost technology was used to fabricate the crystalline solar cells, the second generation was focused on cos optimisation using amorphous silicon, copper indium gallium diselenide (CIGS), and cadmium telluride (CdTe). Since these materials have been deposited only in a thin layer on the solid substrate, it is denoted as the thin-film technology. The third generation of solar cells includes complex solar cells and emerging

photovoltaic technologies like dye-sensitised solar cells or organic solar cells. Here, the organic solar cells are the solar cells using the organic semiconductors in the active layer. Even though the power conversion efficiency was lower than 1 % at the early stage [3, 154], nowadays, it is more than 13 %, see Fig. 1.36.

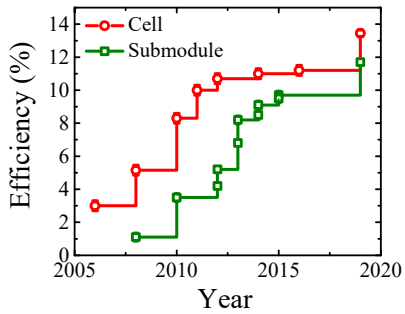


Fig. 1.36. The evolution of overall efficiency of organic solar cells as well as submodules [155-161].

Organic solar cells are devices with bipolar nature, it is required to conduct both electrons and holes. Hence, the organic solar cell architecture must reflect the requirement on charge generation, separation, and extraction. As a result, there is a need for a precise design of active organic layer as well as charge extraction electrodes. Since the organic solar cells are thin-film devices deposited on a solid substrate, they have a sandwich structure, and one electrode must be transparent for the incident light. Even though there is no conductive and transparent materials, there are specific metal oxides that offer a balance between the conductivity and the optical transparency; hence, the name transparent conductive oxides (TCOs) is used for this family of materials. In most cases, the indium tin oxide (ITO) is used as a transparent electrode since it offers plausible figure of Merit, FoM, that is evaluated as a ratio of optical transmittance T and the sheet resistance R_{sq} as follows

$$FoM = \frac{T^{10}}{R_{\mathrm{sq}}} \tag{1.15}$$

where $R_{\mathrm{sq}} = \rho/d$ is the ratio of the resistivity ρ and the film thickness d. The sheet resistance is commonly used to obtain a film-area independent variable with unit Ω/sq, where sq stands for 'square' abbreviation. Since the work function of ITO of about 4.5 eV is mostly suitable for hole ohmic contact for most organic semiconductors, the architecture based on TCO as a hole extraction electrode is denoted as the normal geometry. On the other hand, if the TCO is used as an electron extraction electrode, it is known as inverted geometry of organic solar cells, as illustrated in Fig. 1.37.

In the normal geometry, it is common to apply hole extraction layer on the transparent and (*i.e.* ITO) to suppress the surface roughness as well as improve the effective work function of the anode. The common materials for the hole extraction layer are MoO_3 [162, 163], V_2O_5 [163], NiO [164], W_2S [165]. In the cases of conductive organic polymer

poly(3,4-ethylenedioxylenethiophene):poly(styrenesulphonic acid) (PEDOT:PSS), the organic hole extraction layer can even replace the TCO electrode [166]. On the other hand, the electrode extraction part should be made of low work function materials. The electron extraction layer is mostly of LiF or Cs_2CO_3, whereas the metal cathode materials are low work function metals like Ca (2.9 eV), Al (4.1-4.3 eV), Mg (3.66 eV), Sm (2.7 eV), or Ag (4.5-4.7 eV) [167].

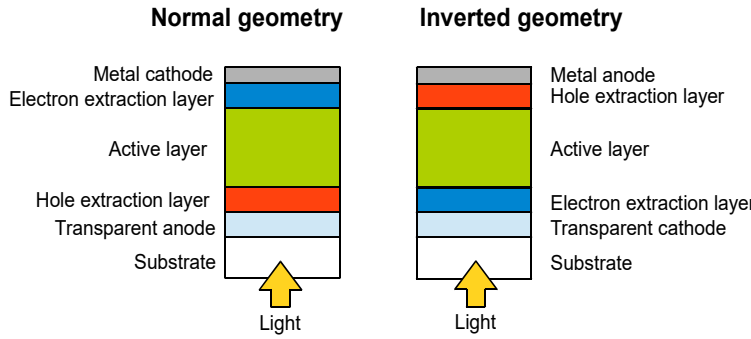


Fig. 1.37. The normal and inverted geometry of organic solar cells.

The inverted solar cells require a more sophisticated device design since the ITO electrode is not suitable for electron extraction. The ITO surface must be modified by the electron extraction layer that must be optically transparent and exhibit low work function. The most common materials are ZnO or TiO_2 [168]. Compared with conventional organic solar cells in normal geometry, inverted-type geometry exhibits better long-term ambient stability by avoiding the need for the hygroscopic hole-transporting PEDOT:PSS and corrosive low-work-function metal electrode.

Till now, we did not pay attention to the active organic layer even though it is the most crucial in the organic solar cell. In contrast to the inorganic solar cell, the photon absorption generates the excited state of the electron-hole pair, the exciton. It should be noted that the weakly bound charge-transfer excitons display a lower correlation with the photocurrent, while the strongly bound Frenkel excitons are crucial inorganic solar cells. Since the binding energy of Frenkel exciton is about 0.5 eV, the charges cannot be separated by the built-in electric field because their binding energy is too high. Tang, in 1986, proposed a two-layer heterostructure to split the exciton and separate the charges [3]. However, since the excitons have no charge, their migration is ruled by diffusion only. Due to the extremely short lifetime, the excitons are capable to diffuse on a very short distance in a range of few nanometers. In other words, if the excitons that not reach the interface in a period shorter than the lifetime, the charges recombine, and the exciton decays. Hence, for efficient energy conversion, all of the generated excitons should be able to diffuse to the donor-acceptor interface during their lifetime. The double-layer system is limited by the diffusion length of excitons; therefore, there was a need for a donor-acceptor interface distributed across the device, the bulk heterojunction device, see Fig. 1.38.

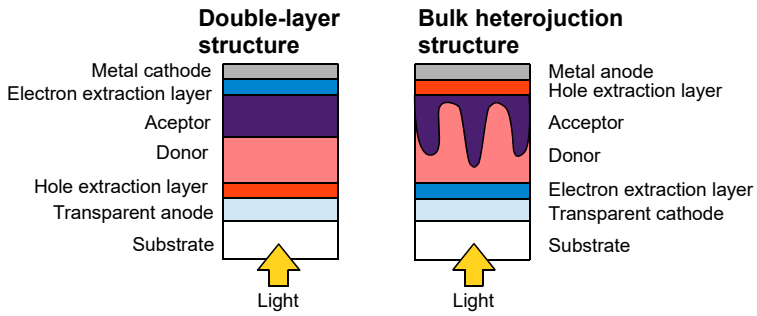


Fig. 1.38. The double-layer and the bulk heterojunction device structure.

In details, the requirements on material properties and device structure can be summarised as follows [169]:

- *Nanoscale phase separation*: the donor-acceptor domain size should be comparable with exciton diffusion length size to allow exciton to reach the interface before it decays;
- *Energy levels alignment*: the energy difference at the donor-acceptor interface must be at least 0.3 eV to dissociate the exciton;
- *High mobilities*: the effective mobilities of electrons and holes must be high enough to prevent the space-charge that suppresses extraction electric field. In addition, the charge transport to the electrode must be fast enough to avoid charge recombination;
- *Optical properties*: absorption spectrum of donor-acceptor materials should match the solar spectrum and should have a high extinction coefficient.

Even though energy band structure, optical and electronic properties are pure material properties, the nanoscale phase separation is a crucial condition on device structure. To satisfy the exciton dissociation efficiency, the bulk heterojunctions are required since they consist of a highly folded architecture such that all excitons are formed close to the heterojunction. The common fabrication of bulk heterojunction is based on spin-casting of donor and acceptor from a common solvent. The phase separation of organic materials at the nanoscale level provide the required domains of donors and acceptors.

Note that most of the inorganic semiconductors exhibit electron mobility larger than the hole mobility. In contrast, that organic semiconductors with *n*-type conductivity are less common and have lower mobility than the materials with *p*-type conductivity. As a result, *n*-type organic semiconductors (*i.e.* acceptors) were a bottleneck of the early-stage design of organic solar cells. After the discovery of the photoinduced electron transfer from a conducting polymer to fullerene (C_{60}) [170], the fullerene molecules have been applied for the organic solar cells [171]. However, the high performance organic solar cells require a bulk-heterojunction structure fabricated by the solution-based technologies and both acceptor and donor should be soluble in a common solvent. Since fullerene is insoluble material, the soluble derivative 6,6-phenyl-C61-butyric acid methyl ester (PCBM) has

been introduced, Fig. 1.39 [172]. This acceptor PCBM enabled new possibilities, and the power conversion efficiency raised from 2.9 % up to 5 % in one decade [172, 173].

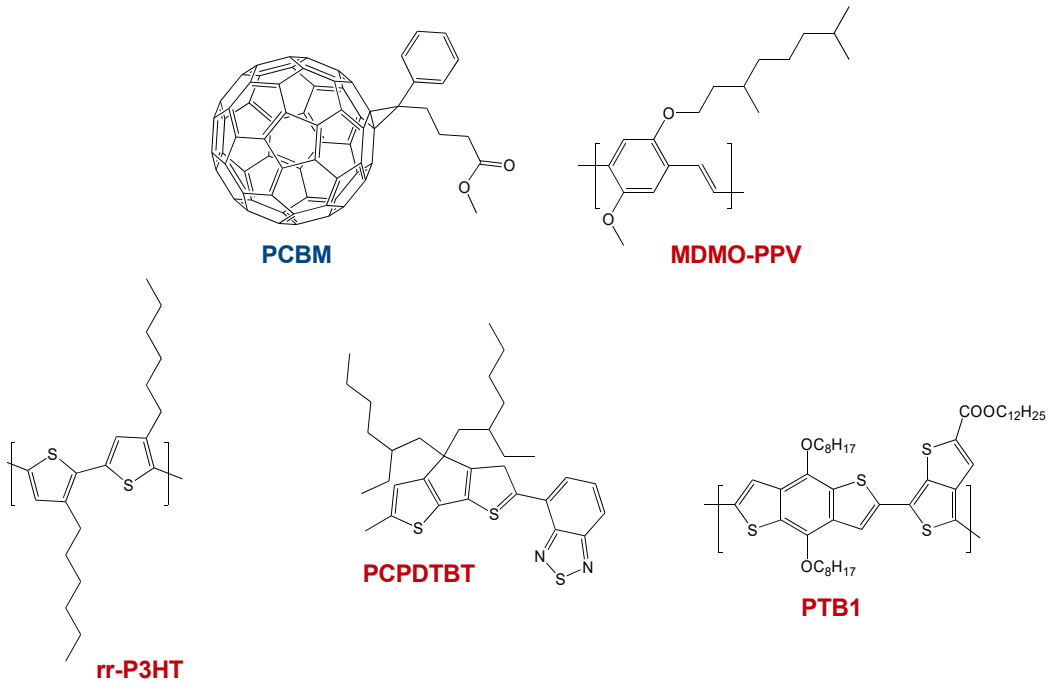


Fig. 1.39. Molecular structure of selected popular organic semiconductors used for organic solar cells. PCBM stands for the most common fullerene-based acceptor, whereas MDMO-PPV, rr-P3HT, PCPDTBT and PTB are typical representatives of donors.

The open-circuit voltage V_{oc} is a very important issue; however, it is so compelx that up to now there is no precise explanation for its origin. According to the Shockley't theory, the solar cell behaves as a diode with exponential growth of the current density J and follows relation

$$J = J_0\left(\exp\left(\frac{eV}{n\mathrm{k}T}\right)+1\right) - J_{\mathrm{ph}}, \tag{1.16}$$

where V is the applied voltage, $\mathrm{k}T/e$ is the thermal voltage, n is the ideality factor, J_0 is the current density in reverse voltage, and J_{ph} is the photocurrent. The Eq. (1.16) leads to the typical characteristics illustrated in Fig. 1.40. Note that current density at zero voltage stands for the short-circuit current density J_{sc}, whereas the voltage at zero current density is recognised as the open-circuit voltage V_{oc}. The output power is defined as the product of the current density and the voltage and reaches the maximum values for specific values as follows

$$P_{\mathrm{max}} = J_{\mathrm{max}}V_{\mathrm{max}} = J_{\mathrm{sc}}V_{\mathrm{oc}}FF, \tag{1.17}$$

where we can define a fill-factor FF as a ratio of short-circuit current density, open-circuit voltage, and the maximum power conditions. The overall efficiency is defined as a ratio of incident light power P_{solar} and the output power P_{max}.

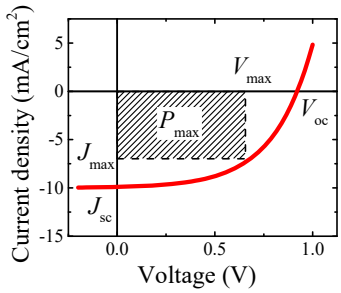


Fig. 1.40. Typical solar cell current density-voltage characteristics.

Hence, the open-circuit voltage can be evaluated from Eq. (1.16) as

$$V_{\mathrm{oc}} = \frac{n\mathrm{k}T}{e}\ln\left(\frac{J_{\mathrm{ph}}}{J_0}+1\right) \tag{1.18}$$

Note that even though the Shockley model does not include any undelaying physics, the photocurrent and the reverse current can be expressed using the intrinsic and the excess carrier densities. For a silicon solar cell made on a *p*-type wafer with acceptor density N_{a}, the voltage depends on the *pn* junction [174] as follows

$$V_{\mathrm{oc}} = \frac{\mathrm{k}T}{e}\ln\left(\frac{\Delta n(N_{\mathrm{a}}+\Delta n)}{n_{\mathrm{i}}^2}+1\right), \tag{1.19}$$

where n_{i} is the intrinsic concentration, Δn and Δp are concentrations of excess electrons and holes, respectively. However, this approach is meaningless for organic semiconductors with zero doping level. In addition, there are additional effects such as open-circuit voltage dependence on illumination, temperature, active layer thickness, or electrode metals, as shown in Fig. 1.41.

Even though there is no common model, several models have been proposed to explaining the open-circuit voltage origin and behaviour. The light intensity dependence has been proposed by Koester *et al.* [176] and utilises a model based on conservation of quasi-Fermi levels across the device. Here the open-circuit voltage depends on the light illumination as

$$V_{\mathrm{oc}} = \frac{E_{\mathrm{gap}}}{e} - \frac{\mathrm{k}T}{e}\ln\left(\frac{(1-P)\gamma N_{\mathrm{c}}^2}{PG}\right), \tag{1.20}$$

where E_{gap} is the energy difference between the HOMO level of hole conductive semiconductor and the LUMO level of electron conductive semiconductor, G is the exciton generation rate, P is the exciton dissociation probability, γ is the Langevin

recombination constant, and N_c is the effective density of states. The model has been later simplified [177] for sufficient illumination as

$$V_{oc} = \frac{E_{gap}}{e} - 0.3 \text{ eV} \tag{1.21}$$

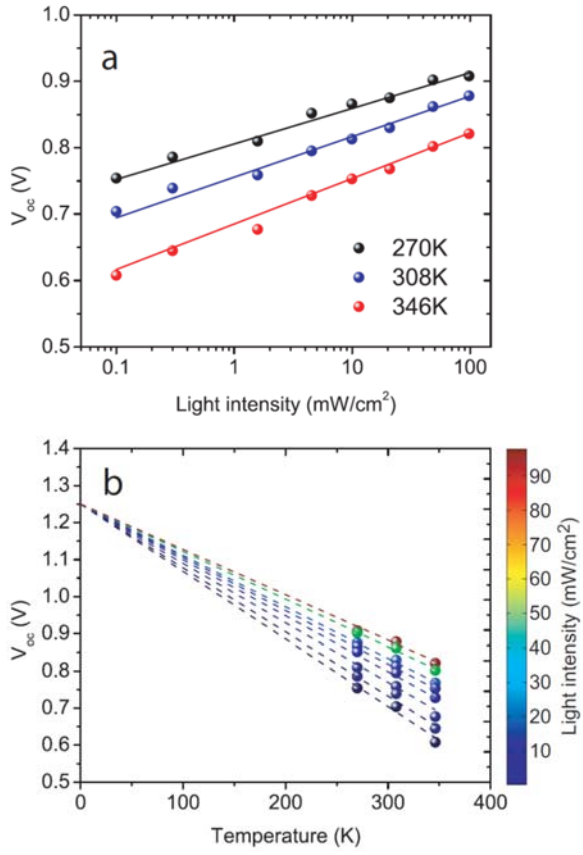


Fig. 1.41. (a) Logarithmic dependence of V_{oc} with incident light intensity with slope kT/e, cell temperature modulated; (b) Linear dependence of V_{oc} with temperature in a PCDTBT:$PC_{71}BM$ solar cell. Reprinted figure with permission from S. R. Cowan, A. Roy and A. J. Heeger, *Physical Review B: Condensed Matter and Material Physics*, Vol. 82, 2010, 245207. Copyright 2010 by the American Physical Society.

The concept proposed by Brabec *et al.* [178] used a model developed to explain the built-in potential at semiconductor/metal interfaces using the index of interface behaviour S [20]. The S is defined as the slope of a plot of the barrier potential V_b of a semiconductor/metal interface versus the work function of the metal, $eV_b = S(\phi_m - \phi_s) + C$, where ϕ_m and ϕ_s are work functions of metal and semiconductor, respectively, and C is constant representing the potential for Ohmic contacts. As a result, the model predicts the open-circuit voltage based on the reduction potential of acceptor molecules, $E_{red(a)}$, in the form

$$V_{\mathrm{oc}} = \left(A_{\mathrm{ox}} - S_1 E_{\mathrm{red(a)}}\right) - S_2\left(\phi_{\mathrm{m}} - E_{\mathrm{red(a)}}\right) + C, \quad (1.22)$$

where A_{ox} stands for all contributions from the positive electrode and S_1 and S_2 have a meaning of the quality factors for semiconductor/semiconductor and metal/semiconductor interface, respectively. This evaluation for a broad family of acceptors and selected metals showed that the variation in acceptor strength is greatly more significant than the dependence on the work function of the electrode. It has been denoted as the Fermi level pinning [179].

1.6. Conclusion Remarks

Organic electronics is still a new scientific discipline based on the application of organic semiconductors in electronic devices. Even though the fundamental principles of the charge transport phenomenon differ from the inorganic materials, specific electronics properties are very similar to silicon or other inorganic materials. This young research field is still experiencing rapid development of fabrication technologies, characterization techniques, and theoretical models. However, the precise characterization of material and device properties requires a deeper understanding of underlying physics as well as more accurate models of devices. Certain achievements have been already reached without real understanding, but further progress beyond the state-of-the-art cannot be made without insight. Organic electronics has strong interdisciplinary nature since it combines knowledge of physics, chemistry, and electronics. This combination of academic disciplines is often an origin of various misunderstandings between different research fields that makes progress slower than expected.

From the fabrication technology perspective, organic electronics go beyond the state-of-the-art and provide new possibilities for large-area and low-cost electronics fabrication. The tremendous abrupt progress in the OLED display applications or organic solar cells efficiencies depicts the evolution of the new science that fills the gap in the knowledge and brings new applications. Besides the already available applications, there are envisioned new ones such as memory devices for neuromorphic computing, photovoltaics working indoor or in the shade, sensors with molecular recognition, or transparent microdisplays for augmented reality.

Novel materials and technologies provide new challenges and open further questions. The variability and inhomogeneity of material electronic properties such as effective mobility force us to develop a new device structure or electronic circuit design to increase the device efficiency and fabrication yield. The fabrication technology enables lightweight, flexible systems with the possibility of device density increase by multiple layer stacking.

Even though the devices are not patterned at the nano-scale level, they are sensitive to molecular interaction and makes a breath-taking interface. It has been demonstrated that organic electronics sensors offer molecular recognition using DNA to detect cancer or other diseases. Since the organic molecules may exhibit a favourable interaction with other organic molecules, organic electronics devices are envisioned as a promising candidate for the “holy grail” of bioelectronics and biocompatible electronics capable of

communication with a living matter such as neurons. As a result, organic electronics is interdisciplinary and going beyond the horizon of standard electronics.

Organic semiconductors also represent a fascinating challenge for science and technology and require modification of general assumptions on semiconducting materials. They prove that the semiconducting nature does not belong to the doped semiconductors only, but it is a universal feature of dielectrics materials. Interestingly, it pointed out that we need to leave common ideas and take a step back to keep the general overview. The development of organic electronics is not only about fundamental science, but it has significant industrial applications. Nowadays is organic electronics present mostly in OLED displays, but it already aims for great and exciting applications such as healthcare, photovoltaics, sensors and low-power systems to improve the life quality of human society by enabling high-end devices for everyone.

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Chapter 2

Reconfigurable Conduction Mode in Bipolar Junction Transistor-based Architectures for Recyclability

Roberto Baca-Arroyo

2.1. Introduction

Today, the disturbing factor involved in climate change appears to be burning carbon-containing materials into industrial process, as in the silicon semiconductor industry where much larger quantities are put in the atmosphere as a waste product. In addition, due to the modern industrial revolution where each time people have reacted in acquire products planned by semiconductor technology, a lifestyle depended on uneven pattern of consumption has increased since 1950 which is not expecting to progress for the coming decades because it creates another worldwide issue known as electronic waste [1, 2].

To mitigate high-volume electronic waste produced each year during a manufacturing process or household hardware that in the past worked but now is out-of-date, today technological change coupled with political and economic realities must be rethinking into a sustainable industry, where emergent technologies related to sensing schemes for Internet-of-Things (IoT), wireless communication systems and electrical power usage will define our next lifestyle [3]. Such these innovative solutions must consider not only the circuit architecture but also other key feature as degrees of complexity in operation to satisfy technological standards. Such feature is known as reconfiguration which can be defined as the dynamic self-adjustment of the internal structure of a device during operation by external stimulus rather than fixed output-to-input relationship [4].

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For instance, it is feasible to enable states into a device dependent on carrier´s conduction phenomena, use of passive and active building blocks and reduced number of them. Fig. 2.1 illustrates the expected recyclability actions in a sustainable electronics' industry.

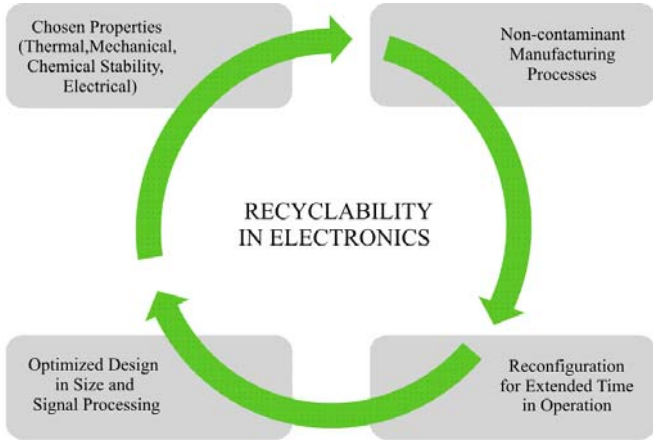

Fig. 2.1. Recyclability actions planned for functional devices fabrication in a sustainable industry.

For more than five decades, the Moore´s Law has described and predicted the shrinkage of transistors, but after of intense research efforts in solid-state device engineering only data processing-focused technology established on complementary metal-oxide-semiconductor (CMOS) transistors with reduced gate length to keep adequate connectivity between logic processor and memory has been created by package-level technology rather than architecture-level technology [5]. It means that when the silicon CMOS stops shrinking entirely, the semiconductor industry will become less efficient in the following years. Still, for more than a decade researchers have been exploring ways to produce monolithic integrated circuits using stressed transistor's silicon where them must be built atop one another allowing charge carriers to move at lower voltages to increase speed and power efficiency in computer architectures of multiple layers between the logic processor and data-storage devices, but these face limitations of how considerably power they can dissipate without increase the probability of failure as in the following cases. First, in the basic switch-inductor circuit for industrial applications must satisfy a compromise between high-duty cycle and low-duty cycle signal ratio to drive the switch to achieve steady power conduction parameters from full load to light load condition; hence, digital signal processors (DSPs) built by advanced CMOS technology, where high sampling rate to improve dynamic response of power devices in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) under huge stress are used to implement robust signal sequences algorithms [6, 7]. Second, thermal degradation and current-leakage problems during manufacture of silicon CMOS processors used as driver circuits enable unstable presence and absence of on-state and off-state pulses of high switching frequencies (> 100 kHz), making that power switches to operate critically due to the relatively poorer conduction (switching losses) and when

overdriven the switches to provide desired output current also temperature losses increase [8].

In recent years has been demonstrated that functionality of the solid-state ionic devices based on bipolar junction transistor (BJT) technology in comparison to that widely used field-effect transistor (FET) technology has significantly major impact for signals processing in electrochemical and biomedical applications [9, 10]. Recent advances in FET technologies have demonstrated flexibility to integrate digital systems, because it is typically easy to manufacture at relatively low temperatures, such as the upcoming technology based on 3D chips made of carbon nanotube field-effect transistors (CNFETs), where CNFETs can be built in multiple tiers much more easily than with silicon. But anomalous sensing signal changes required to generate relevant operating conditions due to their calibration dependence on surface-charge modulation make CNFETs do not well suitable [11, 12]. So, the use of bulk properties in BJT rather than surface effects in FET opens the possibility in reduction the switching losses as well as the electromagnetic interference (EMI) noise when pulse-based circuits operate at lower and medium frequencies (< 100 kHz).

Earlier configurations for square-wave pulse circuits used in television broadcasting, where cut-off and saturation modes to drive timing and synchronizing subsystems under extreme on-state/off-state cycles ratio during operation resulted in recurrent failure scenarios in the past decades [13]. But such those pulse-processing subsystems were the fundamentals for the beginning of CMOS technology-based digital television and signal conditioning circuitry based on boxcar sampling to help in reducing size and power consumption provided by modern integration techniques [14]. The latter is motivation to seek circuit architecture-level technology to operate under extended lifecycle at lower heat dissipation, and unstressed electrical conduction using soft conduction modes to perform reliable technologies for analysis of data sequences from a variety of sensing signals, which might be planned, for example when a continuous voltage adjusts each built-in device enabling its internal structure that constantly must will examine for reconfiguration incoming to determine the operating conditions into numerous signal-distribution paths using a reduced number of building blocks inside signal processing architectures.

2.2. Reconfigurable Conduction Mode

It is well known that the bipolar junction transistors (BJTs) were the key component to enable amplification and processing of electronic signals in circuits in the 1960s, 1970s and the mid-1980s. [15]. The BJT is a three-terminal device in which the electric current between the collector and emitter terminals is driven by bias current applied to the base.

The principle of operation in the BJT is modulation by mobile charge carries [16]. For example, BJT in n-p-n structure can be seen as two p-n junctions sharing a narrow base region, where both emitter and collector regions are n-doped, and the base region is p-doped. When the BJT is driven in common-emitter configuration as shown in Fig. 2.2, the base-emitter junction is forward biased, and the collector-emitter junction is reverse biased; then the BJT operates in active mode. As accumulation of minority charge carriers

at the base-emitter junction increases, this cause that the potential through the base-emitter junction to drop and collector current rise as a function of the bias voltage V_1, thus, once a small signal (commonly sinusoid) V_{IN} ($V_{IN} << 1$ V) is injected to the amplifier circuit, an out-phase sinusoid signal larger than the input signal result at the output V_{OUT}. But, if the signal V_{IN} increases above 1 V, signal V_{OUT} saturates, and the amplifier circuit behave like to an inverter circuit [17].

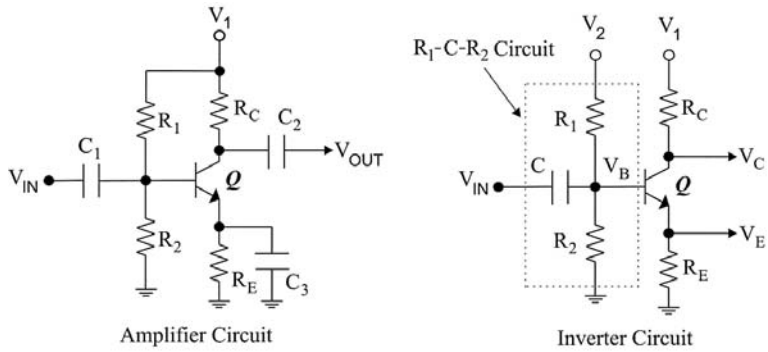

Fig. 2.2. Typical architecture of a BJT-based amplifier circuit and their modified version as inverter circuit.

To operate the amplifier circuit as an approximated inverter circuit, the signal V_{IN} as square-wave pulses must satisfy that $V_{IN} > 1$ V, also the coupling capacitor C_2 and bypass capacitor C_3 must be removed to observe operation in switching mode. In spite of using the amplifier circuit as inverter circuit as proposed in Fig. 2.2, it must operate at constant frequency to avoid a mixture of amplification and switching features. Therefore, it is advantageous here to understand how the forced switching mode in the BJT can be equivalent to the reconfigurable conduction when an external stimulus such as variable bias voltage V_2 can change their internal states. Thus, action of the internal states is revealed by the waveforms in Fig. 2.3.

An empirical description related to the operation of these states is given below:

Sate 1. A positive voltage V_{IN} is applied as a square-wave pulse during t_1, forward bias in the base-emitter junction of transistor Q occur by base current from V_2 through the resistive divider by R_1 and R_2, as well as by emitter resistor R_E. At the base of Q, the signal V_B is offset a certain positive voltage level and signal V_C forced at saturation mode, while a square-wave pulse reduced in amplitude occur in the signal V_E.

State 2. Zero voltage V_{IN} is applied as a square-wave pulse during t_2 and here is supposed that the capacitor C begins to be charged and transient reverse bias in the base-emitter junction occur as shown in signal V_B which is offset-up by resistive connection of R_1, R_2, and R_E depended on V_2. So, the collector-emitter junction of Q is forced to operate in unstable cut-off mode and signal V_C is offset with positive voltage level as a quasi-pulse with unstable on-state, while signal V_E is close to zero.

State 3. At the reference point (vertical dashed line in Fig. 2.3) a positive region of signal V_B during t_2 grows as a function of the voltage excursion and likewise base-emitter junction again becomes forward biased. Here, it is supposed that a discharge for the capacitor C begins and will ends steadily during t_1. Under this condition, signals V_C and V_E were driven in absence of input current.

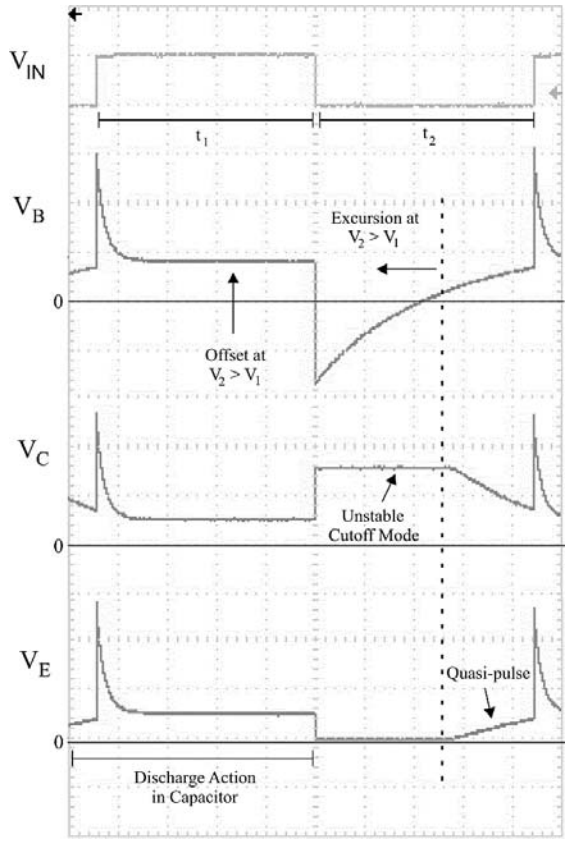

Fig. 2.3. Waveforms presented by the inverter circuit when it is operated in cut-off and saturation modes.

Observing the phenomenon previously described where unstable conduction mode as a function of the bias voltage V_2 and signals V_C and V_E was supposed as on-state and off-state logic levels; then, such that operating mode can be defined as a soft conduction mode based on dynamic operation of the R_1-C-R_2 circuit in Fig. 2.3 to be functionally architected in the following two cases of Fig. 2.4.

Case 1: Reconfigurable inverter circuit, where the resistor R_2 is inserted among resistor R_1 and base-emitter junction (diode) of the transistor Q. The resistor R is series connected at the collector region and bias voltage V_1, while that the emitter region is connected at zero (ground reference) to ensure the output pulse to have a rectangular waveform during off-sate interval.

Case 2: Reconfigurable non-inverter circuit, where the base-emitter junction (diode) of the transistor Q is inserted among resistor R_1 and resistor R_2. The collector region is series connected to the bias voltage V_1 and the output signal must be extracted from the resistor R_2 connected to zero (ground reference) to ensure a near rectangular waveform during operation.

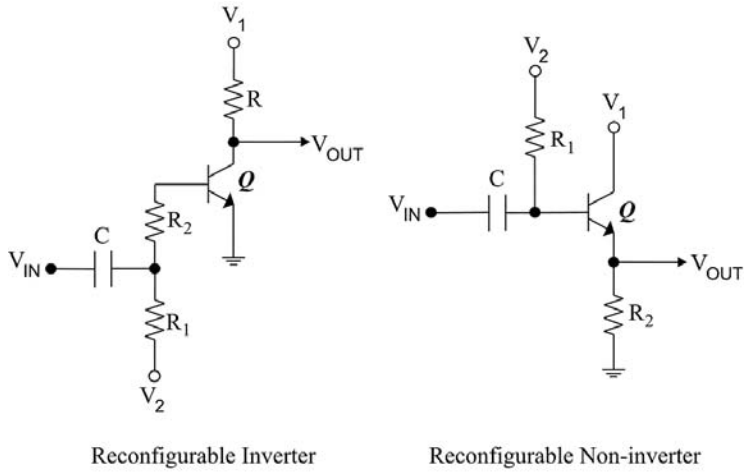

Fig. 2.4. Proposed circuit architectures to operate how reconfigurable inverter (case 1) and reconfigurable non-inverter (case 2).

2.2.1. Stability Analysis and Design Criteria

Considering the differential equations for the R_1-C-R_2 circuit of Fig. 2.2 which governs the soft operation mode in a reconfigurable scheme as a function of voltages V_1 and V_2 and currents in the circuits of Fig. 2.4, these can be described as

$$\frac{dI}{dt}+\left(\frac{1}{R_1C}\right)I=\left(\frac{1}{R_1}\right)\frac{dV_2}{dt}, \tag{2.1}$$

$$\frac{dV_2}{dt}=\left(R_1+R_2\right)\frac{dI_B}{dt}, \tag{2.2}$$

where I correspond to the capacitor current and I_B is the bias current in base region of Q.

As V_2 appears in both equations (2.1) and (2.2) and V_B is equal to the voltage resulted in the R_1-C-R_2 circuit, thus, solutions for I and I_B can be written as

$$\frac{R_1I}{V_2}=\exp\left(-\frac{t}{\tau}\right), \tag{2.3}$$

$$\left(\frac{1}{R_1+R_2}\right)\frac{V_B}{I_B}=1-\exp\left(-\frac{t}{\tau}\right), \tag{2.4}$$

where $\tau = R_1C$ is the time constant

Substituting equation (2.3) into equation (2.4) and due to the resistive divider among R_1 and R_2, then $V_2 > V_B$ allows to obtain the two stability conditions.

$$\exp\left(-\frac{t}{\tau}\right)< 1, \tag{2.5}$$

$$\frac{R_1+R_2}{R_1}>\frac{I}{I_B}, \tag{2.6}$$

Equation (2.5) assume to be positive and always less than one when the transient conduction time t_C is lower than the time constant R_1C as occur in the signal V_B and is expected in V_C and V_E signals during t_2 as shown in Fig. 2.3. While equation (2.6) shows how must be the current ratio of I and I_B as a function of the resistors R_1 and R_2.

Based on the time-evolution of signal V_B as depicted in Fig. 2.3, a design criterion for the R_1-C-R_2 circuit to operate under reconfigurable mode; therefore, must satisfy that $t_C < R_1C$ and $R_1 > R_2$ to ensure stable operation during t_2 (off-state interval of signal V_B).

2.2.2. Practical Examples

Using the derived analysis in the previous section, two examples were developed to demonstrate the circuit operation in each case (see Fig. 2.4). In both circuits, the n-p-n BJT (type BC547; Fairchild Semiconductor) and ceramic capacitor C = 22 nF of low equivalent series resistance (ESR) type were used. All the resistors for biasing purpose were of ¼ W at 5 %.

To case 1 were used the following components: R_1 = 68 kΩ, R_2 = 22 kΩ, and R = 2.2 kΩ, where the operating stages and experimental waveforms are displayed in Fig. 2.5. At the base of Q, the waveform received through the capacitor C behaves like to the signal V_B of the Fig. 2.3 when the operating frequency was 500 Hz with duty cycle of 20 % and V_1 = 3 V. First, when the input positive pulse (V_{IN}) is setting (stage 1), there was bias current I_B across the base region as a function of the resistive divider among R_1 and R_2, and the positive-going excursion drives Q toward saturation mode. Second, when Q drives in cut-off mode, negative-going excursion have effect and charge time of capacitor C is limited by R_1 depended on V_2 where it is made variable from 3 V to 9 V and time interval t_C is reconfigured during stage 2. Third, the discharge time for capacitor C occur throughout of R_2 and impedance of the base-emitter junction of Q. Here, an off-current (I_{OFF}) flows during the zero voltage V_{IN} at the time interval larger than constant R_2C (stage 3).

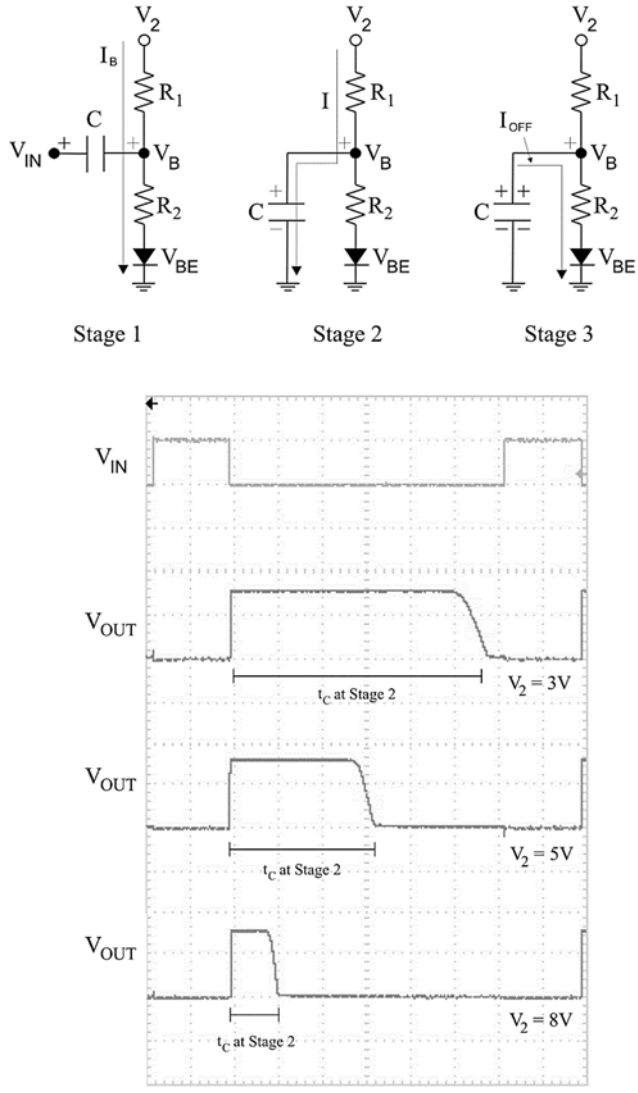

Fig. 2.5. Conduction time in the reconfigurable inverter and experimental input-output waveforms at three bias voltages.

To case 2 were used the following components: R_1 = 52 kΩ and R_2 = 18 kΩ to operate under large-signal condition, where the operating stages and experimental waveforms are displayed in Fig. 2.6. First, when the input positive pulse (V_{IN}) with operating frequency of 280 Hz, duty cycle of 20 % and V_1 = 3 V during stage 1, Q is already saturated by variable base current I_B limited by R_1 and R_2 and depended on V_2 from 3 V to 12 V, thus a positive-going pulse in R_2 results. Second, the zero-going input pulse allows that the waveform received in the base of Q behaves like to the signal V_B of Fig. 2.3, where capacitor C is charged by R_1-C circuit action and off-state action is generated which means that no bias current I_B across the base of Q occur which results in cut-off state (stage 2). Third, at the point which the excursion of the signal V_B during off-state is not sufficient

to retain the base-emitter junction (diode) and R_2 in cut-off state, discharge in the C-diode-R_2 circuit has effect and Q once again saturates, enabling the flow of an on-current (I_{ON}) which favors a positive-going pulse excursion in R_2 during stage 3 whose time interval t_C must be larger than the constant R_2C. In addition, so that R_2 is lower than R_1 and there is no collector resistor, can be expected non-equal pulse amplitude in R_2 in comparison to V_1 amplitude.

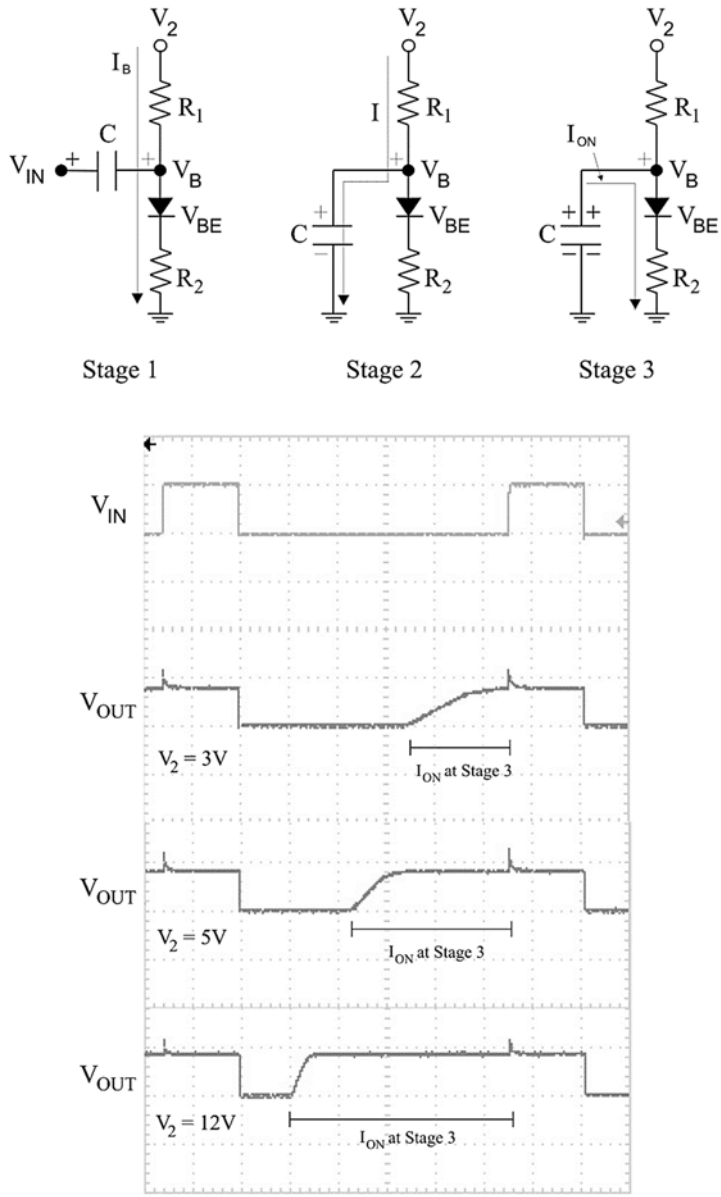

Fig. 2.6. Conduction time in the reconfigurable non-inverter and experimental input-output waveforms at three bias voltages.

2.3. Circuit Architectures

New technologies are required to solve existing challenges and achieve the desired performance for novel operations as it applies to the emergent applications focused on sustainable engineering. The specific scope that the sustainable engineering must address can be still unclear today but taking advantage of the reconfigurable conduction mode could be crucial to design building blocks as driver circuits under feasible conditions for activating power devices (e.g., in soft switching mode and similar other); therefore, this approach may be advantageously an ideal scheme for progress and scale-up pathway dependent on existing standards. Hence, based on foregoing principles detailed in Section 2.2, some theoretic models for circuit architectures are next discussed.

2.3.1. Time-shifted Pulses

The demand for power devices is growing phenomena to enable our daily lives. From power conversion to autonomous supplies in driving machines, such as electric cars, warehouse robots, and automata inside industrial process, there are different necessities for better performance of the gate-controlled devices dependent on the size and weight in the circuit used for triggering them [18]. Although it is recognized that advances in power semiconductor technology continuously improve physical characteristics, it is still worthwhile considering the degree to which gate-triggered circuits affect the overall system performance.

In general, the trigger circuit must be specified in terms of the minimum energy at the gate, length of time in which it must be active, and the maximum time allowed for the signal to rise from zero to its required amplitude [18, 19]. To ensure that the whole physical conduction area of the power device is turned on and it is available for full conduction, a minimum pulse width must be allowable to maintain the gate voltage or gate current paths distributed to a minimum to keep capacitive and inductive reactance's at their lowest possible level in optimizing the overall triggering action.

To describe how the power devices, such as a silicon-controlled rectifiers (SCRs) operating at 60 Hz can allow reduction in both volume and weight for the trigger circuit, a diagram for time-shifted pulses circuit shown in Fig. 2.7 is proposed. Their architecture has one reconfigurable non-inverter, one soft inverter, and one reconfigurable inverter whose basic operating principle can be discussed as follows. For instance, when a full-rectified wave is first converted in short time pulses V_{IN} and these are applied to the reconfigurable non-inverter, a large positive excursion V_{SE} at the soft-inverter output is caused by the reversed pulse excursion in R_2 depending on bias voltage V from 3 V to 9 V to operate approximately from 10 % to 90 % duty cycle. Thus, when signal V_{SE} is applied as displayed in Fig. 2.8, the narrowed pulses at V_{OUT} from the reconfigurable inverter can be triggered. The suggested components, R = 220 Ω, R_1 = 39 kΩ, R_2 = 10 kΩ, R_3 = 2.2 kΩ, R_4 = 15 kΩ, R_5 = 3.3 kΩ, C_1 = 470 nF, C_2 = 100 nF, and n-p-n BJT (type BC547; Fairchild Semiconductor) could be used when the proposed architecture is developed.

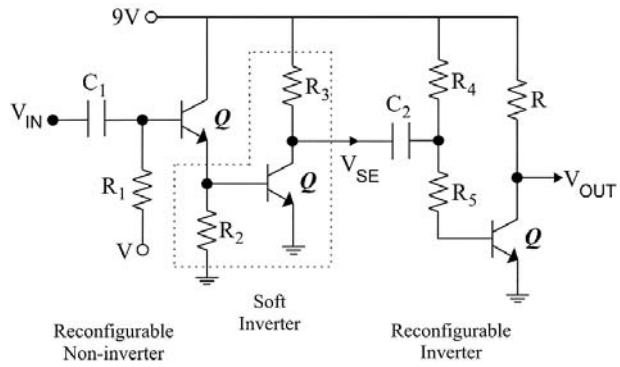

Fig. 2.7. Trigger circuit inspired on reconfigurable mode conduction using circuits of Fig. 2.4.

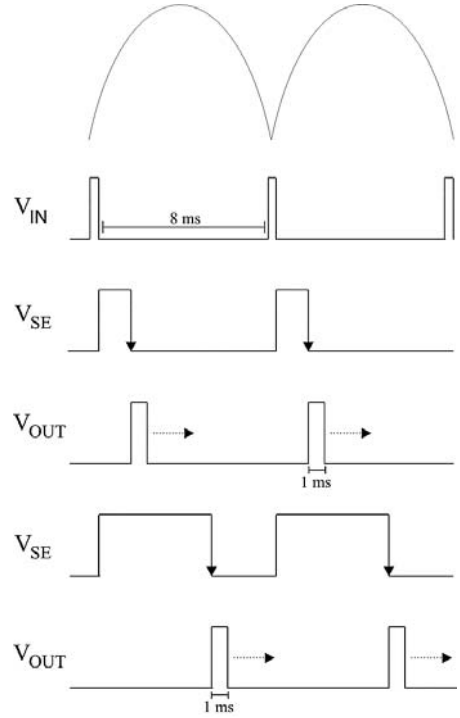

Fig. 2.8. Expected waveforms when a full-rectified wave at 60 Hz is narrow pulse converted and processed in the circuit of Fig. 2.7.

2.3.2. Timing Sequences

Nowadays, 3-phase induction motors are cost-effective in electromechanical energy conversion (EEC) in industrial, residential (ventilation, air conditioning, heating, and pumping systems), and automotive applications. Due to the low maintenance, inexpensive design, and variable-speed capability make the 3-phase induction motor (IM) the work horse for power management [18]. Still, the 3-phase IM from their stator wiring needs to

induce a magnetic field in the rotor which consists of a wound rotor or squirrel cage type, where the magnetic field can be generated by the frequency-depend circulating currents resulted from the rotating magnetomotive force (MMF).

A variable-frequency circuit architecture able to adjust the motor speed by varying the electrical frequency could be achieved via a rectifier stage, a direct current (DC) bus voltage, an inverter stage of six power switches from sw1 to sw6 performed by driver circuits useful to active timing sequences as shown in the scheme of Fig. 2.9 [20, 21]. In the last decades, variable-frequency operation methods have been classified in two major classes: scalar control and vector control. Scalar control, popularly known as voltage/frequency (V/F) control is considered as a simple approach based on the modification of DC voltage amplitude and the frequency. Vector control, known as field-oriented control allows not only the change in amplitude and frequency of the voltage vectors, but also the instantaneous position of the flux and the separated operation of the flux and the torque by adjusting the direct and quadrature component of the stator currents [18, 21]. Today, such control methods are implemented using advanced digital processors where computing algorithms to synthesize complex real-time signal sequences are encoded with programming languages, such as assembler, C and C++ to increase accurate in the speed regulation and soft star-up for 3-phase IM operation [22]. But, the rotor and stator losses in the 3-phase IMs can limit their operation response, due to the high-frequency pulse width modulation (PWM) switching in the inverter stage, and anomalous distributed wiring that can induce significant noise and recurrent errors in the signal sequences when these are transferred to the driver circuits [20].

Advances in power semiconductors, great progress in digital processors as well as in magnetic material (permanent magnets) technology, today are an important factor in power signal processing which have enabled alternative motor technologies such as brushless DC motors [22]. But, high cost of the permanent magnets, unstable high-frequency PWM switching, complexity in computing algorithms, and mainly environmental concerns in silicon semiconductor industry are the primary reason for seeking solutions in both industrial and residential sector in order to get an optimized performance capable to mitigate the losses experienced in the process of generating the rotor magnetic field as function of the behavior of the per-phase equivalent circuit and speed-torque equations as shown in Fig. 2.9.

Thus, operation of the low-power electric motors (lower than 500 W) will must be advantageously realized to ensure minimal hardware complexity (fewer building blocks), soft switching-mode operation at lower frequencies, better noise immunity, and minor maintenance requirements.

For example, processing the timing sequences of Fig. 2.10 in a start-connected 3-phase induction motor realized with the variable-frequency circuit architecture of Fig 2.11 can be performed as shown in the equivalent scheme of Fig. 2.12 when six conduction states for power switches from sw1 to sw6 of Fig. 2.9 are enabling; then a reconfigurable operating principle in the 3-phase IM by means of a variable-frequency inverter stage focused on timing sequences of Fig. 2.10 would allow activation of power switches, such as N-channel power MOSFETs or IGBTs through the classical driver circuits.

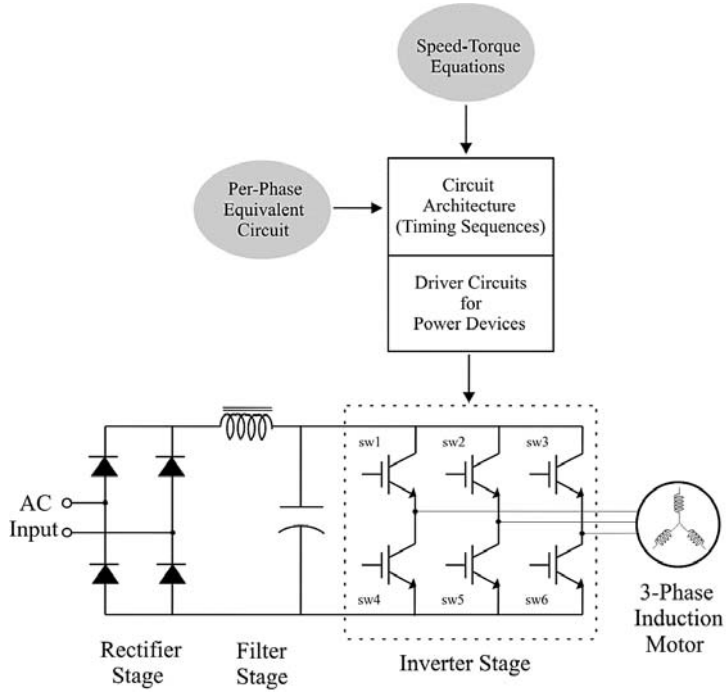

Fig. 2.9. Typical scheme showing the building blocks for power signal processing for 3-phase induction motor.

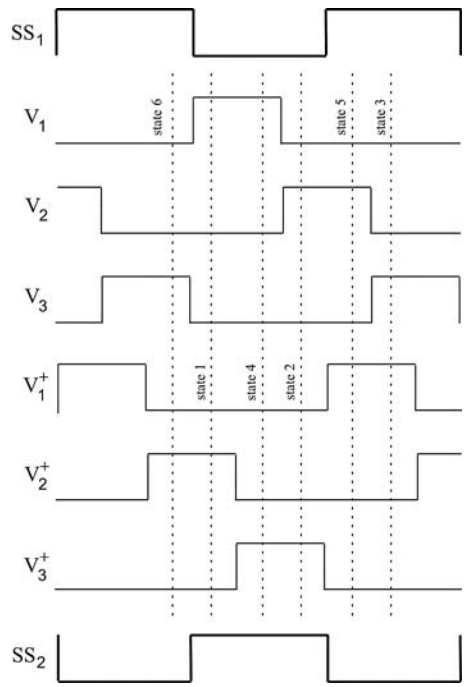

Fig. 2.10. Timing sequences to satisfy the soft mode conduction in a 3-phase induction motor.

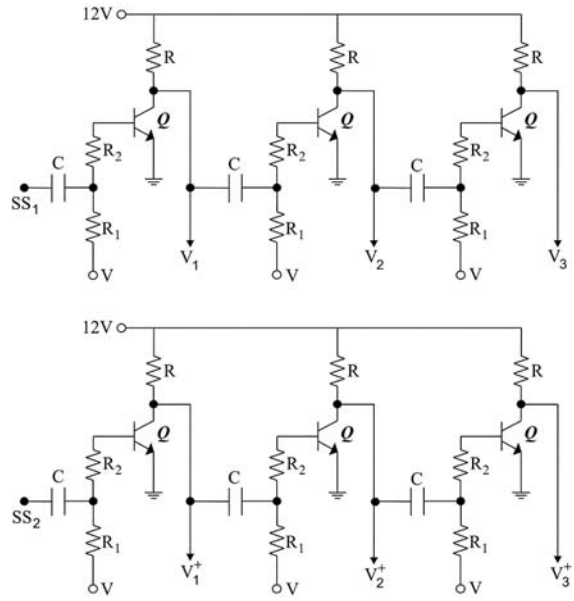

Fig. 2.11. Reconfigurable circuit architecture inspired on cascade-connected inverters to produce the timing sequences of Fig. 2.10.

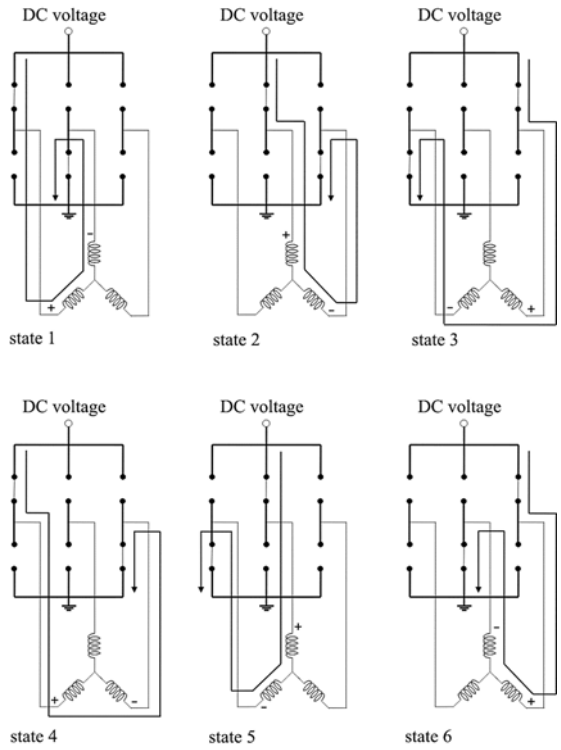

Fig. 2.12. Conduction states of power devices in the inverter stage using equivalent switches in each time sequence of Fig. 2.10.

Due to the electrical characteristics imposed by the CMOS technology-based driver circuits (i.e., integrated circuit IR2109), the supply voltage for the circuit architecture of Fig. 2.11 must be above 10 V, thus, cascade-connected inverters appropriate to operate from 20 Hz to 50 Hz in reconfigurable mode will be dependent on decreasing bias voltage V ranged from 12 V to 5 V when them are start-up, for examples with two variable-frequency square signals SS_1 and SS_2. The time sequences as three pulses V_1, V_2, and V_3 or V_1^+, V_2^+, and V_3^+ as displayed in Fig. 2.10 can be produced for triggering each trailing edge of the preceding pulses, respectively. Therefore, when portion of the negative signal excursion in SS_1 or SS_2 signal is applied to the base-emitter junction in each first transistor, the cut-off state occurs, resulting in a positive pulse V_1 or V_1^+ of width adjusted by V. The same action will occur when the trailing edge of V_1 or V_1^+ injected in each second transistor, as well as the trailing edge of V_2 or V_2^+ injected in each third transistor are accomplished, then, each transistor will be driven at cut-off state where a pulse V_2 or V_2^+ and pulse V_3 or V_3^+ with width adjusted once again results at their output.

The proposed components, R = 2.2 kΩ, R_1 = 47 kΩ, R_2 = 4.7 kΩ, C = 220 nF, and n-p-n BJT (type BC547; Fairchild Semiconductor) can be used when the circuit architecture of Fig. 2.11 is developed.

2.4. Conclusions

Electric and thermal limitations commonly occur in semiconductor-based modern technologies in several forms: Conduction losses caused by skin effect because the wiring effective resistance increase when the frequency-depend energy required to generate magnetic fields is transferred; Material losses related to the magnetic flux cycles is responsible during the energy conversion, because eddy currents flows in circular current paths; Structure losses due to the extreme scattering phenomena by anomalous high electrical currents paths are triggered by temperature increase runaway in semiconductor devices at low voltage operation.

Next-generation sustainable technologies must be planned to operate within a lower losses scheme and more efficiently in terms of electrical energy management. Therefore, reconfiguration was suggested as a promising strategy where soft mode conduction can be usefully enabled. Here was suggested the modification for the bias voltage, so that to define the dynamic behavior of passive components (i.e., resistors and capacitors). Due to the BJT have advantages over CMOS transistor in terms of their reconfiguration qualified by reduced number of building blocks, unstressed electrical conduction, and unusual modes of operation; thus architecture-level technology based on BJT-similar physical structures resulted from advanced materials research might encourage scalable commercial chip solution, satisfying recyclability issues next years to fabrication of emergent functional devices by socially and environmentally responsible professionals.

Acknowledgement

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Chapter 3

Models and Techniques for Reliability Studies of Nano-scaled Interconnects

Hajdin Ceric, Houman Zahedmanesh, Roberto Lacerda de Orio, and Siegfried Selberherr

3.1. Introduction

The reliability of interconnects is affected by a complex degradation process driven by several driving forces, each of which being present from the very beginning of interconnect technology. These forces are electromigration (EM), stressmigration (SM), and thermomigration (TM). The driving forces induce a material transport in the interconnect metal, which damages the crystal structure and causes the formation of intrinsic voids. The increase of the metal resistance due to migration and growth of intrinsic voids leads finally to interconnect failure.

The thermal budget in integrated circuits (ICs) represents a problem beyond TM in interconnect metals. The heat produced by Joule heating in the interconnects in addition to the heat produced by other devices induces thermomechanical stress throughout the ICs and also affects the reliability of transistors.

Low-*k* materials have been introduced to ensure high performance of ICs with their low dielectric constant, but, unfortunately, they have brought additional thermal and mechanical problems. Low mechanical strength of low-k materials does not offer as much restraint for the degradation driving forces as sillca-based interlevel dielectric materials. Another problem with low-k dielectrics is their poor thermal conductivity which adds to the already severe thermal problems of ICs. As the thickness of interconnects decreases, the importance of material transport along grain boundaries (GBs) and interfaces increases [1-4]. Thus, the lifetime of interconnects becomes more sensitive to the values of the parameters which determine the transport, such as effective valences and diffusivities. The interconnect thickness also has an impact on the interconnect resistivity and the effective

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valence, which have to be considered [5, 6]. The material transport is additionally determined by the GB distribution and the orientation of single grains. The metallic microstructure in a given interconnect is influenced by the specific process conditions, choice of materials, and interconnect dimensions [7]. Improvement of the reliability for future nano-scaled interconnects can be achieved with the introduction of copper technology modifications or application of new metals as replacement for copper. Significant improvement was achieved by introducing CoWP capping layers which efficiently suppressed EM along interfaces [8, 9]. Besides CoWP, several other capping layer materials like CuSiN, CuGeN, $MnSi_xO_y$, etc. have been tested, which also improve the EM performance. Another possibility to influence the EM behavior is to change the barrier layer which covers the bottom and side walls of the copper interconnect from a typically Ti or Ta based material to Ru or its alloys etc. [10, 11]. In order to suppress EM along GBs (Fig. 3.1) dilute Cu alloys have been successfully applied. A significant reduction of material transport along the GBs has been achieved by alloying Cu with Al [12] and Mn [13-15].

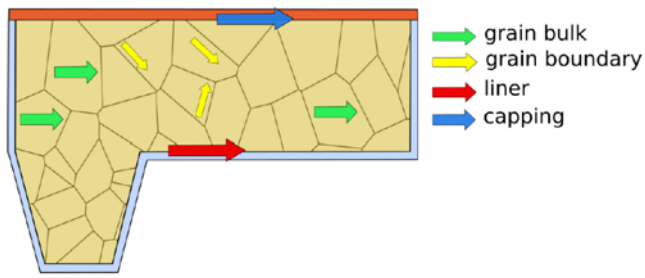

Fig. 3.1. Interconnect line with its different migration paths for material transport.

The necessity to wrap the Cu wires (in order to prevent copper migration into the neighboring dielectric) into metallic and dielectric diffusion barriers represents an additional major obstacle for scaling the dimensions of Cu interconnects below 10 nm, because the barrier itself is made of a material which has a higher resistivity than Cu. Therefore, the actual effective resistivity of the combined Cu interconnect and barrier layer is increased [10]. This barrier problem with Cu becomes even more apparent, when one considers that a practical realization of a via structure needs more barrier material than a straight interconnect line [3]. This is one of the important motivations to look for Cu replacement, besides more favorable EM properties.

To use a metal with a higher bulk resistivity than Cu, but which does not demand a barrier layer, is a preferable option [16], provided that in total it may have a similar or even lower resistivity than Cu [16]. Several metals and alloys which have potential to replace copper in the future, like Co, Ru, Ni(B) etc., have been proposed and studied in recent years [1, 3, 4, 6, 16]. Some of the metals under investigation, like Co and Ni, are magnetic. Depending on the application, the interconnect geometry, the operation frequency, and the magnetic field have to be considered.

For each metal or alloy, the prediction of the actual location of the void embryo emergence represents a challenging issue. In the case of Cu, voids nucleate inside the interconnect line either at the cap interface or at the bottom of a via or in the bulk of the interconnect metal above the via, as presented in Fig. 3.2. These different sites of void nucleation and the subsequent void dynamics lead to a multimodality of interconnect failure [17, 18].

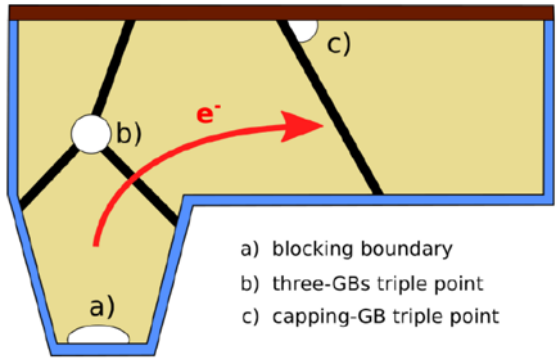

Fig. 3.2. Three characteristic void nucleation sites inside a dual-damascene interconnect.

3.1.1. Black's Equation

Since its publishing, Black's equation [19] is a widespread and a very popular mathematical basis for modelling and predicting interconnect failure behavior. It expresses a median interconnect time-to-failure, t_{MTTF}, in dependence of the following three parameters: the pre-exponential A coefficient, the current exponent n, and the activation energy E_a.

$$t_{\mathrm{MTTF}} = \frac{A}{j^n} exp\left(-\frac{E_a}{k\,T}\right) \tag{3.1}$$

Particularly important here is the activation energy E_a, because this parameter has the largest impact on the predicted median interconnect time-to-failure (MTF), as we can see from (3.1). If we consider the physics of EM induced transport, it becomes clear that the activation energy as used in (3.1) is a result of the cumulative effect of several different activation energies related to the various different migration paths. For a complete picture of EM degradation, at least the following migration paths must be considered:

- Grain bulk;
- Barrier layer;
- Capping layer;
- Grain boundaries.

Each of these migration paths is characterized its own diffusion coefficient which depends on the particular diffusion coefficient pre-exponential and on the particular activation

energy. Generally speaking, the cumulative activation energy, as used in (3.1), is not only a function of the activation energies of each of the above-mentioned migration paths, but also a function of the interconnect's layout geometry and microstructure.

3.1.2. Beyond Black's Equation

The cumulative activation energy, E_a, is routinely determined during EM tests and the knowledge of its value is quite useful for the prediction of interconnect lifetimes, but rather problematic, if one wants to study in detail the particular degradation mechanism which leads to the EM failure itself. The crucial question is to which extent each of the activation energies of the different acting migration paths actually contributes to the cumulative activation energy. The importance of this question becomes obvious, if one considers some new material for the capping or the barrier layer, or to modify the copper electro-deposition process in such a way that it influences the copper microstructure. In such a case, the real impact of the technological change must be estimated. There are two ways how this can be done. The first one is experimentally, where a dedicated measurement setup is used to estimate the activation energy of the new capping and barrier interface. The second approach is the application of simulation using physics-based models. This approach provides not only a far more comprehensive understanding of the impact of new materials, but also offers a deeper insight, how the whole degradation process leading to the failure unfolds.

3.2. The Physics-BASED Modelling of Electromigration

Physics-based modelling of EM uses the framework [20], which represents a further development from the original work of Sarychev and Zithnikov [21]. According to this modelling approach, the lifetime of an interconnect structure t_f consists of a void nucleation time t_N and a void evolution time t_E, corresponding to two failure development phases.

$$t_f = t_N + t_E \tag{3.2}$$

Each of these two phases demands its own modelling effort.

The central governing equations of EM models are the vacancy flux equation (3.3) and the vacancy balance equation (3.4).

$$\overrightarrow{J_v} = D_{\text{eff}}\left(\frac{C_v}{kT}|Z^*_{\text{eff}}e|\rho\vec{j} + \frac{C_v}{kT}f\Omega\nabla p - \nabla C_v\right), \tag{3.3}$$

$$\frac{\partial C_v}{\partial t} = -\nabla\cdot\overrightarrow{J_v} + G_{\text{eff}}(C_v), \tag{3.4}$$

where D_{eff} is the local diffusivity, C_v is the vacancy concentration, p is the hydrostatic stress, ρ is the interconnect resistivity, $\vec{j}$ is the current density, Ω is the atomic volume, and f is the atom-vacancy relaxation factor. G_{eff} is the Rosenberg-Ohring recombination

term and Z^*_{eff} is the effective valence. In order to reproduce realistic mechanical conditions, all materials in the structure and their corresponding properties must be included in the modelling framework. Both the void nucleation model, as well as the void evolution model, are solved simultaneously with the equations of mechanics [21].

$$\frac{\partial \varepsilon_{ij}^{v}}{\partial t} = \frac{1}{3}\left[(1-f)\nabla \cdot \overrightarrow{J_v} + f G_{\text{eff}}(C_v)\right]\delta_{ij}, \tag{3.5}$$

$$\nabla \cdot \sigma = 0, \quad \sigma = E\left(\varepsilon - \varepsilon^{v} - \varepsilon^{th}\right), \tag{3.6}$$

where E is the the fourth-order elasticity tensor, ε^{v} is the volumetric strain component which rises due to EM, and ε^{th} represents the impact of thermal loads.

From the stress tensor σ, the normal stresses at all interfaces and GBs can be obtained. The *void nucleation phase* ends, when one of the normal stresses surmounts the local critical stress threshold σ_{crit}, which is discussed in the next sections. The time needed for the critical stress threshold to be reached is the void nucleation time t_N.

3.2.1. Blech's Equation

The dynamics of the vacancy flux $\overrightarrow{J_v}$, plays a crucial role in the development of EM failure. When for $\overrightarrow{J_v} = 0$ the stress equilibrium state is achieved (cf. Fig. 3.3) for a back-flow stress which is lower than the critical stress-threshold needed for void nucleation, the interconnect is virtually "immortal" (arbitrarily long-living). This situation corresponds to the generalization of the one-dimensional Blech effect.

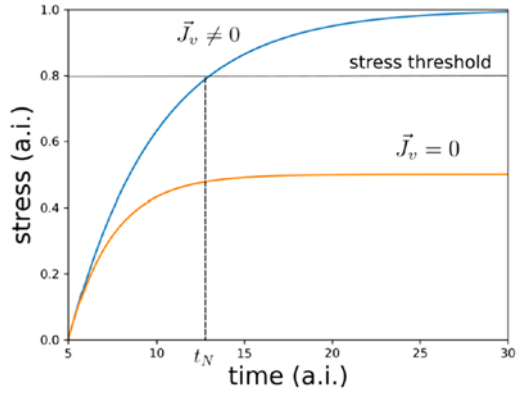

Fig. 3.3. Stress dynamics depending on the zero-flux condition.

If one assumes that the pressure and vacancy concentration are in a local equilibrium [20]

$$C_v = C_v^0 exp\left(W_f - \frac{\Omega p}{kT}\right), \tag{3.7}$$

where W_f is the interaction energy between the vacancy and the stress field and C_v^0 is the vacancy concentration in the absence of any stress effects, the Blech's condition follows directly from the zero-flux condition ($\vec{J_v} = 0$), by inserting (3.7) into (3.3). One obtains for a one-dimensional linear interconnect of length l

$$j_x l = \frac{\Omega(1+f)\Delta\sigma_x^{eq}}{\rho\left|Z_{eff}^* e\right|} = \frac{\Omega(1+f)\left|\sigma_x(l) - \sigma_x(0)\right|}{\rho\left|Z_{eff}^* e\right|}, \tag{3.8}$$

where $p = -\sigma_x$ and $\sigma_x(l)$ and $\sigma_x(0)$ are the stresses at both ends of the linear interconnect. When the zero-flux condition is attained for a certain back-stress which is higher than the critical-stress needed for void nucleation, a void embryo is formed.

3.2.2. Effective Valence and Resistivity

The bulk effective valence Z_{bulk}^*, and the resistivity ρ are related on a fundamental physical level, because both parameters characterize different aspects of electron scattering in a current carrying metal [22].

$$Z_{\text{bulk}}^*(T) = Z_d + Z_w(T) = Z_d + \frac{K}{\rho(T)}, \tag{3.9}$$

where Z_d is the direct valence which is assumed to be equal to the bare valence of Cu, and K is the proportionality factor which has been fitted for Z_{bulk}^* for a thick interconnect at room temperature. Various advanced models can be used for modeling the interconnect resistivity [23].

Because on average, there are fewer atoms inside the GBs than in the bulk, the GB region presents a repulsive potential to the electrons. Consequently, the electron wind force in the GB region is lower than in the bulk. As shown by Sorbello [24] even for a low GB potential (1/10 of the Fermi energy), the wind force inside the GB is about 20 % smaller than in its immediate vicinity outside the GB.

3.2.3. Conditions for Void Nucleation

The conditions for void nucleation are determined by either the geometrical and/or the microstructural features of the interconnect metal and layout. One particular geometrical feature can hinder vacancy flux and thus cause a local increase in the concentration of vacancies, which in turn leads to a local increase in the tensile mechanical stress. After a certain stress-threshold is attained, an initial void is nucleated [25, 26]. A microstructural feature, such as a GB, can also lead to a local disturbance of material transport and to a subsequent rise in tensile stress at so-called triple points (an intersection of a GB with an interface). The absolute critical value of stress σ_{crit} can be expressed as

$$\sigma_{\text{crit}} = \left(\frac{kG_cB}{h_{Cu}}\right)^{1/2}, \tag{3.10}$$

where G_c is the interface energy per unit area related to the top interface of the line between Cu and the cap layer. B denotes the confinement/effective modulus, h_{Cu} denotes the height of the line, and k is a calibration parameter. All parameter values are set according to previous works [27, 28].

3.3. Modelling of the Microstructure

The microstructure of Cu interconnects generally depends on the technological process, the interconnect geometry, and the choice of surrounding materials. Different choices of materials for barrier and cap layers may influence properties of the microstructure [28]. There are several studies dealing with the impact of the Cu microstructure on the EM failure behavior [29, 30]. They describe, how the GBs distribution and the texture inside single grains influence the interconnect failure and the failure time distribution. For a complete modelling of the microstructure, besides a description of the grain crystallography, an appropriate understanding of the GB physics is a necessity. The following three aspects of GB physics must be considered [31]:

- The GB as a fast diffusivity path;
- The GB as a site of vacancy production and annihilation;
- The GB as an obstacle to material transport.

In the case of typical microstructures for small interconnects, two additional aspects must be considered. First, the microstructure strongly depends on the interconnect width and second, due to the increased temperatures during operation, the microstructure may undergo transformations. Experimental SEM/FIB/EBSD [32-35] studies of interconnects' microstructures provide the grain size distribution and the crystal orientations inside grains. The studies show that the grain sizes inside Cu interconnects are distributed according to the lognormal distribution and tend to have several predominant crystal orientations [34]. An "effective values" approach has been used for a long time to model the cumulative effect of different atomic transport paths on the overall diffusivity. The main advantage of this approach is its simplicity, because one basically needs only the geometrical dimensions of the interconnect line and some characteristics of the microstructure to calculate an effective value of diffusivity and effective valence. The GB volume fraction ϵ_p dependent effective values of the Rosenberg-Ohring term G_{eff}, the effective valence Z^*_{eff}, and the effective diffusivity D_{eff}, are given by the following terms, respectively [27]:

$$G_{\text{eff}}(C_v) = -\left(C_{eq} - C_v\right)\left(\frac{1-\epsilon_p}{\tau_{\text{bulk}}} + \frac{\epsilon_p}{\tau_{gb}}\right), \tag{3.11}$$

$$Z^*_{\text{eff}} = Z^*_{\text{bulk}}\left(1-\epsilon_p\right) + Z^*_{gb}\epsilon_p, \tag{3.12}$$

$$D_{\text{eff}} = D_{\text{bulk}} + D_{\text{lin}}\left(\frac{2}{w} + \frac{1}{h}\right)\delta_{\text{I-lin}} + D_{\text{cap}}\frac{\delta_{\text{I-cap}}}{h} + \epsilon_p D_{gb}, \tag{3.13}$$

where h is the interconnect height and w is the interconnect width. Each transport path is characterized by its diffusivity and its thickness: bulk (D_{bulk}, h), cap layer (D_{cap}, $\delta_{\text{I-cap}}$), and liner (D_{lin}, $\delta_{\text{I-lin}}$).

Equations (3.11), (3.12), and (3.13) can be directly used for parametrization of the vacancy dynamics model given by equations (3.3) and (3.4). However, this type of "cumulative" microstructure description is inadequate to capture microstructural features important for interconnect reliability. A model which is able to capture all the relevant microstructural aspects requires a detailed description of the vacancy dynamics at a single GB as introduced in [31].

For the implementation in the GB plane (Fig. 3.4), the model is described by the Rosenberg-Ohring term

$$G_g = -\frac{1}{\tau_g}\left(C_v^{eq} - C_v^{im}\left(1 - \frac{2\omega_R}{\omega_T(C_{v1} + C_{v2})}\right)\right), \tag{3.14}$$

and a segregation condition at the GB, which regulates the vacancy transport from the Grain 1 to the Grain 2.

$$J_{12} = \omega_T\left(C_v^{eq} - C_v^{im}\right)(C_{v1} - C_{v2}), \tag{3.15}$$

where C_{v1} and C_{v2} are the vacancy concentrations in Grain 1and Grain 2, respectively, ω_T is the vacancy-trapping rate, ω_R is the vacancy release rate, C_v^{im} is the concentration of vacancies trapped in the GB, C_v^{eq} is the equilibrium vacancy concentration, and τ_{gb} is the vacancy recombination rate. The model is complete with the diffusivity D_{GB} in the GB plane. The detailed GB model, combined with the vacancy dynamics equations (3.2) and (3.3), produces pile-ups of vacancies at triple points in three-dimensional microstructures, as shown in Fig. 3.5. The corresponding peaks of the mechanical stress are presented in Fig. 3.6.

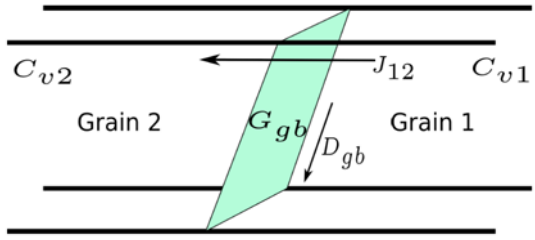

Fig. 3.4. Schematic picture of the two-dimensional GB plane.

The detailed GB model can be applied at the surface of an arbitrary shape defining the GB between two adjacent grains. The only condition is an appropriate FEM discretization of the surface.

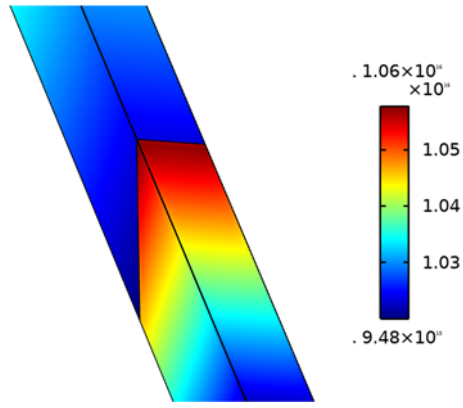

Fig. 3.5. Increase of the vacancy concentration (1/cm³) close to a triple point along the capping layer. The locations of the peak vacancy concentrations correspond to the peaks of the tensile stress.

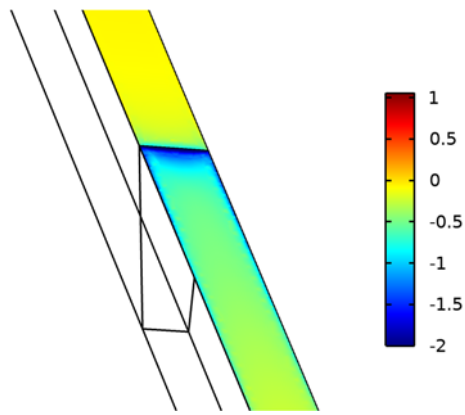

Fig. 3.6. Peak of mechanical stress (MPa) close to a triple point along the capping layer.

3.4. Analytical Model for Void Growth

In order to estimate the duration of the second phase of failure development, it is necessary to predict the void growth velocity. The normal velocity v_n of the void surface is calculated according to [20].

$$v_n = \Omega(\vec{J}_v \cdot \vec{n} - \nabla \cdot \vec{J}_s) \tag{3.16}$$

From (3.16) it can be seen that the void surface evolves due to the vacancy transport in the normal direction, $\vec{J}_v \cdot \vec{n}$, and the divergence of the surface vacancy flux, $\nabla \cdot \vec{j}_s$ (Fig. 3.7). The surface vacancy flux $\vec{J}_s$ itself rises due to the tangential component of the current density $\vec{j}_t$ and the surface gradient of the chemical potential μ_s.

$$\overrightarrow{J_s} = -\frac{D_s\delta_s}{kT\Omega}\left(\left|Z_s^* e\right|\rho\vec{j_t} + \nabla_s\mu_s\right), \tag{3.17}$$

where D_s is the surface diffusivity and δ_s is the thickness of the diffusion surface. The surface chemical potential μ_s is given as

$$\mu_s = \Omega(W_s - \gamma_s\kappa) \tag{3.18}$$

where γ_s is the surface energy, κ is the local curvature of the surface, and $W_s = (\sigma:\varepsilon)/2$ is the local elastic strain energy density. From (3.16)-(3.18) follows that there are four components of the surface velocity: the elastic strain energy velocity component v_n^s, the EM velocity component v_n^e, the surface free energy velocity component v_n^f, and the vacancy absorption velocity component v_n^v.

$$v_n = v_n^s + v_n^e + v_n^f + v_n^v \tag{3.19}$$

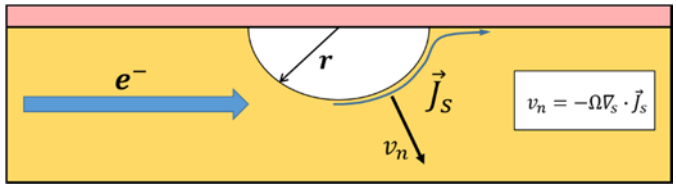

Fig. 3.7. Atom migration along the void surface and the resulting normal velocity.

We assume that the void possesses throughout its growth a half-cylindrical shape and that the EM velocity component (v_n^e) dominates over the other three velocity components.

$$v_n^e = \frac{D_s\delta_s\rho|Z_s^* e|}{kT}\nabla_s\overrightarrow{Jt} \tag{3.20}$$

The lower limit (the worst case) of the void evolution time t_E is obtained by assuming that the whole void of radius r grows with the maximum velocity at its surface, $v_n^{max}(r)$ [27].

$$t_E = \int_{r_0}^{r_c}\frac{dr}{v_n^{max}(r)} \tag{3.21}$$

Here, the critical void radius r_c is the solution of the equation

$$R_{failure} = R_{total}(r_c), \tag{3.22}$$

where R_{failure} is the predefined failure resistance (usually 20 % of the nominal interconnect resistance) and $R_{\text{total}}(r_c)$ is an analytical function estimating the resistance of an interconnect containing a half-cylindirical void with radius r_c. The initial radius of a void r_0 is estimated based on the local pressure distribution near the triple point, where the void is assumed to emerge (see Section 3.5).

Even in case of a fully three-dimensional simulation, due to the assumption of a half-cylindrical void, the tangential component of the current density $j_t(r,\theta)$ can be estimated for all void sizes and interconnect thicknesses h (= $2w$) as

$$j_t(r,\theta) = \frac{j_0 h \sin\theta}{h - r\sin\theta} q(r), \tag{3.23}$$

where j_0 is the current density far away from the void surface (in a region unperturbed by the presence of a void) and the angle θ (cf. Fig. 3.8) determines the position on the void surface. $q(r)$ is an additional fitting function [36] introduced to closely match the analytical surface velocity calculations with those calculated with COMSOL Multiphysics [37].

$$\mathrm{q(r)} = \sum_{\mathrm{i}=0}^{\mathrm{n}} (-1)^{\mathrm{i}} \left(\frac{\mathrm{r}}{\mathrm{h}}\right)^{2\mathrm{i}} \tag{3.24}$$

By substituting (3.24) in (3.23) and then (3.23) in (3.20), the following expression is obtained:

$$v_n(r,\theta) = \frac{D_s \delta_s \rho |Z_s^* e|}{kTr} \frac{dj_t(r,\theta)}{d\theta}, \tag{3.25}$$

The comparison of analytical surface normal velocity calculations (3.25) and COMSOL Multiphysics calculations for $h = 2w = 46$ nm and a current density $j = 1.0$ MA/cm² for two different void sizes ($r_1 = 0.6h$ and $r_2 = 0.8h$) and for a typical operating condition temperature of 100 °C is shown in Fig. 3.9. Since the worst case scenario is of interest, i.e., void growth with the maximum surface velocity, for the estimation of the void evolution time t_E in (3.21) the following expression is used:

$$v_n^{max}(r) = \frac{D_s \delta_s \rho |Z_s^* e|}{kTr} \max_{0 \le \theta \le \pi} v_n(r,\theta), \tag{3.26}$$

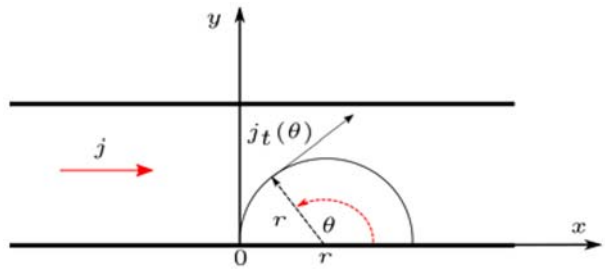

Fig. 3.8. Structure used in the derivation of equation (3.23).

3.5. Estimation of Initial Void Size

After an initial void is formed, the previously built stress ($p(x,y,z)$) relaxes. The volume of the initial void is determined as

$$V_0 = -\frac{1}{B}\int_V p(x,y,z)\, dx\, dy\, dz \tag{3.27}$$

In order to simplify the model implementation, it is assumed that a cylindrical void is formed around the triple point and spans the entire interconnect width w. This assumption allows for the calculation of the initial void radius r_0.

$$r_0 = \sqrt{\frac{2V_0}{\pi w}} \tag{3.28}$$

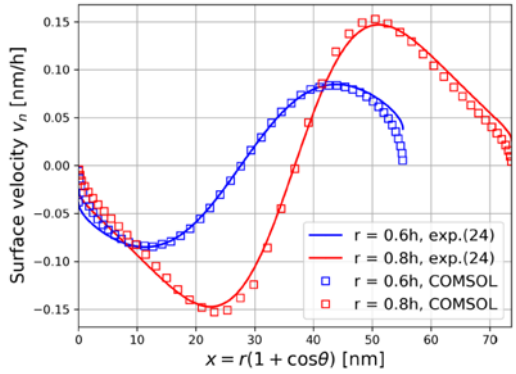

Fig. 3.9. Comparison between analytically calculated surface normal velocity using (3.25) with FEM calculation performed in COMSOL Multiphysics for 100 °C and for a current density $j = 1.0$ MA/cm².

3.6. Resistance Calculation

An increase of the interconnect resistance leads to interconnect failure. The resistance increase is caused by the emergence, subsequent growth, shape change, and movement of intrinsic voids. The evolving void surface can be modelled with different levels of accuracy, but more accurate modelling is always more computationally demanding. For the sake of simplicity and speed of calculation, we use three-dimensional void shapes with a simple geometrical basis, like a half-circle and a half-ellipse.

The resistance of an interconnect segment containing a cylindrical void with elliptical basis ($2a$ and $2b$ are the minor and major axes, respectively, cf. Fig. 3.10) is

$$R_0(a,b) = \frac{a\rho}{bw}\left[\pi\left(\frac{h}{s} - 1\right) + \frac{2h}{s}\arctan\left(\frac{b}{s}\right)\right], \tag{3.29}$$

with $s = (h^2 - b^2)^{1/2}$. The total resistance $R_{total}(a,b)$ for a void placed in a straight interconnect line is calculated according to the equivalent circuit presented in Fig. 3.11:

$$\frac{1}{R_{total}(a,b)} = \frac{1}{R_{cap}} + \frac{1}{R_{lin}} + \frac{1}{R_{metal}(a,b)}, \tag{3.30}$$

$$R_{metal}(a,b) = 2R_2(b)+R_0(a,b), \tag{3.31}$$

$$R_2(b) = \frac{\rho_{metal}(1-2b)}{2wh}, \tag{3.32}$$

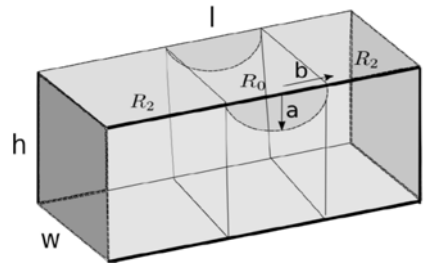

Fig. 3.10. Structure used in the derivation of equation (3.29).

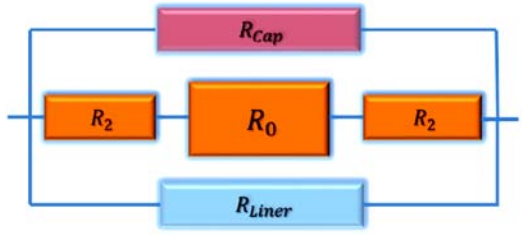

Fig. 3.11. Replacement schema for a segment of an interconnect containing a cylindrical void. The resistances of the cap layer, R_{cap}, and of the liner, R_{lin}, are included.

With the expressions (3.21) and (3.25), and the resistance calculation based on (3.30), the dependence of the void growth time on the interconnect dimensions can be determined. Fig. 3.12 shows the resistance increase for a 1 μm long and 23 nm wide interconnect section for three different temperatures and a current density j = 1.0 MA/cm^2.

3.7. Overall Scheme

In order to estimate the interconnect lifetime (t_f), both the void nucleation (t_N), as well as the void evolution time (t_E) must be estimated as accurately as possible. The complete simulation scheme utilized in this work is presented in Fig. 3.13. As one can see, the overall simulation procedure is divided into two parts: estimation of t_N (void nucleation time), which is performed numerically by application of the FEM, and the estimation of t_E (void evolution time), which is carried out analytically. The equation system solved in the FEM part of the simulation consists of equations (3.3)-(3.6) together with the Laplace equation for the electric field (cf. Fig. 3.13). The solution of the Laplace equation provides the distribution of the current density j inside the metallization, which is needed for solving the vacancy balance equations (3.3) and (3.4).

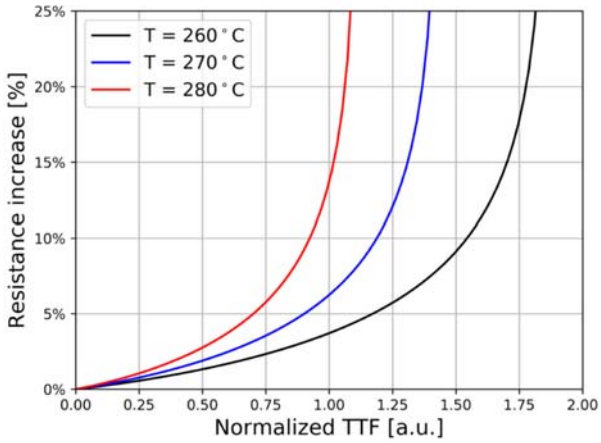

Fig. 3.12. Resistance change for three different temperatures.

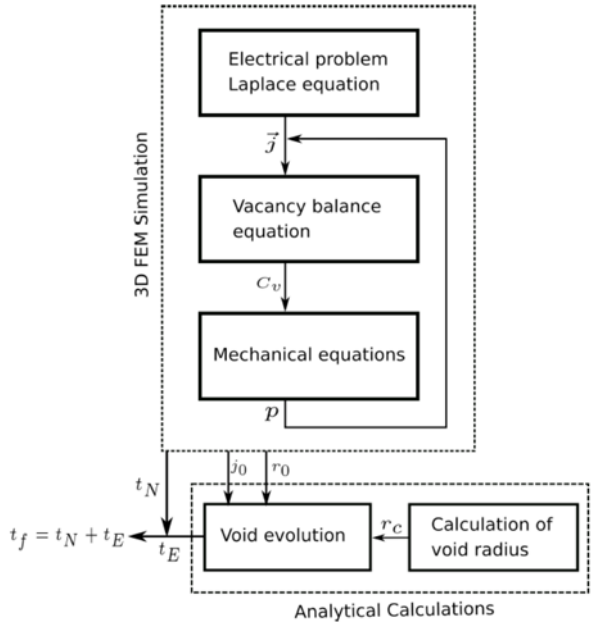

Fig. 3.13. Overall two-part simulation scheme. The void nucleation time is determined in the "3D FEM Simulation" part and the void evolution time in the "Analytical Calculations" part.

The solution of the vacancy balance equations determines the vacancy concentration C_v throughout the metal bulk. The redistribution of vacancies, driven by EM and the accompanying forces, gives rise to mechanical stress calculated by simultaneously solving equations (3.5) and (3.6). The vacancy balance equation and the mechanical equations are solved in a time loop, until the critical stress is reached at some triple point at the capping layer. This event also marks the end of the 3D FEM part of the simulation flow. The results from the 3D FEM solution, which are carried over to further processing are: the void

nucleation time t_N, the current density j_0, and the radius of the initial void r_0. The current density j_0 and the void radius r_0 are needed for the calculation of the void evolution time. The critical void radius r_c is obtained by solving equation (3.22).

3.8. Simulation Results and Discussion

The modelling framework described above is used to study the *failure time* dependence on:

a) Interconnect thickness;

b) Mechanical and material transport properties of SiN_x and Co caps.

COMSOL Multiphysics [37] was used for the simulations. The 1 µm long Cu interconnect is placed between two contacts and encapsulated in a Ta barrier layer on all sides except the top, which is covered with the cap layer. The Cu interconnect with all interface layers is fully embedded in SiO_2 (cf. Fig. 3.14). Typical material properties for all involved materials and interfaces are assumed, including a stress threshold of 20 MPa stress threshold for void nucleation at the SiN_x cap and of 30 MPa at the Co cap. The interface diffusivity at the SiN_x/Cu interface is assumed to be 100 times higher than at the Co/Cu interface. The temperature for the simulations is set at 300 °C. The detailed modelling approach allows for the observation of different physical characteristics as the failure develops.

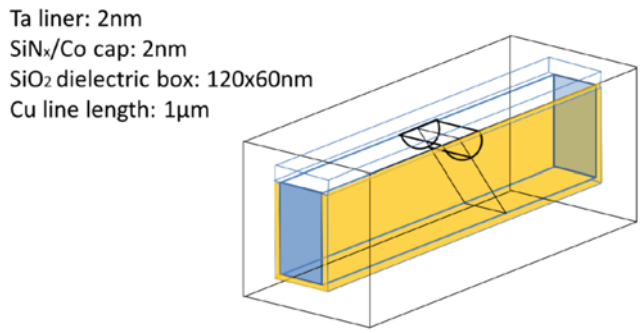

Fig. 3.14. Structure used for simulations. A cylindrical void nucleation is assumed at the triple point.

As one can see from (3.21), an estimation of the void evolution time (t_E) demands the extraction of the function $v_n^{max}(r)$, which can be studied in detail by the simulation results presented in Fig. 3.15, obtained by the overall simulation schema discussed in Section 3.7.

The interconnect lifetimes for both types of capping layers are significantly reduced for a thinner interconnect (cf. Table 3.1), but the benefit of replacing SiN_x with Co is clearly recognizable. This behavior is confirmed by numerous experimental results (e.g. [3, 16, 27, 38]), as expected, because for thinner interconnects a larger portion of atoms is

transported along the interfaces and a smaller void volume is sufficient to produce the fatal failure.

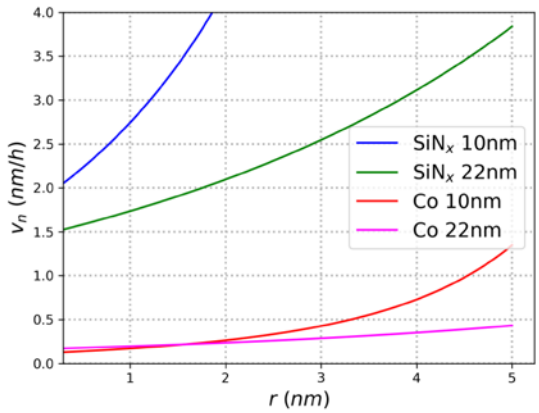

Fig. 3.15. Normal velocity (v_n) of the void surface in dependence on the void radius (r) for SiN_x and the Co cap.

Table 3.1. Lifetime dependence on interconnect thickness. All failure times are normalized to the t_F, the failure time of a 22 nm wide interconnect with a SiN_x cap.

Capping	**Thickness [nm]**	t_N/t_F	t_E/t_F	t_f/t_F
SiN_x	10	0.200	0.099	0.299
SiN_x	22	0.395	0.605	1.000
Co	10	0.304	1.598	1.902
Co	22	0.608	5.379	5.987

3.9. Conclusion

By reducing the width of interconnects to 10 nm and below, while at the same time considering Cu-replacement metals, interconnect reliability studies are on the verge of entering uncharted territory for the first time in more than 20 years. While experimental methods for the analysis of interconnect failures have been gradually improved and refined, mathematical models, which were directly applied for study of experimental results, have remained to a large part basically one-dimensional models. These models inevitably rely on effective and average properties of crucial parameters, e.g. diffusivity, and mostly ignore explicit three-dimensional features, which indubitably influence these parameters. As we know today, the reliability of downscaled interconnect increasingly depends on the atomic migration along interfaces, whereas the interconnect metal microstructure plays an important role and thus must be addressed accordingly. To meet the challenges of current and future interconnect reliability, an application of advanced physically based models is a necessity. The development of these models took place in parallel to the development of advanced experimental methods, but they have never been

fully utilized for the study of experimental results. We presented an EM reliability model which considers different effects related to the narrowness of the interconnect, as well as to the particular material choice needed for a layout realization. Among the particular effects taken into account are the effective valence dependence on the microstructure and interconnect thickness, the effects of interfacial EM paths, and void growth under the assumption of a narrow interconnect. The dependence of interconnect lifetimes on length, thickness, and the diffusivities of the cap layers obtained by simulation fully match known and published results.

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Chapter 4

The Analytical Models of Random Variations in FGMOSFET

Rawid Banchuin

4.1. Introduction

The Floating Gate MOSFET (FGMOSFET), has been extensively utilized in various electronic circuits range from a current mirror circuit to a neuromorphic sensor circuit [1-15]. Similarly to the MOSFET based circuits, the performance of the FGMOSFET based ones have also been deteriorated by process induced device level random variations [16, 17]. This is because these device level variations yield the random variations in circuit level parameters e.g. drain current and transconductance etc. Among various circuit level parameters, the drain current (I_D) has been found to be the key circuit level parameter of FGMOSFET as it is directly measurable and can be the basis for determining the others.

According to its importance, the analytical models of process induced random variation in I_D (ΔI_D) of the FGMOSFET have been proposed [18-25]. Some of the proposed models are statistical ones [18, 21-23] where the others are probabilistic modes [19, 20, 24, 25]. In this chapter, a revision of these models will be presented by starting with those models dedicated to the above 100 nm FGMOSFET [18-20] followed by the nanometer FGMOSFET dedicated models [21-25] respectively. Before we proceed further, a brief overview of FGMOSFET will be given in the subsequent section.

4.2. An Overview of FGMOSFET

FGMOSFET is a special type of MOSFET with an additional gate isolated within the oxide, namely the floating gate [18]. Since the FGMOSFET may employs multiple inputs, it can be also referred to as the Multiple Input Floating Gate MOSFET (MIFGMOSFET). A cross sectional view of an N-type FGMOSFET with N inputs where $N > 1$ can be depicted in Fig. 4.1 where its symbol and equivalent circuit have been depicted in Fig. 4.2. Such equivalent circuit is composed of a MOSFET, N input capacitances

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(C_1, C_2, C_3,…C_N), the overlap capacitance between floating-gate and drain (Cfd), overlap capacitance between floating-gate and source (C_{fs}) and parasitic capacitance between floating gate and substrate (C_{fb}) [18].

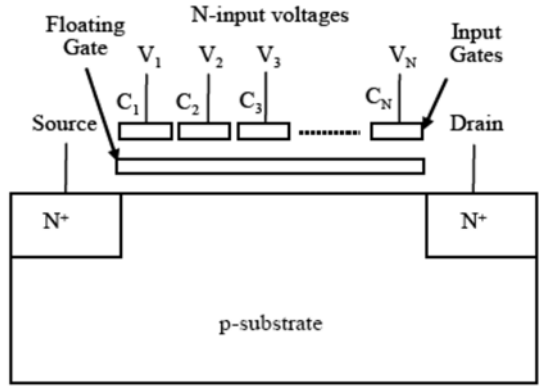

Fig. 4.1. A cross sectional view of N-type N inputs FGMOSFET [18].

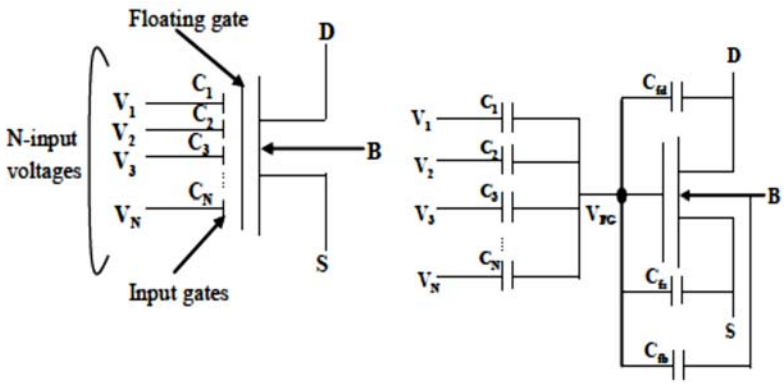

Fig. 4.2. The symbol (left) and equivalent circuit model (right) of an N-type N inputs FGMOSFET [18].

Let $\{i\} = \{1, 2, 3,\ldots, N\}$, the voltage at the floating gate voltage (V_{FG}) can be given by [18]

$$V_{FG} = \sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B, \tag{4.1}$$

where V_i, V_D, V_S and V_S denote the input voltage at any ith input, the drain voltage, the source voltage and the bulk voltage respectively. Note also that k_i, k_{fd}, k_{fs} and k_{fb} stand for the coupling factor of any ith input, drain, source and bulk and be respectively defined as

$$k_i = \frac{C_i}{\sum_{i=1}^{N}[C_i] + C_{fd} + C_{fs} + C_{fb}}, \tag{4.2}$$

$$k_{fd} = \frac{C_{fd}}{\sum_{i=1}^{N}[C_i] + C_{fd} + C_{fs} + C_{fb}}, \tag{4.3}$$

$$k_{fs} = \frac{C_{fs}}{\sum_{i=1}^{N}[C_i] + C_{fd} + C_{fs} + C_{fb}}, \tag{4.4}$$

$$k_{fb} = \frac{C_{fb}}{\sum_{i=1}^{N}[C_i] + C_{fd} + C_{fs} + C_{fb}} \tag{4.5}$$

By inspecting the equivalent circuit depicted in Fig. 4.2, it has been found that the equation of I_D of FGMOSFET can be obtained from that of the MOSFET by simply replacing the gate to source voltage (V_{GS}) in the equation of I_D of MOSFET by the voltage from floating gate to source (V_{FGS}) which can be found as

$$V_{FGS} = V_{FG} - V_S \tag{4.6}$$

4.3. The Above 100 nm FGMOSFET Dedicated Models

In this section, a revision of those models of ΔI_D of the above 100 nm FGMOSFET will be presented. The very first one have been proposed in 2015 [18]. In such work, both triode and saturation regions of operation have been considered. For the FGMOSFET in triode region, all coupling factors are functions of V_D as C_{fb} does thus these coupling factors can be alternatively given by [18]

$$k_i(V_D) = \alpha_{i0} + \alpha_{i1}V_D, \tag{4.7}$$

$$k_{fd}(V_D) = \alpha_{d0} + \alpha_{d1}V_D, \tag{4.8}$$

$$k_{fs}(V_D) = \alpha_{s0} + \alpha_{s1}V_D, \tag{4.9}$$

$$k_{fb}(V_D) = \alpha_{b0} + \alpha_{b1}V_D, \tag{4.10}$$

where α_{i0}, α_{d0}, α_{s0}, α_{b0} and α_{i1}, α_{d1}, α_{s1}, α_{b1} are the coefficients of the first two terms of the power series representation of $k_i(V_D)$, $k_{fd}(V_D)$, $k_{fs}(V_D)$ and $k_{fb}(V_D)$. As a result, V_{FG} can be given by (4.1) but with the coupling factors as given by (4.7)-(4.10).

For taking the second order effects such as mobility degradation and short channel effect etc., into account, the equations of I_D of MOSFET with linear model of mobility degradation [26] has been adopted as the basis. Hence, I_D of the FGMOSFET operated in triode region can be given by keeping in mind that $\alpha_{s0} + \alpha_{s1} V_D << 1$ as [18]

$$\begin{aligned} I_D = \beta[1\text{-}\theta(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_D - V_S - V_{TH})] \times \\ \times [(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_D - V_S - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2], \end{aligned} \tag{4.11}$$

where V_{TH}, β and θ denote the threshold voltage, current factor and mobility degradation coefficient respectively.

As a result, ΔI_D can be obtained as follows [18]

$$\begin{aligned} \Delta I_D = (\frac{\partial I_D}{\partial V_{TH}}) \Delta V_{TH} + (\frac{\partial I_D}{\partial \beta}) \Delta \beta + (\frac{\partial I_D}{\partial \theta}) \Delta \theta + (\frac{\partial I_D}{\partial \alpha_{d0}}) \Delta \alpha_{d0} + \\ + (\frac{\partial I_D}{\partial \alpha_{d1}}) \Delta \alpha_{d1} + (\frac{\partial I_D}{\partial \alpha_{b0}}) \Delta \alpha_{b0} + (\frac{\partial I_D}{\partial \alpha_{b1}}) \Delta \alpha_{b1} + \\ + \sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i0}}) \Delta \alpha_{i0}] + \sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i1}}) \Delta \alpha_{i1}], \end{aligned} \tag{4.12}$$

where ΔV_{TH}, $\Delta \alpha_{i0}$, $\Delta \alpha_{i1}$, $\Delta \alpha_{d0}$, $\Delta \alpha_{d1}$, $\Delta \alpha_{b0}$, $\Delta \alpha_{b1}$, $\Delta \beta$ and $\Delta \theta$ stand for the process induced device level random variation in V_{TH}, α_{i0}, α_{i1}, α_{d0}, α_{d1}, α_{b0}, α_{b1}, β and θ respectively. Note also that [18]

$$\begin{aligned} \frac{\partial I_D}{\partial V_{TH}} = \frac{\beta}{2} V_{DS}[4\theta(\alpha_{b1} V_B V_D + \alpha_{b0} V_B + (\alpha_{d0} + \alpha_{d1} V_D) V_D + \\ + \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i]) - \theta(4(V_S + V_{TH}) + V_{DS}) - 2]], \end{aligned} \tag{4.13}$$

$$\begin{aligned} \frac{\partial I_D}{\partial \beta} = [1\text{-}\theta(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_D - V_S - V_{TH})] \times \\ \times [(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_D - V_S - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2], \end{aligned} \tag{4.14}$$

$$\frac{\partial I_D}{\partial \theta} = \beta[V_S + V_{TH} - V_B(\alpha_{b0} + \alpha_{b1}V_D) - V_D(\alpha_{d0} + \alpha_{d1}V_D)) - \\ - \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1}V_D)V_i]][-\frac{1}{2}V_{DS}(V_{DS} + 2(V_S + V_{TH})) \\ + V_{DS}(\alpha_{b1}V_BV_D + \alpha_{b0}V_B + (\alpha_{d0} + \alpha_{d1}V_D)V_D + \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1}V_D)V_i]), \tag{4.15}$$

$$\frac{\partial I_D}{\partial \alpha_{d0}} = \frac{\beta}{2}V_DV_{DS}[2 + \theta V_{DS} + 4\theta(V_S + V_{TH}) - \\ - 4\theta[(\alpha_{b1}V_BV_D + \alpha_{b0}V_B + (\alpha_{d0} + \alpha_{d1}V_D)V_D + \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1}V_D)V_i]], \tag{4.16}$$

$$\frac{\partial I_D}{\partial \alpha_{b0}} = \frac{\beta}{2}V_BV_{DS}[2 + \theta V_{DS} + 4\theta(V_S + V_{TH}) - 4\theta[(\alpha_{b1}V_BV_D + \alpha_{b0}V_B + \\ + (\alpha_{d0} + \alpha_{d1}V_D)V_D + \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1}V_D)V_i]], \tag{4.17}$$

$$\frac{\partial \mathrm{I_D}}{\partial \alpha_{d1}} = \frac{\beta}{2}\mathrm{V_{DS}V_D^2}[2 + \theta \mathrm{V_{DS}} + 4\theta(V_S + V_{TH}) - \\ - 4\theta[(\alpha_{b1}V_BV_D + \alpha_{b0}V_B + (\alpha_{d0} + \alpha_{d1}V_D)V_D + \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1}V_D)\mathrm{V_i}]], \tag{4.18}$$

$$\frac{\partial \mathrm{I_D}}{\partial \alpha_{b1}} = \frac{\beta}{2}\mathrm{V_BV_DV_{DS}}[2 + \theta \mathrm{V_{DS}} + 4\theta(V_S + V_{TH}) - \\ - 4\theta[(\alpha_{b1}V_BV_D + \alpha_{b0}V_B + (\alpha_{d0} + \alpha_{d1}V_D)V_D + \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1}V_D)\mathrm{V_i}]], \tag{4.19}$$

$$\frac{\partial \mathrm{I_D}}{\partial \alpha_{i0}} = \frac{\beta}{2}\mathrm{V_{DS}}\sum_{i=1}^{N}[V_i][2 + \theta \mathrm{V_{DS}} + 4\theta(V_S + V_{TH}) - \\ - 4\theta[(\alpha_{b1}V_BV_D + \alpha_{b0}V_B + (\alpha_{d0} + \alpha_{d1}V_D)V_D + \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1}V_D)\mathrm{V_i}]], \tag{4.20}$$

$$\frac{\partial \mathrm{I_D}}{\partial \alpha_{i}} = \frac{\beta}{2}\mathrm{V_DV_{DS}}\sum_{i=1}^{N}[V_i][2 + \theta \mathrm{V_{DS}} + 4\theta(V_S + V_{TH}) - \\ - 4\theta[(\alpha_{b1}V_BV_D + \alpha_{b0}V_B + (\alpha_{d0} + \alpha_{d1}V_D)V_D + \sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1}V_D)\mathrm{V_i}]] \tag{4.21}$$

Since ΔV_{TH}, $\Delta\alpha_{i0}$, $\Delta\alpha_{i1}$, $\Delta\alpha_{d0}$, $\Delta\alpha_{d1}$, $\Delta\alpha_{b0}$, $\Delta\alpha_{b1}$, $\Delta\beta$ and $\Delta\theta$ are zero mean random variables, so does ΔI_D. However, ΔI_D employs nonzero variance. By using (4.12), the variance of ΔI_D $(\sigma^2_{\Delta I_D})$ of FGMOSFET in triode region can be found as [18]

$$\sigma^2_{\Delta I_D} = (\frac{\partial I_D}{\partial V_{TH}})^2 \sigma^2_{\Delta V_{TH}} + (\frac{\partial I_D}{\partial \beta})^2 \sigma^2_{\Delta\beta} + (\frac{\partial I_D}{\partial \theta})^2 \sigma^2_{\Delta\theta} + (\frac{\partial I_D}{\partial \alpha_{d0}})^2 \sigma^2_{\Delta\alpha_{d0}} + (\frac{\partial I_D}{\partial \alpha_{d1}})^2 \sigma^2_{\Delta\alpha_{d1}} +$$
$$+ (\frac{\partial I_D}{\partial \alpha_{b0}})^2 \sigma^2_{\Delta\alpha_{b0}} + (\frac{\partial I_D}{\partial \alpha_{b1}})^2 \sigma^2_{\Delta\alpha_{b1}} + \sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i0}})^2 \sigma^2_{\Delta\alpha_{i0}}] + \sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i1}})^2 \sigma^2_{\Delta\alpha_{i1}}] +$$
$$+ 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \beta})\rho_{\Delta V_{TH},\Delta\beta}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\beta}} + 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \theta})\rho_{\Delta V_{TH},\Delta\theta}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\theta}} +$$
$$+ 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \alpha_{d0}})\rho_{\Delta V_{TH},\Delta\alpha_{d0}}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\alpha_{d0}}} + 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \alpha_{d1}})\rho_{\Delta V_{TH},\Delta\theta}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\alpha_{d1}}} +$$
$$+ 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \alpha_{b0}})\rho_{\Delta V_{TH},\Delta\alpha_{d0}}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\alpha_{b0}}} + 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \alpha_{b1}})\rho_{\Delta V_{TH},\Delta\theta}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\alpha_{b1}}} +$$
$$+ 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \alpha_{i0}})\rho_{\Delta V_{TH},\Delta\alpha_{i0}}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}] +$$
$$+ 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \alpha_{i1}})\rho_{\Delta V_{TH},\Delta\alpha_{i1}}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}] + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \theta})\rho_{\Delta\beta,\Delta\theta}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\theta}} +$$
$$+ 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \alpha_{d0}})\rho_{\Delta\beta,\Delta\alpha_{d0}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\alpha_{d0}}} + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \alpha_{d1}})\rho_{\Delta\beta,\Delta\alpha_{d1}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\alpha_{d1}}} +$$
$$+ 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \alpha_{b0}})\rho_{\Delta\beta,\Delta\alpha_{b0}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\alpha_{b0}}} + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \alpha_{b1}})\rho_{\Delta\beta,\Delta\alpha_{b1}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\alpha_{b1}}} +$$
$$+ 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \alpha_{i0}})\rho_{\Delta\beta,\Delta\alpha_{i0}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}] + 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \alpha_{i1}})\rho_{\Delta\beta,\Delta\alpha_{i1}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}] +$$
$$+ 2(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial \alpha_{d0}})\rho_{\Delta\theta,\Delta\alpha_{d0}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta\alpha_{d0}}} + 2(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial \alpha_{d1}})\rho_{\Delta\theta,\Delta\alpha_{d1}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta\alpha_{d1}}} +$$
$$+ 2(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial \alpha_{b0}})\rho_{\Delta\theta,\Delta\alpha_{b0}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta\alpha_{b0}}} + 2(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial \alpha_{b1}})\rho_{\Delta\theta,\Delta\alpha_{b1}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta\alpha_{b1}}} +$$
$$+ 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial \alpha_{i0}})\rho_{\Delta\theta,\Delta\alpha_{i0}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}] + 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial \alpha_{i1}})\rho_{\Delta\theta,\Delta\alpha_{i1}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}] +$$
$$+ 2(\frac{\partial I_D}{\partial \alpha_{d0}})(\frac{\partial I_D}{\partial \alpha_{d1}})\rho_{\Delta\alpha_{d0},\Delta\alpha_{d1}}\sqrt{\sigma^2_{\Delta\alpha_{d0}}}\sqrt{\sigma^2_{\Delta\alpha_{d1}}} + 2(\frac{\partial I_D}{\partial \alpha_{d0}})(\frac{\partial I_D}{\partial \alpha_{b0}})\rho_{\Delta\alpha_{d0},\Delta\alpha_{b0}}\sqrt{\sigma^2_{\Delta\alpha_{d0}}}\sqrt{\sigma^2_{\Delta\alpha_{b0}}} +$$
$$+ 2(\frac{\partial I_D}{\partial \alpha_{d0}})(\frac{\partial I_D}{\partial \alpha_{b1}})\rho_{\Delta\alpha_{d0},\Delta\alpha_{b1}}\sqrt{\sigma^2_{\Delta\alpha_{d0}}}\sqrt{\sigma^2_{\Delta\alpha_{b1}}} + 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{d0}})(\frac{\partial I_D}{\partial \alpha_{i0}})\rho_{\Delta\alpha_{d0},\Delta\alpha_{i0}}\sqrt{\sigma^2_{\Delta\alpha_{d0}}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}] +$$
$$+ 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{d0}})(\frac{\partial I_D}{\partial \alpha_{i1}})\rho_{\Delta\alpha_{d0},\Delta\alpha_{i1}}\sqrt{\sigma^2_{\Delta\alpha_{d0}}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}] + 2(\frac{\partial I_D}{\partial \alpha_{d1}})(\frac{\partial I_D}{\partial \alpha_{b0}})\rho_{\Delta\alpha_{d1},\Delta\alpha_{b0}}\sqrt{\sigma^2_{\Delta\alpha_{d1}}}\sqrt{\sigma^2_{\Delta\alpha_{b0}}} +$$
$$+ 2(\frac{\partial I_D}{\partial \alpha_{d1}})(\frac{\partial I_D}{\partial \alpha_{b1}})\rho_{\Delta\alpha_{d1},\Delta\alpha_{b1}}\sqrt{\sigma^2_{\Delta\alpha_{d1}}}\sqrt{\sigma^2_{\Delta\alpha_{b1}}} + 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{d1}})(\frac{\partial I_D}{\partial \alpha_{i0}})\rho_{\Delta\alpha_{d1},\Delta\alpha_{i0}}\sqrt{\sigma^2_{\Delta\alpha_{d1}}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}] +$$

$$
\begin{aligned}
&+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{d1}})(\frac{\partial I_D}{\partial \alpha_{i1}})\rho_{\Delta\alpha_{d1},\Delta\alpha_{i1}}\sqrt{\sigma^2_{\Delta\alpha_{d1}}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}]+2(\frac{\partial I_D}{\partial \alpha_{b0}})(\frac{\partial I_D}{\partial \alpha_{b1}})\rho_{\Delta\alpha_{b0},\Delta\alpha_{b1}}\sqrt{\sigma^2_{\Delta\alpha_{b0}}}\sqrt{\sigma^2_{\Delta\alpha_{b1}}}+\\
&+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{b0}})(\frac{\partial I_D}{\partial \alpha_{i0}})\rho_{\Delta\alpha_{b0},\Delta\alpha_{i0}}\sqrt{\sigma^2_{\Delta\alpha_{b0}}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}]+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{b0}})(\frac{\partial I_D}{\partial \alpha_{i1}})\rho_{\Delta\alpha_{b0},\Delta\alpha_{i1}}\sqrt{\sigma^2_{\Delta\alpha_{b0}}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}]+\\
&+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{b1}})(\frac{\partial I_D}{\partial \alpha_{i0}})\rho_{\Delta\alpha_{b1},\Delta\alpha_{i0}}\sqrt{\sigma^2_{\Delta\alpha_{b1}}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}]+\\
&+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{b1}})(\frac{\partial I_D}{\partial \alpha_{i1}})\rho_{\Delta\alpha_{b1},\Delta\alpha_{i1}}\sqrt{\sigma^2_{\Delta\alpha_{b1}}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}]+\\
&+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i0}})(\frac{\partial I_D}{\partial \alpha_{i1}})\rho_{\Delta\alpha_{i0},\Delta\alpha_{i1}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}]+\\
&+\sum_{\substack{j=1\\ j\neq i}}^{N}\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i0}})(\frac{\partial I_D}{\partial \alpha_{j0}})\rho_{\Delta\alpha_{i0},\Delta\alpha_{j0}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}\sqrt{\sigma^2_{\Delta\alpha_{j0}}}]+\\
&+\sum_{j=1}^{N}\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i0}})(\frac{\partial I_D}{\partial \alpha_{j1}})\rho_{\Delta\alpha_{i0},\Delta\alpha_{j1}}\sqrt{\sigma^2_{\Delta\alpha_{i0}}}\sqrt{\sigma^2_{\Delta\alpha_{j1}}}]+\\
&+\sum_{j=1}^{N}\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i1}})(\frac{\partial I_D}{\partial \alpha_{j0}})\rho_{\Delta\alpha_{i1},\Delta\alpha_{j0}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}\sqrt{\sigma^2_{\Delta\alpha_{j0}}}]+\\
&+\sum_{\substack{j=1\\ j\neq i}}^{N}\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha_{i1}})(\frac{\partial I_D}{\partial \alpha_{j1}})\rho_{\Delta\alpha_{i1},\Delta\alpha_{j1}}\sqrt{\sigma^2_{\Delta\alpha_{i1}}}\sqrt{\sigma^2_{\Delta\alpha_{j1}}}],
\end{aligned}
\tag{4.22}
$$

where $\rho_{\Delta x,\Delta y}$ such as $\rho_{\Delta V_{TH},\Delta\beta}$, $\rho_{\Delta\beta,\Delta\theta}$ and $\rho_{\Delta V_{TH},\Delta\theta}$ etc., denotes the correlation coefficient of Δx and Δy. Moreover, $\sigma^2_{\Delta V_{TH}}$, $\sigma^2_{\Delta\beta}$, $\sigma^2_{\Delta\alpha_{i0}}$, $\sigma^2_{\Delta\alpha_{i1}}$, $\sigma^2_{\Delta\alpha_{d0}}$, $\sigma^2_{\Delta\alpha_{d1}}$, $\sigma^2_{\Delta\alpha_{b0}}$, $\sigma^2_{\Delta\alpha_{b1}}$, and $\sigma^2_{\Delta\theta}$ respectively denote the variances of ΔV_{TH}, $\Delta\alpha_{i0}$, $\Delta\alpha_{i1}$, $\Delta\alpha_{d0}$, $\Delta\alpha_{d1}$, $\Delta\alpha_{b0}$, $\Delta\alpha_{b1}$, $\Delta\beta$ and $\Delta\theta$.

For the FGMOSFET operates in saturation region on the other hand, the model formulation become simpler as the coupling factors are independent of V_D as C_{fb} does. So, V_{FG} can be solely given by (4.1) without referring to (4.7)-(4.10). Therefore the resulting I_D can be obtained by keeping in mind that $k_{fs} << 1$ as [18]

$$
\begin{aligned}
I_D = \frac{\beta}{2}(1+\lambda V_{DS})[1-\theta(\sum_{i=1}^{N}[k_i V_i]+k_{fd}V_D+k_{fb}V_B-V_S-\\
-V_{TH})](\sum_{i=1}^{N}[k_i V_i]+k_{fd}V_D+k_{fb}V_B-V_S-V_{TH})^2,
\end{aligned}
\tag{4.23}
$$

where λ stands for the channel length modulation coefficient.

By using (4.23), ΔI_D of FGMOSFET in the saturation region can be found as [18]

$$\Delta I_D = (\frac{\partial I_D}{\partial V_{TH}})\Delta V_{TH} + (\frac{\partial I_D}{\partial \beta})\Delta\beta + (\frac{\partial I_D}{\partial \theta})\Delta\theta + (\frac{\partial I_D}{\partial \lambda})\Delta\lambda + \\ + (\frac{\partial I_D}{\partial k_{fd}})\Delta k_{fd} + (\frac{\partial I_D}{\partial k_{fb}})\Delta k_{fb} + \sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_i})\Delta k_i], \tag{4.24}$$

where $\Delta\lambda$ is the process induced random variations in λ and [18]

$$\frac{\partial \mathrm{I_D}}{\partial \beta} = \frac{1+\lambda V_{DS}}{2}[1\text{-}\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - \\ - V_{TH})](\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH})^2, \tag{4.25}$$

$$\frac{\partial \mathrm{I_D}}{\partial \theta} = \frac{\beta}{2}(1+\lambda V_{DS})(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH})^3, \tag{4.26}$$

$$\frac{\partial \mathrm{I_D}}{\partial V_{TH}} = \frac{\beta}{2}(1+\lambda V_{DS})[3\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - \mathrm{V_S} - \\ - \mathrm{V_{TH}})\text{-}2](\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH}), \tag{4.27}$$

$$\frac{\partial \mathrm{I_D}}{\partial \lambda} = \frac{\beta}{2}V_{DS}[1\text{-}\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - \mathrm{V_S} - \\ - \mathrm{V_{TH}})](\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH})^2, \tag{4.28}$$

$$\frac{\partial \mathrm{I_D}}{\partial k_{fd}} = -\frac{\beta}{2}V_D(1+\lambda V_{DS})[3\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - \mathrm{V_S} - \\ - \mathrm{V_{TH}})\text{-}2](\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH}) \tag{4.29}$$

$$\frac{\partial \mathrm{I_D}}{\partial k_{fb}} = -\frac{\beta}{2}V_B(1+\lambda V_{DS})[3\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - \mathrm{V_S} - \\ - \mathrm{V_{TH}})\text{-}2](\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH}), \tag{4.30}$$

$$\frac{\partial \mathrm{I_D}}{\partial k_i} = -\frac{\beta}{2}(\sum_{i=1}^{N}[k_i V_i])(1+\lambda V_{DS})[3\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - \mathrm{V_S} - \\ - \mathrm{V_{TH}})\text{-}2](\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH}) \tag{4.31}$$

Since ΔV_{TH}, $\Delta\beta$, Δk_i, Δk_{fd}, Δk_{fb}, $\Delta\theta$ and $\Delta\lambda$ employ zero means, ΔI_D employs zero average. In addition, $\sigma^2_{\Delta I_D}$ can be derived in terms of $\sigma^2_{\Delta V_{TH}}$, $\sigma^2_{\Delta\beta}$, $\sigma^2_{\Delta k_i}$, $\sigma^2_{\Delta k_{fd}}$, $\sigma^2_{\Delta k_{fb}}$, $\sigma^2_{\Delta\theta}$ and $\sigma^2_{\Delta\lambda}$ where $\sigma^2_{\Delta k_i}$, $\sigma^2_{\Delta k_{fd}}$, $\sigma^2_{\Delta k_{fb}}$ and $\sigma^2_{\Delta\lambda}$ stand for the variances of Δk_i, Δk_{fd}, Δk_{fb} and $\Delta\lambda$ as given here by (4.32) [18]. Since $\sigma^2_{\Delta I_D}$ which is a statistical parameter has been highlighted, this model and the others with similar statistical parameter highlighting [21-23] can be referred to as the statistical models.

In order to verify the proposed model, the root mean square (rms.) value of ΔI_D calculated by using the model ($\Delta I_{D,rms,M}$) assuming that $N = 2$ has been compared to its SPICE BSIM3v3 based reference ($\Delta I_{D,rms,SPICE}$) obtained by using the Monte-Carlo SPICE simulation where a 0.25 μm level CMOS process technology of TSMC with all necessary parameters provided by MOSIS has been adopted [18]. The graphical results can be depicted here in Fig. 4.3-4.6 where strong agreements between $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ can be observed. The average deviations of $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ which are considerably very small [18], have been summarized here in Table 4.1. By these strong agreements and very small average deviations, the accuracy of the model has been verified.

$$
\begin{aligned}
\sigma^2_{\Delta I_D} = {} & (\frac{\partial I_D}{\partial V_{TH}})^2\sigma^2_{\Delta V_{TH}} + (\frac{\partial I_D}{\partial \beta})^2\sigma^2_{\Delta\beta} + (\frac{\partial I_D}{\partial \theta})^2\sigma^2_{\Delta\theta} + (\frac{\partial I_D}{\partial \lambda})^2\sigma^2_{\Delta\lambda} + (\frac{\partial I_D}{\partial k_{fb}})^2\sigma^2_{\Delta k_{fb}} + \\
& + (\frac{\partial I_D}{\partial k_{fd}})^2\sigma^2_{\Delta k_{fd}} + \sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_i})^2\sigma^2_{\Delta k_i}] + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial V_{TH}})\rho_{\Delta\beta,\Delta V_{TH}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta V_{TH}}} + \sqrt{a^2+b^2} + \\
& + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \theta})\rho_{\Delta\beta,\Delta\theta}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\theta}} + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial \lambda})\rho_{\Delta\beta,\Delta\lambda}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\lambda}} + \\
& + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial k_{fd}})\rho_{\Delta\beta,\Delta k_{fd}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta k_{fd}}} + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta\beta,\Delta k_{fb}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta k_{fb}}} + \\
& + 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta\beta,\Delta k_i}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta k_i}}] + 2(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial V_{TH}})\rho_{\Delta\theta,\Delta V_{TH}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta V_{TH}}} + \\
& + 2(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial \lambda})\rho_{\Delta\theta,\Delta\lambda}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta\lambda}} + 2(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial k_{fd}})\rho_{\Delta\theta,\Delta k_{fd}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta k_{fd}}} + \\
& + 2(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta\theta,\Delta k_{fb}}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta k_{fb}}} + 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \theta})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta\theta,\Delta k_i}\sqrt{\sigma^2_{\Delta\theta}}\sqrt{\sigma^2_{\Delta k_i}}] + \\
& + 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial \lambda})\rho_{\Delta V_{TH},\Delta\alpha_\lambda}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\lambda}} + 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial k_{fd}})\rho_{\Delta V_{TH},\Delta k_{fd}}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta k_{fd}}} + \\
& + 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta V_{TH},\Delta k_{fb}}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta\alpha k_{fb}}} + 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta V_{TH},\Delta k_i}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta k_i}}] + \\
& + 2(\frac{\partial I_D}{\partial \lambda})(\frac{\partial I_D}{\partial k_{fd}})\rho_{\Delta\lambda,\Delta k_{fd}}\sqrt{\sigma^2_{\Delta\lambda}}\sqrt{\sigma^2_{\Delta\alpha k_{fd}}} + 2(\frac{\partial I_D}{\partial \lambda})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta\lambda,\Delta k_{fb}}\sqrt{\sigma^2_{\Delta\lambda}}\sqrt{\sigma^2_{\Delta\alpha k_{fb}}} +
\end{aligned}
$$

$$+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \lambda})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta\lambda,\Delta k_i}\sqrt{\sigma^2_{\Delta\lambda}}\sqrt{\sigma^2_{\Delta k_i}}]+2(\frac{\partial I_D}{\partial k_{fd}})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta k_{fd},\Delta k_{fb}}\sqrt{\sigma^2_{\Delta k_{fd}}}\sqrt{\sigma^2_{\Delta\alpha k_{fb}}}+$$

$$+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_{fd}})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta k_{fd},\Delta k_i}\sqrt{\sigma^2_{\Delta k_{fd}}}\sqrt{\sigma^2_{\Delta k_i}}]+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_{fb}})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta k_{fb},\Delta k_i}\sqrt{\sigma^2_{\Delta k_{fb}}}\sqrt{\sigma^2_{\Delta k_i}}]+$$

$$+\sum_{\substack{j=1\\ j\neq i}}^{N}\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_i})(\frac{\partial I_D}{\partial k_j})\rho_{\Delta k_i,\Delta k_j}\sqrt{\sigma^2_{\Delta k_i}}\sqrt{\sigma^2_{\Delta k_j}}] \tag{4.32}$$

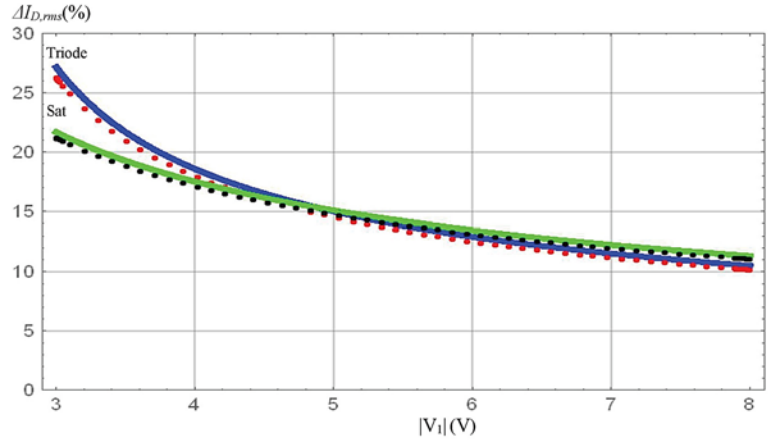

Fig. 4.3. The N-type FGMOSFET based $\Delta I_{D,rms,M}$ (normal line) and $\Delta I_{D,rms,SPICE}$ (dotted line) v.s. $|V_1|$ where $|V_2| = 0$ [18].

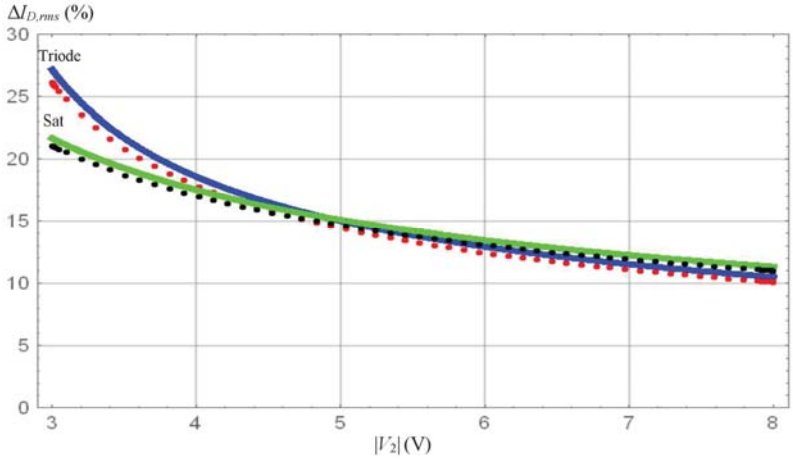

Fig. 4.4. The N-type FGMOSFET based $\Delta I_{D,rms,M}$ (normal line) and $\Delta I_{D,rms,SPICE}$ (dotted line) v.s. $|V_2|$ where $|V_2| = 0$ [18].

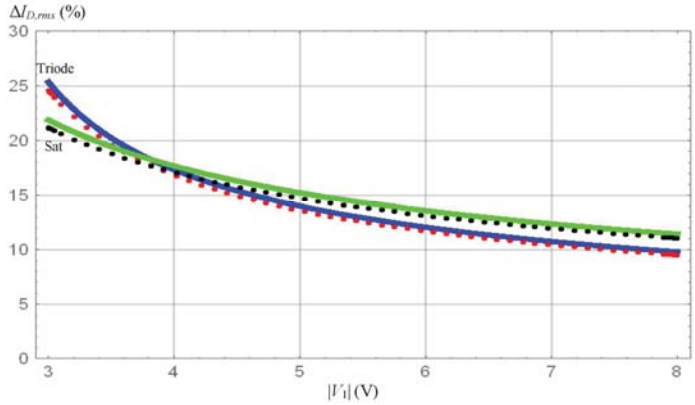

Fig. 4.5. The P-type FGMOSFET based $\Delta I_{D,rms,M}$ (normal line) and $\Delta I_{D,rms,SPICE}$ (dotted line) v.s. $|V_2|$ where $|V_2| = 0$ [18].

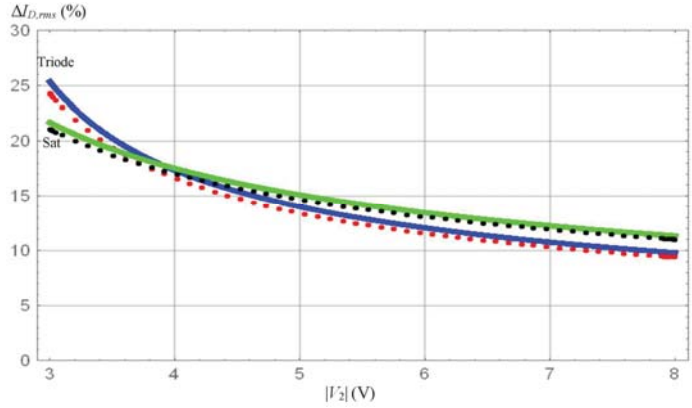

Fig. 4.6. The P-type FGMOSFET based $\Delta I_{D,rms,M}$ (normal line) and $\Delta I_{D,rms,SPICE}$ (dotted line) v.s. $|V_2|$ where $|V_2| = 0$ [18].

Table 4.1. The average deviations of $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ [18].

N-type		**P-type**	
Triode	Sat	Triode	Sat
3.74725 %	2.6901 %	3.70765 %	3.6681 %

Since ΔI_D is a random variable, its probabilistic distribution has also been found to be interesting. Therefore the probabilistic models of ΔI_D in term of the probability density functions of ΔI_D expressed in a per-unit basis ($\Delta I_D/I_D$) have been proposed [19, 20] where the random dopant fluctuation (RDF) and line edge roughness (LER) which are the significant sources of process induced random variation in CMOS technology [27], have been emphasized. For simplicity, the simplified equation of I_D of FGMOSFET in

saturation region as given by (4.33) has been adopted in [19]. Note also that $\beta = \mu C_{ox}\frac{W}{L}$, where μ, C_{ox}, W and L represent the mobility of the carriers, gate oxide capacitance per unit area, channel width and channel length respectively.

$$I_D = \frac{\mu}{2} C_{ox} \frac{W}{L} (\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})^2 \tag{4.33}$$

Based on (4.33), $\Delta I_D/I_D$ can be found as given by (4.34) where C_{inv}, N_{sub}, V_{FB}, W_{dep} and ϕ_F denote capacitance of the inversion layer, substrate doping concentration, flat band voltage, width of the depletion layer and Fermi potential respectively [19].

$$\frac{\Delta I_D}{I_D} = -2(\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})^{-1}(V_{TH} - qN_{sub}W_{dep}C_{inv}^{-1} - V_{FB} - 2\varphi_F) \tag{4.34}$$

For deriving the probability density function of $\Delta I_D/I_D$ ($f(\delta I_D/I_D)$) where $\delta I_D/I_D$ stands for the corresponding sample variable, the often cited analytical model of physical level nonidealities induced device level variation [27, 28] has been adopted. As a result, $f(\delta I_D/I_D)$ can be found as [19]

$$f(\frac{\delta I_D}{I_D}) = \frac{\sqrt{3WLC_{inv}}\sum_{i=1}^{N} k_i V_i - V_S - V_{TH}}{2\sqrt{2\pi N_{sub}W_{dep}}q} \exp\left[-\frac{3WLC_{inv}^2(\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})^2(\delta I_D / I_D)^2}{8N_{sub}W_{dep}q^2}\right] \tag{4.35}$$

However, only the model for saturation region operated FGMOSFET has been proposed in [19] where the short channel effect has been unfortunately overlooked. Therefore an improved model which taking these ignored issues into account, has been proposed in [20]. In such work, the simplified equations of I_D yet short channel effect included which can be given here by (4.36) and (4.37) for the FGMOSFET in triode and saturation region respectively [20], have been adopted as the basis.

$$I_D = \mu C_{ox}\frac{W}{L}[1-\theta(\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})][(\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2], \tag{4.36}$$

$$I_D = \frac{\mu}{2} C_{ox}\frac{W}{L}[1-\theta(\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})](\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})^2(1+\lambda V_{DS}) \tag{4.37}$$

As a result, $\Delta I_D/I_D$ and $f(\delta I_D/I_D)$ of triode region operated FGMOSFET can be found as [20]

$$\begin{aligned}\frac{\Delta I_D}{I_D} = \{&\theta[1-\theta(\sum_{i=1}^{N} k_i V_i - V_S - V_{THt})]^{-1} - V_{DS}[(\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})V_{DS} - \\ &-\frac{1}{2}V_{DS}^2]^{-1}\}(V_{TH} - qN_{sub}W_{dep}C_{inv}^{-1} - V_{FB} - 2\varphi_F),\end{aligned} \tag{4.38}$$

$$f(\frac{\delta I_D}{I_D}) = \\ = \sqrt{\frac{3WLC_{inv}^2\{\theta[1-\theta(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})]^{-1} - V_{DS}[(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]^{-1}\}^{-2}}{2\pi N_{sub}W_{dep}q^2}} \times \\ \times \exp[-\frac{3WLC_{inv}^2\{\{\theta[1-\theta(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})]^{-1} - V_{DS}[(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]^{-1}\}^{-1}(\frac{\delta I_D}{I_D})\}^2}{2N_{sub}W_{dep}q^2}]$$

(4.39)

On the other hand, those of the device in saturation region can be obtained as follows [20]

$$\frac{\Delta I_D}{I_D} = \{\theta[1-\theta(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})]^{-1} - \\ - 2(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})^{-1}\}(V_{TH} - qN_{sub}W_{dep}C_{inv}^{-1} - V_{FB} - 2\varphi_F),$$

(4.40)

$$f(\frac{\delta I_D}{I_D}) = \\ = \sqrt{\frac{3WLC_{inv}^2\{\theta[1-\theta(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})]^{-1} - V_{DS}[(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]^{-1}\}^{-2}}{2\pi N_{sub}W_{dep}q^2}} \times \\ \times \exp[-\frac{3WLC_{inv}^2\{\{\theta[1-\theta(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})]^{-1} - V_{DS}[(\sum_{i=1}^{N}k_iV_i - V_S - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2]^{-1}\}^{-1}(\frac{\delta I_D}{I_D})\}^2}{2N_{sub}W_{dep}q^2}]$$

(4.41)

In both [19] and [20], the model verifications have been performed based on 0.25 μm level CMOS process technology by comparing $f(\delta I_D / I_D)$ with the candidate FGMOSFET based probability distribution of $\Delta I_D/I_D$ ($f'(\delta I_D / I_D)$) obtained from the BSIM3v3 based Monte-Carlo simulations with 3000 runs and applying the Kolmogorov-Smirnof test (KS-test) which is a powerful goodness of fit test [29, 30], with 99 % confidence level. With such confidence level and number of runs, the critical value of the test can be given by 0.0297596 [19, 20]. The resulting values of KS-test statistic (*KS*) have been summarized here in Tables 4.2 and 4.3.

Table 4.2. Values of *KS* of the model proposed in [19].

N-type (Sat)	P-type (Sat)
0.02823	0.02619

Table 4.3. Values of *KS* of the model proposed in [20].

N-type		P-type	
Triode	Sat	Triode	Sat
0.01935	0.02013	0.01873	0.01895

Since these *KS*'s are lower than the critical value, the accuracies of the models have been verified. In addition, it has been found that the improved model [20] is more accurate than its predecessor [19] due to lower *KS*'s. The graphical comparisons of $f(\delta I_D / I_D)$ and $f'(\delta I_D / I_D)$ of such improved model can be depicted here in Figs. 4.7-4.10 where the strong agreements can be observed.

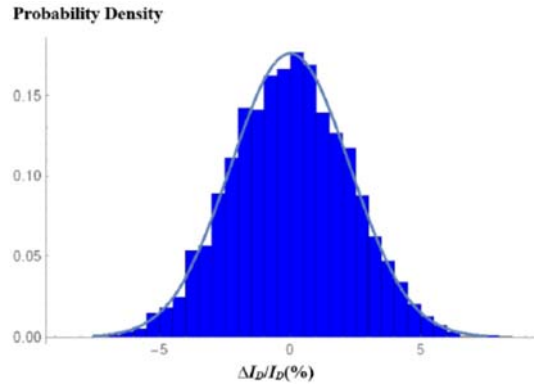

Fig. 4.7. The N-type triode region operated FGMOSFET based $f(\delta I_D / I_D)$ (line) and $f'(\delta I_D / I_D)$ (histogram) [20].

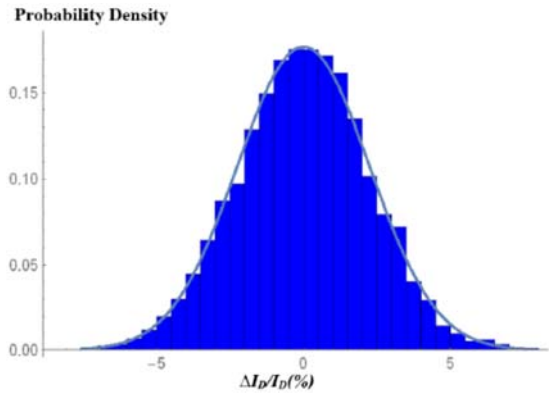

Fig. 4.8. The P-type triode region operated FGMOSFET based $f(\delta I_D / I_D)$ (line) and $f'(\delta I_D / I_D)$ (histogram) [20].

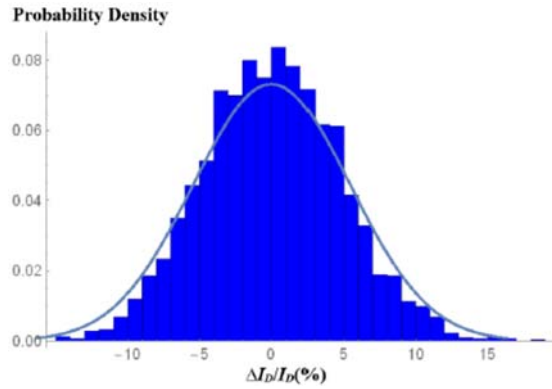

Fig. 4.9. The N-type saturation region operated FGMOSFET based $f(\delta I_D / I_D)$ (line) and $f'(\delta I_D / I_D)$ (histogram) [20].

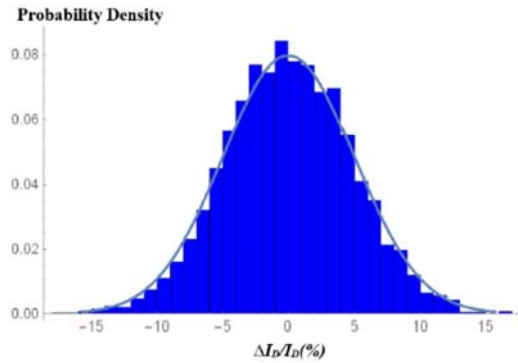

Fig. 4.10. The P-type saturation region operated FGMOSFET based $f(\delta I_D / I_D)$ (line) and $f'(\delta I_D / I_D)$ (histogram) [20].

4.4. The Nanometer FGMOSFET Dedicated Models

The very first modelling attempt for the nanometer FGMOSFET has been made in 2016 where the subthreshold device which its I_D can be given here by (4.42) where I_0, n, V_T and Q stand for the subthreshold specific current, subthreshold parameter, thermal voltage and charge stored on the floating gate per total capacitance of the floating gate respectively, has been used as the basis [21].

$$I_D = I_0 \frac{W}{L}\left[1-\exp\left[-\frac{V_{DS}}{V_T}\right]\right]\exp\left[\frac{\sum_{i=1}^{N}[k_i V_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B}{nV_T}-\frac{V_S}{V_T}+\frac{Q}{V_T}\right] \tag{4.42}$$

By using (4.42), $\Delta I_D/I_D$ can be found as [21]

$$\frac{\Delta I_D}{I_D}=\frac{\Delta I_0}{I_0}+\frac{\Delta W}{W}-\frac{\Delta L}{L}+\frac{Q}{\mathrm{V_T}}(\frac{\Delta Q}{Q})- \\ -\frac{\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B}{nV_T}(\frac{\Delta n}{n})+\frac{k_{fd}V_D}{nV_T}(\frac{\Delta k_{fd}}{k_{fd}})+ \\ +\frac{k_{fs}V_S}{nV_T}(\frac{\Delta k_{fs}}{k_{fs}})+\frac{k_{fb}V_B}{nV_T}(\frac{\Delta k_{fb}}{k_{fb}})+\sum_{i=1}^{N}\left[\frac{k_iV_i}{nV_T}(\frac{\Delta k_i}{k_i})\right], \tag{4.43}$$

where $\Delta W/W$, $\Delta L/L$, $\Delta Q/Q$, $\Delta n/n$, $\Delta I_0/I_0$, $\Delta k_{fd}/k_{fd}$, $\Delta k_{fs}/k_{fs}$, $\Delta k_{fb}/k_{fb}$ and $\Delta k_i/k_i$ are the per-unit random variations in W, L, Q, n, I_0, k_{fd}, k_{fs}, k_{fb} and k_i respectively.

As a result, the standard deviation of $\Delta I_D/I_D$ ($\sigma_{\Delta I_D/I_D}$) can be derived in terms of the variances of its contributors as given here by (4.44) [21]. For model verification, $\sigma_{\Delta I_D/I_D}$ has been compared with its Monte-Carlo SPICE simulation bases reference ($\sigma_{\Delta I_D/I_D}\big|_{SPICE}$), where $N = 2$ and the 65 nm level CMOS process technology have been assumed. The SPICE BSIM4 with all necessary SPICE parameters provided by PTM has been adopted [21]. The obtained results can be depicted here in Figs. 4.11 and 4.12 where strong agreements between $\sigma_{\Delta I_D/I_D}$ and $\sigma_{\Delta I_D/I_D}\big|_{SPICE}$ which are respectively displayed as normal and dotted lines, can be observed. The average errors which are very small [21], have been summarized here in Table 4.4. By these strong agreements and very small errors, the model's accuracy has been verified.

$$\sigma_{\frac{\Delta I_D}{I_D}}=\{\sigma^2_{\frac{\Delta I_0}{I_0}}+\sigma^2_{\frac{\Delta W}{W}}+\sigma^2_{\frac{\Delta L}{L}}+(\frac{Q}{V_T})^2\sigma^2_{\frac{\Delta Q}{Q}}+\left[\frac{1}{nV_T}\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B\right]^2\sigma^2_{\frac{\Delta n}{n}}+ \\ +(\frac{k_{fd}V_D}{nV_T})^2\sigma^2_{\sigma^2_{\frac{\Delta k_{fd}}{k_{fd}}}}+(\frac{k_{fs}V_S}{nV_T})^2\sigma^2_{\sigma^2_{\frac{\Delta k_{fs}}{k_{fs}}}}+(\frac{k_{fB}V_S}{nV_T})^2\sigma^2_{\sigma^2_{\frac{\Delta k_{fb}}{k_{fb}}}}+\sum_{i=1}^{N}\left[(\frac{k_iV_i}{nV_T})^2\sigma^2_{\frac{\Delta k_i}{k_i}}\right]+ \\ +2\rho_{\Delta I_0,\Delta W}\sqrt{\sigma^2_{\frac{\Delta I_0}{I_0}}}\sqrt{\sigma^2_{\frac{\Delta W}{W}}}-2\rho_{\Delta I_0,\Delta L}\sqrt{\sigma^2_{\frac{\Delta I_0}{I_0}}}\sqrt{\sigma^2_{\frac{\Delta L}{L}}}+\frac{2\rho_{\Delta I_0,\Delta Q}Q}{V_T}\sqrt{\sigma^2_{\frac{\Delta I_0}{I_0}}}\sqrt{\sigma^2_{\frac{\Delta Q}{Q}}} \\ -\frac{2\rho_{\Delta I_0,\Delta n}}{nV_T}(\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B)\sqrt{\sigma^2_{\frac{\Delta I_0}{I_0}}}\sqrt{\sigma^2_{\frac{\Delta n}{n}}}+2\rho_{\Delta I_0,\Delta k_{fd}}(\frac{k_{fd}V_D}{nV_T})\sqrt{\sigma^2_{\frac{\Delta I_0}{I_0}}}\sqrt{\sigma^2_{\frac{\Delta k_{fd}}{k_{fd}}}}+ \\ +2\rho_{\Delta I_0,\Delta k_{fs}}(\frac{k_{fs}V_S}{nV_T})\sqrt{\sigma^2_{\frac{\Delta I_0}{I_0}}}\sqrt{\sigma^2_{\frac{\Delta k_{fs}}{k_{fs}}}}+2\rho_{\Delta I_0,\Delta k_{fb}}(\frac{k_{fb}V_B}{nV_T})\sqrt{\sigma^2_{\frac{\Delta I_0}{I_0}}}\sqrt{\sigma^2_{\frac{\Delta k_{fb}}{k_{fb}}}}+ \\ -\frac{2\rho_{\Delta W,\Delta n}}{nV_T}(\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B)\sqrt{\sigma^2_{\frac{\Delta W}{W}}}\sqrt{\sigma^2_{\frac{\Delta n}{n}}}+2\rho_{\Delta W,\Delta k_{fd}}(\frac{k_{fd}V_D}{nV_T})\sqrt{\sigma^2_{\frac{\Delta W}{W}}}\sqrt{\sigma^2_{\frac{\Delta k_{fd}}{k_{fd}}}}+$$

$$+\sum_{i=1}^{N}\left[(\frac{2k_iV_i}{nV_T})\rho_{\Delta I_0,\Delta k_i}\sqrt{\sigma^2_{\frac{\Delta I_0}{I_0}}}\sqrt{\sigma^2_{\frac{\Delta k_i}{k_i}}}\right]-2\rho_{\Delta W,\Delta L}\sqrt{\sigma^2_{\frac{\Delta W}{W}}}\sqrt{\sigma^2_{\frac{\Delta L}{L}}}+\frac{2Q}{V_T}\rho_{\Delta W,\Delta Q}\sqrt{\sigma^2_{\frac{\Delta W}{W}}}\sqrt{\sigma^2_{\frac{\Delta Q}{Q}}}-$$

$$+2\rho_{\Delta W,\Delta k_{fs}}(\frac{k_{fd}V_S}{nV_T})\sqrt{\sigma^2_{\frac{\Delta W}{W}}}\sqrt{\sigma^2_{\frac{\Delta k_{fs}}{k_{fs}}}}+2\rho_{\Delta W,\Delta k_{fb}}(\frac{k_{fd}V_B}{nV_T})\sqrt{\sigma^2_{\frac{\Delta W}{W}}}\sqrt{\sigma^2_{\frac{\Delta k_{fb}}{k_{fb}}}}+\sum_{i=1}^{N}\left[(\frac{2k_iV_i}{nV_T})\rho_{\Delta W,\Delta k_i}\sqrt{\sigma^2_{\frac{\Delta W}{W}}}\sqrt{\sigma^2_{\frac{\Delta k_i}{k_i}}}\right]+$$

$$+\frac{2\rho_{\Delta L,\Delta n}}{nV_T}(\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B)\sqrt{\sigma^2_{\frac{\Delta L}{L}}}\sqrt{\sigma^2_{\frac{\Delta n}{n}}}-\frac{2Q}{V_T}\rho_{\Delta L,\Delta Q}\sqrt{\sigma^2_{\frac{\Delta L}{L}}}\sqrt{\sigma^2_{\frac{\Delta Q}{Q}}}-$$

$$-2\rho_{\Delta L,\Delta k_{fd}}(\frac{k_{fd}V_D}{nV_T})\sqrt{\sigma^2_{\frac{\Delta L}{L}}}\sqrt{\sigma^2_{\frac{\Delta k_{fd}}{k_{fd}}}}-2\rho_{\Delta L,\Delta k_{fs}}(\frac{k_{fs}V_S}{nV_T})\sqrt{\sigma^2_{\frac{\Delta L}{L}}}\sqrt{\sigma^2_{\frac{\Delta k_{fs}}{k_{fs}}}}-$$

$$-2\rho_{\Delta L,\Delta k_{fb}}(\frac{k_{fd}V_B}{nV_T})\sqrt{\sigma^2_{\frac{\Delta L}{L}}}\sqrt{\sigma^2_{\frac{\Delta k_{fb}}{k_{fb}}}}-\sum_{i=1}^{N}\left[(\frac{2k_iV_i}{nV_T})\rho_{\Delta L,\Delta k_i}\sqrt{\sigma^2_{\frac{\Delta L}{L}}}\sqrt{\sigma^2_{\frac{\Delta k_i}{k_i}}}\right]-$$

$$-2\rho_{\Delta n,\Delta Q}\frac{Q}{V_T}(\frac{\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B}{nV_T})\sqrt{\sigma^2_{\frac{\Delta n}{n}}}\sqrt{\sigma^2_{\frac{\Delta Q}{Q}}}-$$

$$-\frac{2\rho_{\Delta n,\Delta k_{fd}}k_{fd}V_D}{nV_T}(\frac{\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B}{nV_T})\sqrt{\sigma^2_{\frac{\Delta n}{n}}}\sqrt{\sigma^2_{\frac{\Delta k_{fd}}{k_{fd}}}}-$$

$$-\frac{2\rho_{\Delta n,\Delta k_{fs}}k_{fs}V_S}{nV_T}(\frac{\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B}{nV_T})\sqrt{\sigma^2_{\frac{\Delta n}{n}}}\sqrt{\sigma^2_{\frac{\Delta k_{fs}}{k_{fs}}}}-$$

$$-\frac{2\rho_{\Delta n,\Delta k_{fb}}k_{fb}V_B}{nV_T}(\frac{\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B}{nV_T})\sqrt{\sigma^2_{\frac{\Delta n}{n}}}\sqrt{\sigma^2_{\frac{\Delta k_{fb}}{k_{fb}}}}-$$

$$-\sum_{i=1}^{N}\left[\frac{2k_iV_i(\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B)}{(nV_T)^2}\rho_{\Delta n,\Delta k_i}\sqrt{\sigma^2_{\frac{\Delta n}{n}}}\sqrt{\sigma^2_{\frac{\Delta k_i}{k_i}}}\right] \tag{4.44}$$

For the nanometer FGMOSFET operates above the threshold level on the other hand, the alpha power law [31] which has been successfully applied to the variability analysis of nanometer MOSFET [32, 33], has been adopted as the modelling basis [22-25]. Therefore by keeping in mind that $k_{fs} << 1$, I_D of nanometer FGMOSFET operates in the saturation region can be found as [22]

$$I_D=\frac{\beta}{2}(\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fb}V_B-V_S-V_{TH})^{\alpha}, \tag{4.45}$$

where α stands for the velocity saturation index.

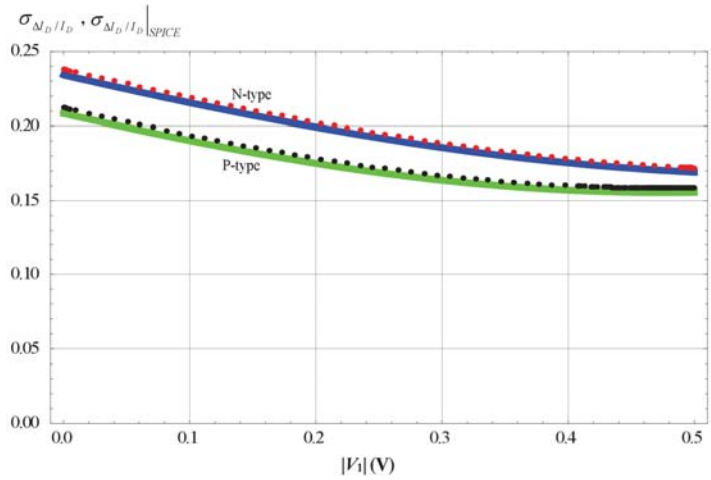

Fig. 4.11. The N-type and P-type subthreshold FGMOSFET based comparative plots against $|V_1|$, where $|V_2| = 0$ [21].

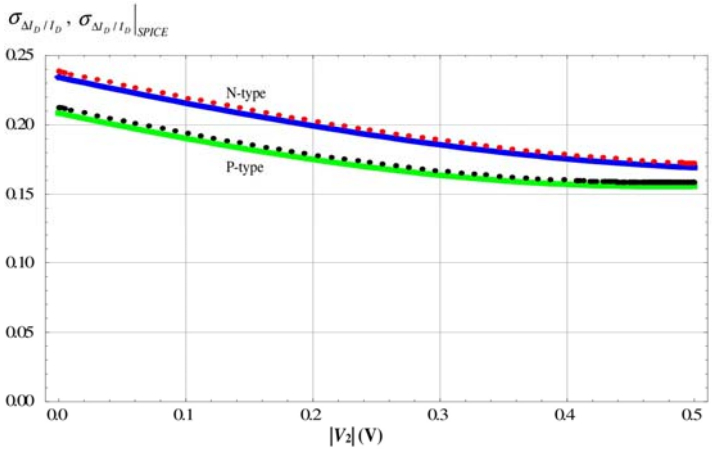

Fig. 4.12. The N-type and P-type subthreshold FGMOSFET based comparative plots against $|V_2|$, where $|V_1| = 0$ [21].

Table 4.4. Average errors of the model proposed in [21].

N-type		P-type	
$\|V_1\| = 0$	$\|V_2\| = 0$	$\|V_1\| = 0$	$\|V_2\| = 0$
1.8244 %	1.6245 %	1.9518 %	1.8904 %

As a result, ΔI_D of the above threshold nanometer FGMOSFET can be given by [22]

$$\Delta I_D = (\frac{\partial I_D}{\partial V_{TH}})\Delta V_{TH} + (\frac{\partial I_D}{\partial \alpha})\Delta\alpha + (\frac{\partial I_D}{\partial \beta})\Delta\beta + \\ + (\frac{\partial I_D}{\partial k_{fd}})\Delta k_{fd} + (\frac{\partial I_D}{\partial k_{fb}})\Delta k_{fb} + \sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_i})\Delta k_i], \tag{4.46}$$

where $\Delta\alpha$ denotes process induced device level random variation in α and

$$\frac{\partial I_D}{\partial V_{TH}} = -\frac{\alpha\beta}{2}(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH})^{\alpha-1}, \tag{4.47}$$

$$\frac{\partial I_D}{\partial \alpha} = \frac{\beta}{2}(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - \\ - V_{TH})^{\alpha}\ln[\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH}], \tag{4.48}$$

$$\frac{\partial I_D}{\partial \beta} = \frac{1}{2}(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH})^{\alpha}, \tag{4.49}$$

$$\frac{\partial I_D}{\partial k_{fd}} = \frac{\alpha\beta}{2}V_D(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH})^{\alpha-1}, \tag{4.50}$$

$$\frac{\partial I_D}{\partial k_{fb}} = \frac{\alpha\beta}{2}V_B(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH})^{\alpha-1}, \tag{4.51}$$

$$\frac{\partial I_D}{\partial k_i} = \frac{\alpha\beta}{2}V_i(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fb}V_B - V_S - V_{TH})^{\alpha-1} \tag{4.52}$$

Henceforth, it has been found that [22]

$$\sigma^2_{\Delta I_D} = (\frac{\partial I_D}{\partial V_{TH}})^2\sigma^2_{\Delta V_{TH}} + (\frac{\partial I_D}{\partial \alpha})^2\sigma^2_{\Delta\alpha} + (\frac{\partial I_D}{\partial \beta})^2\sigma^2_{\Delta\beta} + (\frac{\partial I_D}{\partial k_{fb}})^2\sigma^2_{\Delta k_{fb}} + (\frac{\partial I_D}{\partial k_{fd}})^2\sigma^2_{\Delta k_{fd}} + \\ + \sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_i})^2\sigma^2_{\Delta k_i}] + 2(\frac{\partial I_D}{\partial \alpha})(\frac{\partial I_D}{\partial V_{TH}})\rho_{\Delta\alpha,\Delta V_{TH}}\sqrt{\sigma^2_{\Delta\alpha}}\sqrt{\sigma^2_{\Delta V_{TH}}} + \\ + 2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial V_{TH}})\rho_{\Delta\beta,\Delta V_{TH}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta V_{TH}}} + \\ + 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial k_{fd}})\rho_{\Delta V_{TH},\Delta k_{fd}}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta k_{fd}}} + \sum_{\substack{j=1\\ j\neq i}}^{N}\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_i})(\frac{\partial I_D}{\partial k_j})\rho_{\Delta k_i,\Delta k_j}\sqrt{\sigma^2_{\Delta k_i}}\sqrt{\sigma^2_{\Delta k_j}}] + \\ + 2(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta V_{TH},\Delta k_{fb}}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta k_{fb}}} + 2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial V_{TH}})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta V_{TH},\Delta k_i}\sqrt{\sigma^2_{\Delta V_{TH}}}\sqrt{\sigma^2_{\Delta k_i}} +$$

$$+2(\frac{\partial I_D}{\partial \alpha})(\frac{\partial I_D}{\partial \beta})\rho_{\Delta\alpha,\Delta\beta}\sqrt{\sigma^2_{\Delta\alpha}}\sqrt{\sigma^2_{\Delta\beta}}+2(\frac{\partial I_D}{\partial \alpha})(\frac{\partial I_D}{\partial k_{fd}})\rho_{\Delta\alpha,\Delta k_{fd}}\sqrt{\sigma^2_{\Delta\alpha}}\sqrt{\sigma^2_{\Delta k_{fd}}}+$$
$$+2(\frac{\partial I_D}{\partial \alpha})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta\alpha,\Delta k_{fb}}\sqrt{\sigma^2_{\Delta\alpha}}\sqrt{\sigma^2_{\Delta k_{fb}}}+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \alpha})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta\alpha,\Delta k_i}\sqrt{\sigma^2_{\Delta\alpha}}\sqrt{\sigma^2_{\Delta k_i}}]+$$
$$+2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial k_{fd}})\rho_{\Delta\beta,\Delta k_{fd}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta k_{fd}}}+2(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta\beta,\Delta k_{fb}}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta\alpha k_{fb}}}+$$
$$+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial \beta})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta V_{TH},\Delta k_i}\sqrt{\sigma^2_{\Delta\beta}}\sqrt{\sigma^2_{\Delta k_i}}]+2(\frac{\partial I_D}{\partial k_{fd}})(\frac{\partial I_D}{\partial k_{fb}})\rho_{\Delta k_{fd},\Delta k_{fb}}\sqrt{\sigma^2_{\Delta k_{fd}}}\sqrt{\sigma^2_{\Delta\alpha k_{fb}}}+$$
$$+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_{fb}})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta k_{fb},\Delta k_i}\sqrt{\sigma^2_{\Delta k_{fb}}}\sqrt{\sigma^2_{\Delta k_i}}]+2\sum_{i=1}^{N}[(\frac{\partial I_D}{\partial k_{fd}})(\frac{\partial I_D}{\partial k_i})\rho_{\Delta k_{fd},\Delta k_i}\sqrt{\sigma^2_{\Delta k_{fd}}}\sqrt{\sigma^2_{\Delta k_i}}] \quad (4.53)$$

The accuracy of this very first model for the above threshold nanometer FGMOSFET has been verified by comparing the model based $\Delta I_{D,rms,M}$ to $\Delta I_{D,rms,SPICE}$ obtained by using Monte-Carlo simulation at nanometer level based on SPICE BSIM4. The resulting average deviation between $\Delta I_{D,rms,M}$ and $\Delta I_{D,rms,SPICE}$ has been found to be 5.65 % which is notably small. However, the triode region operated FGMOSFET has been unfortunately overlooked in [22].

Therefore an improved model has been proposed in [23] by also considering such formerly ignored triode region operated device. In addition, the effects of θ and λ have also been taken into account. By following [18] but without assuming that $\alpha_{s0}+\alpha_{s1}V_D << 1$, the alpha power law based I_D of FGMOSFET in triode region can be given by [23]

$$\begin{aligned} I_D = {} & \frac{\beta}{2}(\sum_{i=1}^{N}[(\alpha_{i0}+\alpha_{i1}V_D)V_i]+(\alpha_{d0}+\alpha_{d1}V_D)V_D+(\alpha_{s0}+\alpha_{s1}V_D)V_S+ \\ & +(\alpha_{b0}+\alpha_{b1}V_D)V_B-V_S-V_{TH})^{\alpha}[1-\theta(\sum_{i=1}^{N}[(\alpha_{i0}+\alpha_{i1}V_D)V_i]+ \\ & +(\alpha_{d0}+\alpha_{d1}V_D)V_D+(\alpha_{s0}+\alpha_{s1}V_D)V_S+ \\ & +(\alpha_{b0}+\alpha_{b1}V_D)V_B-V_S-V_{TH})](1+\lambda V_{DS})[\frac{2V_{DS}}{V_{DS,sat}}-(\frac{V_{DS}}{V_{DS,sat}})^2] \end{aligned} \quad (4.54)$$

Therefore the resulting $\Delta I_D/I_D$ can be found as [23]

$$\frac{\Delta I_D}{I_D}=S^{I_D}_{V_{DS,sat}}(\frac{\Delta V_{DS,sat}}{V_{DS,sat}})+S^{I_D}_{V_{TH}}(\frac{\Delta V_{TH}}{V_{TH}})+S^{I_D}_{\alpha}(\frac{\Delta\alpha}{\alpha})+$$
$$+S^{I_D}_{\beta}(\frac{\Delta\beta}{\beta})+S^{I_D}_{\theta}(\frac{\Delta\theta}{\theta})+S^{I_D}_{\lambda}(\frac{\Delta\lambda}{\lambda})+S^{I_D}_{\alpha}a_{\gamma_{d0}}(\frac{\Delta\alpha_{d0}}{\alpha_{d0}})+S^{I_D}_{\alpha_{d1}}(\frac{\Delta\alpha_{d1}}{\alpha_{d1}})+$$

$$+S_{\alpha_{s0}}^{I_D}(\frac{\Delta\alpha_{s0}}{\alpha_{s0}})+S_{\alpha_{s1}}^{I_D}(\frac{\Delta\alpha_{s1}}{\alpha_{s1}})+S_{\alpha_{b0}}^{I_D}(\frac{\Delta\alpha_{b0}}{\alpha_{b0}})+S_{\alpha_{b1}}^{I_D}(\frac{\Delta\alpha_{b1}}{\alpha_{b1}})+$$
$$+\sum_{i=1}^{N}[S_{\alpha_{i0}}^{I_D}(\frac{\Delta\alpha_{i0}}{\alpha_{i0}})]+\sum_{i=1}^{N}[S_{\alpha_{i1}}^{I_D}(\frac{\Delta\alpha_{i1}}{\alpha_{i1}})], \tag{4.55}$$

where $S_X^{I_D}$ and $\Delta X/X$ stand the sensitivity of I_D to X and the per-unit process induced random variation in X which in turn can be either V_{TH}, β, α_{i0}, α_{d0}, α_{s0}, α_{b0}, α_{i1}, α_{d1}, α_{s1}, α_{b1}, α, λ, θ or $V_{DS,sat}$. Note also that $S_\beta^{I_D}=1$ and [23]

$$S_{V_{DS,sat}}^{I_D}=-(1+\frac{V_{DS}}{V_{DS}-2V_{DS,sat}}), \tag{4.56}$$

$$\begin{aligned}S_{V_{TH}}^{I_D}=&V_{TH}\{-\theta[\theta(\sum_{i=1}^{N}[(\alpha_{i0}+\alpha_{i1}V_D)V_i]+(\alpha_{d0}+\alpha_{d1}V_D)V_D+(\alpha_{s0}+\alpha_{s1}V_D)V_S+\\&+(\alpha_{b0}+\alpha_{b1}V_D)V_B)-\theta V_S-\theta V_{TH}-1]^{-1}+\\&+\alpha[\sum_{i=1}^{N}[(\alpha_{i0}+\alpha_{i1}V_D)V_i]+(\alpha_{d0}+\alpha_{d1}V_D)V_D+(\alpha_{s0}+\alpha_{s1}V_D)V_S+\\&+(\alpha_{b0}+\alpha_{b1}V_D)V_B-V_S-V_{TH}]^{-1}\}V_D,\end{aligned} \tag{4.57}$$

$$\begin{aligned}S_{\alpha}^{I_D}=&\alpha\ln[\sum_{i=1}^{N}[(\alpha_{i0}+\alpha_{i1}V_D)V_i]+(\alpha_{d0}+\alpha_{d1}V_D)V_D+(\alpha_{s0}+\alpha_{s1}V_D)V_S+\\&+(\alpha_{b0}+\alpha_{b1}V_D)V_B-V_S-\mathrm{V_{TH}}],\end{aligned} \tag{4.58}$$

$$\begin{aligned}S_{\theta}^{I_D}=&[\theta(\sum_{i=1}^{N}[(\alpha_{i0}+\alpha_{i1}V_D)V_i]+(\alpha_{d0}+\alpha_{d1}V_D)V_D+(\alpha_{s0}+\alpha_{s1}V_D)V_S+\\&+(\alpha_{b0}+\alpha_{b1}V_D)V_B)-\theta V_S-\theta\mathrm{V_{TH}}-1]^{-1}+1,\end{aligned} \tag{4.59}$$

$$S_{\lambda}^{I_D}=\frac{\lambda V_{DS}}{1+\lambda V_{DS}}, \tag{4.60}$$

$$\begin{aligned}S_{\alpha_{d0}}^{I_D}=&\alpha_{d0}V_D\{\theta[\theta(\sum_{i=1}^{N}[(\alpha_{i0}+\alpha_{i1}V_D)V_i]+(\alpha_{d0}+\alpha_{d1}V_D)V_D+(\alpha_{s0}+\alpha_{s1}V_D)V_S+\\&+(\alpha_{b0}+\alpha_{b1}V_D)V_B)-\theta V_S-\theta\mathrm{V_{TH}}-1]^{-1}+\\&+\alpha[\sum_{i=1}^{N}[(\alpha_{i0}+\alpha_{i1}V_D)V_i]+(\alpha_{d0}+\alpha_{d1}V_D)V_D+(\alpha_{s0}+\alpha_{s1}V_D)V_S+\\&+(\alpha_{b0}+\alpha_{b1}V_D)V_B-V_S-\mathrm{V_{TH}}]^{-1}\},\end{aligned} \tag{4.61}$$

$$S_{\alpha_{s0}}^{I_D} = \alpha_{s0} V_S \{\theta[\theta(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B) - \theta V_S - \theta \mathrm{V_{TH}} - 1]^{-1} + \\ + \alpha[\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B - V_S - \mathrm{V_{TH}}]^{-1}\}, \tag{4.62}$$

$$S_{\alpha_{b0}}^{I_D} = \alpha_{b0} V_B \{\theta[\theta(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B) - \theta V_S - \theta \mathrm{V_{TH}} - 1]^{-1} + \\ + \alpha[\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B - V_S - \mathrm{V_{TH}}]^{-1}\}, \tag{4.63}$$

$$S_{\alpha_{d1}}^{I_D} = \alpha_{d1} V_D^2 \{\theta[\theta(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B) - \theta V_S - \theta \mathrm{V_{TH}} - 1]^{-1} + \\ + \alpha[\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B - V_S - \mathrm{V_{TH}}]^{-1}\} \tag{4.64}$$

$$S_{\alpha_{s1}}^{I_D} = \alpha_{s1} V_S \{\theta[\theta(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B) - \theta V_S - \theta \mathrm{V_{TH}} - 1]^{-1} + \\ + \alpha[\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B - V_S - \mathrm{V_{TH}}]^{-1}\} V_D, \tag{4.65}$$

$$S_{\alpha_{b1}}^{I_D} = \alpha_{b1} V_B \{\theta[\theta(\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B) - \theta V_S - \theta \mathrm{V_{TH}} - 1]^{-1} + \\ + \alpha[\sum_{i=1}^{N}[(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\ + (\alpha_{b0} + \alpha_{b1} V_D) V_B - V_S - \mathrm{V_{TH}}]^{-1}\} V_D, \tag{4.66}$$

$$
\begin{aligned}
S_{\alpha_{i0}}^{I_D} = \alpha_{i0} V_i \{ & \theta [\theta (\sum_{i=1}^{N} [(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\
& + (\alpha_{b0} + \alpha_{b1} V_D) V_B) - \theta V_S - \theta \mathrm{V_{TH}} - 1]^{-1} + \\
& + \alpha [\sum_{i=1}^{N} [(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\
& + (\alpha_{b0} + \alpha_{b1} V_D) V_B - V_S - \mathrm{V_{TH}}]^{-1} \},
\end{aligned}
\tag{4.67}
$$

$$
\begin{aligned}
S_{\alpha_{i1}}^{I_D} = \alpha_{i1} V_i \{ & \theta [\theta (\sum_{i=1}^{N} [(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\
& + (\alpha_{b0} + \alpha_{b1} V_D) V_B) - \theta V_S - \theta \mathrm{V_{TH}} - 1]^{-1} + \\
& + \alpha [\sum_{i=1}^{N} [(\alpha_{i0} + \alpha_{i1} V_D) V_i] + (\alpha_{d0} + \alpha_{d1} V_D) V_D + (\alpha_{s0} + \alpha_{s1} V_D) V_S + \\
& + (\alpha_{b0} + \alpha_{b1} V_D) V_B - V_S - \mathrm{V_{TH}}]^{-1} \} V_D
\end{aligned}
\tag{4.68}
$$

As a result, $\sigma_{\Delta I_D / I_D}$ can be analytically given by [23]

$$
\begin{aligned}
\sigma_{\frac{\Delta I_D}{I_D}} = \{ & (S_{V_{TH}}^{I_D})^2 \sigma^2_{\frac{\Delta V_{TH}}{V_{TH}}} + (S_{V_{DS,sat}}^{I_D})^2 \sigma^2_{\frac{\Delta V_{DS,sat}}{V_{DS,sat}}} + (S_{\alpha}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha}{\alpha}} + (S_{\beta}^{I_D})^2 \sigma^2_{\frac{\Delta \beta}{\beta}} + (S_{\theta}^{I_D})^2 \sigma^2_{\frac{\Delta \theta}{\theta}} + \\
& + (S_{\lambda}^{I_D})^2 \sigma^2_{\frac{\Delta \lambda}{\lambda}} + (S_{\alpha_{d0}}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}} + (S_{\alpha_{d1}}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha_{d1}}{\alpha_{d1}}} + (S_{\alpha_{s0}}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha_{s0}}{\alpha_{s0}}} + (S_{\alpha_{s1}}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha_{s1}}{\alpha_{s1}}} + \\
& + (S_{\alpha_{b0}}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha_{b0}}{\alpha_{b0}}} + (S_{\alpha_{b1}}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha_{b1}}{\alpha_{b1}}} + \sum_{i=1}^{N} [(S_{\alpha_{i0}}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha_{i0}}{\alpha_{i0}}}] + \sum_{i=1}^{N} [(S_{\alpha_{i1}}^{I_D})^2 \sigma^2_{\frac{\Delta \alpha_{i1}}{\alpha_{i1}}}] + \\
& + 2 \sum_{i=1}^{N} [S_{V_{TH}}^{I_D} S_{\alpha_{i1}}^{I_D} \rho_{\frac{\Delta V_{TH}}{V_{TH}}, \frac{\Delta \alpha_{i1}}{\alpha_{i1}}} \sigma_{\frac{\Delta V_{TH}}{V_{TH}}} \sigma_{\frac{\Delta \alpha_{i1}}{\alpha_{i1}}}] + 2 S_{\alpha_{d0}}^{I_D} S_{\alpha_{d1}}^{I_D} \rho_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}, \frac{\Delta \alpha_{d1}}{\alpha_{d1}}} \sigma_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}} \sigma_{\frac{\Delta \alpha_{d1}}{\alpha_{d1}}} + \\
& + 2 S_{\alpha_{d0}}^{I_D} S_{\alpha_{s0}}^{I_D} \rho_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}, \frac{\Delta \alpha_{s0}}{\alpha_{s0}}} \sigma_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}} \sigma_{\frac{\Delta \alpha_{s0}}{\alpha_{s0}}} + 2 S_{\alpha_{d0}}^{I_D} S_{\alpha_{s1}}^{I_D} \rho_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}, \frac{\Delta \alpha_{s1}}{\alpha_{s1}}} \sigma_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}} \sigma_{\frac{\Delta \alpha_{s1}}{\alpha_{s1}}} + \\
& + 2 S_{\alpha_{d0}}^{I_D} S_{\alpha_{b0}}^{I_D} \rho_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}, \frac{\Delta \alpha_{b0}}{\alpha_{b0}}} \sigma_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}} \sigma_{\frac{\Delta \alpha_{b0}}{\alpha_{b0}}} + 2 S_{\alpha_{d0}}^{I_D} S_{\alpha_{b1}}^{I_D} \rho_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}, \frac{\Delta \alpha_{b1}}{\alpha_{b1}}} \sigma_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}} \sigma_{\frac{\Delta \alpha_{b1}}{\alpha_{b1}}} + \\
& + 2 \sum_{i=1}^{N} [S_{\alpha_{d0}}^{I_D} S_{\alpha_{i0}}^{I_D} \rho_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}, \frac{\Delta \alpha_{i0}}{\alpha_{i0}}} \sigma_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}} \sigma_{\frac{\Delta \alpha_{i0}}{\alpha_{i0}}}] + 2 \sum_{i=1}^{N} [S_{\alpha_{d0}}^{I_D} S_{\alpha_{i1}}^{I_D} \rho_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}, \frac{\Delta \alpha_{i1}}{\alpha_{i1}}} \sigma_{\frac{\Delta \alpha_{d0}}{\alpha_{d0}}} \sigma_{\frac{\Delta \alpha_{i1}}{\alpha_{i1}}}] + \\
& + 2 S_{\alpha_{d1}}^{I_D} S_{\alpha_{s0}}^{I_D} \rho_{\frac{\Delta \alpha_{d1}}{\alpha_{d1}}, \frac{\Delta \alpha_{s0}}{\alpha_{s0}}} \sigma_{\frac{\Delta \alpha_{d1}}{\alpha_{d1}}} \sigma_{\frac{\Delta \alpha_{s0}}{\alpha_{s0}}} + \\
& + 2 S_{\alpha_{d1}}^{I_D} S_{\alpha_{s1}}^{I_D} \rho_{\frac{\Delta \alpha_{d1}}{\alpha_{d1}}, \frac{\Delta \alpha_{s1}}{\alpha_{s1}}} \sigma_{\frac{\Delta \alpha_{d1}}{\alpha_{d1}}} \sigma_{\frac{\Delta \alpha_{s1}}{\alpha_{s1}}} + 2 S_{\alpha_{d1}}^{I_D} S_{\alpha_{b0}}^{I_D} \rho_{\frac{\Delta \alpha_{d1}}{\alpha_{d1}}, \frac{\Delta \alpha_{b0}}{\alpha_{b0}}} \sigma_{\frac{\Delta \alpha_{d1}}{\alpha_{d1}}} \sigma_{\frac{\Delta \alpha_{b0}}{\alpha_{b0}}} +
\end{aligned}
$$

$$+2S_{\alpha_{d1}}^{I_D}S_{\alpha_{b1}}^{I_D}\rho_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}},\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}+2\sum_{i=1}^{N}[S_{\alpha_{d1}}^{I_D}S_{\alpha_{i0}}^{I_D}\rho_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}},\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}]+$$

$$+2\sum_{i=1}^{N}[S_{\alpha_{d1}}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+2\sum_{i=1}^{N}[S_{\alpha_{b0}}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\alpha_{b0}}{\alpha_{b0}},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+$$

$$+2S_{\alpha_{s0}}^{I_D}S_{\alpha_{s1}}^{I_D}\rho_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}},\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}+2S_{\alpha_{s0}}^{I_D}S_{\alpha_{b0}}^{I_D}\rho_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}},\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}+$$

$$+2S_{\alpha_{s0}}^{I_D}S_{\alpha_{b1}}^{I_D}\rho_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}},\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}+2\sum_{i=1}^{N}[S_{\alpha_{s0}}^{I_D}S_{\alpha_{i0}}^{I_D}\rho_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}},\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}]+$$

$$+2\sum_{i=1}^{N}[S_{\alpha_{s0}}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+\sum_{\substack{j=1\\j\neq i}}^{N}\sum_{i=1}^{N}[S_{\alpha_{i1}}^{I_D}S_{\alpha_{j1}}^{I_D}\rho_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}},\frac{\Delta\alpha_{j1}}{\alpha_{j1}}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\alpha_{j1}}{\alpha_{j1}}}]+$$

$$+2S_{V_{TH}}^{I_D}S_{\alpha_{b1}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}+2\sum_{i=1}^{N}[S_{V_{TH}}^{I_D}S_{\alpha_{i0}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}]+$$

$$+2S_{V_{TH}}^{I_D}S_{V_{DS,sat}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta V_{DS,sat}}{V_{DS,sat}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta V_{DS,sat}}{V_{DS,sat}}}+2S_{V_{TH}}^{I_D}S_{\alpha}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha}{\alpha}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha}{\alpha}}+$$

$$+2S_{V_{TH}}^{I_D}S_{\beta}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\beta}{\beta}}+2S_{V_{TH}}^{I_D}S_{\theta}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\theta}{\theta}}+$$

$$+2S_{V_{TH}}^{I_D}S_{\lambda}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\lambda}{\lambda}}+2S_{V_{TH}}^{I_D}S_{\alpha_{d0}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha_{d0}}{\alpha_{d0}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha_{d0}}{\alpha_{d0}}}+$$

$$+2S_{V_{TH}}^{I_D}S_{\alpha_{d1}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}+2S_{V_{TH}}^{I_D}S_{\alpha_{s0}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}+$$

$$+2S_{V_{TH}}^{I_D}S_{\alpha_{s1}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}+2S_{V_{TH}}^{I_D}S_{\alpha_{b0}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}+$$

$$+2\sum_{i=1}^{N}[S_{\alpha}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\alpha}{\alpha},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\alpha}{\alpha}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+2S_{\beta}^{I_D}S_{\theta}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\theta}{\theta}}+$$

$$+2S_{\theta}^{I_D}S_{\lambda}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\lambda}{\lambda}}+2S_{\theta}^{I_D}S_{\alpha_{d0}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\alpha_{d0}}{\alpha_{d0}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\alpha_{d0}}{\alpha_{d0}}}+$$

$$+2S_{\theta}^{I_D}S_{\alpha_{d1}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}+2S_{\theta}^{I_D}S_{\alpha_{s0}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}+$$

$$+2S_{\theta}^{I_D}S_{\alpha_{s1}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}+2S_{\theta}^{I_D}S_{\alpha_{b0}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}+$$

$$+2S_{\theta}^{I_D}S_{\alpha_{b1}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}+2\sum_{i=1}^{N}[S_{\theta}^{I_D}S_{\alpha_{i0}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}]+$$

$$+2S_{\beta}^{I_D}S_{\lambda}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\lambda}{\lambda}}+2S_{\beta}^{I_D}S_{\alpha_{d0}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\alpha_{d0}}{\alpha_{d0}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha_{d0}}{\alpha_{d0}}}+$$

$$
\begin{aligned}
&+2S_{\beta}^{I_D}S_{\alpha_{d1}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}+2S_{\beta}^{I_D}S_{\alpha_{s0}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}+\\
&+2S_{\beta}^{I_D}S_{\alpha_{s1}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}+2S_{\beta}^{I_D}S_{\alpha_{b0}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}+\\
&+2S_{\beta}^{I_D}S_{\alpha_{b1}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}+2\sum_{i=1}^{N}[S_{\beta}^{I_D}S_{\alpha_{i0}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}]+\\
&+2\sum_{i=1}^{N}[S_{\beta}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+2\sum_{i=1}^{N}[S_{\theta}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+\\
&+2S_{\lambda}^{I_D}S_{\alpha_{d0}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\alpha_{d0}}{\alpha_{d0}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha_{d0}}{\alpha_{d0}}}+2\sum_{i=1}^{N}[S_{\lambda}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+\\
&+2S_{\lambda}^{I_D}S_{\alpha_{d1}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha_{d1}}{\alpha_{d1}}}+2S_{\lambda}^{I_D}S_{\alpha_{s0}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha_{s0}}{\alpha_{s0}}}+\\
&+2S_{\lambda}^{I_D}S_{\alpha_{s1}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}+2S_{\lambda}^{I_D}S_{\alpha_{b0}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}+\\
&+2S_{\lambda}^{I_D}S_{\alpha_{b1}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}+2\sum_{i=1}^{N}[S_{\lambda}^{I_D}S_{\alpha_{i0}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}]+\\
&+2S_{\alpha_{s1}}^{I_D}S_{\alpha_{b0}}^{I_D}\rho_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}},\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta\alpha_{b0}}{\alpha_{b0}}}+2\sum_{i=1}^{N}[S_{\alpha_{s1}}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+\\
&+2S_{\alpha_{s1}}^{I_D}S_{\alpha_{b1}}^{I_D}\rho_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}},\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}+2\sum_{i=1}^{N}[S_{\alpha_{s1}}^{I_D}S_{\alpha_{i0}}^{I_D}\rho_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}},\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\alpha_{s1}}{\alpha_{s1}}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}]+\\
&+2\sum_{i=1}^{N}[S_{\alpha_{b1}}^{I_D}S_{\alpha_{i0}}^{I_D}\rho_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}},\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}]+2\sum_{i=1}^{N}[S_{\alpha_{b1}}^{I_D}S_{\alpha_{i1}}^{I_D}\rho_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}},\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\alpha_{b1}}{\alpha_{b1}}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}]+\\
&+\sum_{\substack{j=1\\ j\neq i}}^{N}\sum_{i=1}^{N}[S_{\alpha_{i0}}^{I_D}S_{\alpha_{j0}}^{I_D}\rho_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}},\frac{\Delta\alpha_{j0}}{\alpha_{j0}}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\alpha_{j0}}{\alpha_{j0}}}]+\sum_{j=1}^{N}\sum_{i=1}^{N}[S_{\alpha_{i0}}^{I_D}S_{\alpha_{j1}}^{I_D}\rho_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}},\frac{\Delta\alpha_{j1}}{\alpha_{j1}}}\sigma_{\frac{\Delta\alpha_{i0}}{\alpha_{i0}}}\sigma_{\frac{\Delta\alpha_{j1}}{\alpha_{j1}}}]+\\
&+\sum_{j=1}^{N}\sum_{i=1}^{N}[S_{\alpha_{i1}}^{I_D}S_{\alpha_{j0}}^{I_D}\rho_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}},\frac{\Delta\alpha_{j0}}{\alpha_{j0}}}\sigma_{\frac{\Delta\alpha_{i1}}{\alpha_{i1}}}\sigma_{\frac{\Delta\alpha_{j0}}{\alpha_{j0}}}]\}^{\frac{1}{2}}
\end{aligned}
\tag{4.69}
$$

For the device in saturation region on the other hand, its alpha power law based I_D can be obtained by following [18] yet without assuming that k_{fs} << 1as [23]

$$
\begin{aligned}
I_D=\frac{\beta}{2}(1+\lambda V_{DS})(&\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B-V_S-\\
&-V_{TH})^{\alpha}[1-\theta(\sum_{i=1}^{N}[k_iV_i]+k_{fd}V_D+k_{fs}V_S+k_{fb}V_B-V_S-V_{TH})]
\end{aligned}
\tag{4.70}
$$

Thus $\Delta I_D/I_D$ can be found as [23]

$$\frac{\Delta I_D}{I_D} = S_{V_{TH}}^{I_D}\left(\frac{\Delta V_{TH}}{V_{TH}}\right) + S_{\alpha}^{I_D}\left(\frac{\Delta \alpha}{\alpha}\right) + S_{\beta}^{I_D}\left(\frac{\Delta \beta}{\beta}\right) + S_{\theta}^{I_D}\left(\frac{\Delta \theta}{\theta}\right) + S_{\lambda}^{I_D}\left(\frac{\Delta \lambda}{\lambda}\right) + \\ + S_{k_{fd}}^{I_D}\left(\frac{\Delta k_{fd}}{k_{fd}}\right) + S_{k_{fs}}^{I_D}\left(\frac{\Delta k_{fs}}{k_{fs}}\right) + S_{k_{fb}}^{I_D}\left(\frac{\Delta k_{fb}}{k_{fb}}\right) + \sum_{i=1}^{N}\left[S_{k_i}^{I_D}\left(\frac{\Delta k_i}{k_i}\right)\right], \tag{4.71}$$

where X can now be either V_{TH}, β, k_i, k_{fd}, k_{fs}, k_{fb0}, α, λ or θ. Note also that $S_{\beta}^{I_D} = 1$ and [23]

$$S_{V_{TH}}^{I_D} = -V_{TH}\{\theta[\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}}) - 1]^{-1} + \\ + \alpha(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}})^{-1}\}, \tag{4.72}$$

$$S_{\alpha}^{I_D} = \alpha \ln[\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}}], \tag{4.73}$$

$$S_{\theta}^{I_D} = [\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}}) - 1]^{-1} + 1, \tag{4.74}$$

$$S_{\lambda}^{I_D} = \frac{\lambda V_{DS}}{1 + \lambda V_{DS}}, \tag{4.75}$$

$$S_{k_{fd}}^{I_D} = k_{fd}V_D\{\theta[\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}}) - 1]^{-1} + \\ + \alpha(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}})^{-1}\}, \tag{4.76}$$

$$S_{k_{fs}}^{I_D} = k_{fs}V_S\{\theta[\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}}) - 1]^{-1} + \\ + \alpha(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}})^{-1}\}, \tag{4.77}$$

$$S_{k_{fb}}^{I_D} = k_{fb}V_B\{\theta[\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}}) - 1]^{-1} + \\ + \alpha(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}})^{-1}\}, \tag{4.78}$$

$$S_{k_i}^{I_D} = k_i V_i \{\theta[\theta(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}}) - 1]^{-1} + \\ + \alpha(\sum_{i=1}^{N}[k_i V_i] + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - \mathrm{V_{TH}})^{-1}\}, \tag{4.79}$$

As a result, $\sigma_{\Delta I_D / I_D}$ can be given here by [23]

$$\sigma_{\frac{\Delta I_D}{I_D}} = \{(S_{V_{TH}}^{I_D})^2\sigma^2_{\frac{\Delta V_{TH}}{V_{TH}}} + (S_{\alpha}^{I_D})^2\sigma^2_{\frac{\Delta\alpha}{\alpha}} + (S_{\beta}^{I_D})^2\sigma^2_{\frac{\Delta\beta}{\beta}} + (S_{\alpha}^{I_D})^2\sigma^2_{\frac{\Delta\lambda}{\lambda}} + (S_{\theta}^{I_D})^2\sigma^2_{\frac{\Delta\theta}{\theta}} + (S_{k_{fb}}^{I_D})^2\sigma^2_{\frac{\Delta k_{fb}}{kfb}} + \\ + (S_{k_{fd}}^{I_D})^2\sigma^2_{\frac{\Delta k_{fd}}{k_{fd}}} + (S_{k_{fs}}^{I_D})^2\sigma^2_{\frac{\Delta k_{fs}}{k_{fs}}} + \sum_{i=1}^{N}[(S_{k_i}^{I_D})^2\sigma^2_{\frac{\Delta k_i}{k_i}}] + 2S_{V_{TH}}^{I_D}S_{\alpha}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\alpha}{\alpha}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\alpha}{\alpha}} + \\ + 2S_{V_{TH}}^{I_D}S_{\beta}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\beta}{\beta}} + 2S_{V_{TH}}^{I_D}S_{\theta}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\theta}{\theta}} + \\ + 2S_{V_{TH}}^{I_D}S_{\lambda}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta\lambda}{\lambda}} + 2S_{V_{TH}}^{I_D}S_{k_{fd}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta k_{fd}}{k_{fd}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta k_{fd}}{k_{fd}}} + \\ + 2S_{V_{TH}}^{I_D}S_{k_{fb}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta k_{fb}}{k_{fb}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta k_{fb}}{k_{fb}}} + 2S_{V_{TH}}^{I_D}S_{k_{fs}}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta k_{fs}}{k_{fs}}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta k_{fs}}{k_{fs}}} + \\ + 2\sum_{i=1}^{N}[S_{V_{TH}}^{I_D}S_{k_i}^{I_D}\rho_{\frac{\Delta V_{TH}}{V_{TH}},\frac{\Delta k_i}{k_i}}\sigma_{\frac{\Delta V_{TH}}{V_{TH}}}\sigma_{\frac{\Delta k_i}{k_i}}] + 2S_{\alpha}^{I_D}S_{\beta}^{I_D}\rho_{\frac{\Delta\alpha}{\alpha},\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\alpha}{\alpha}}\sigma_{\frac{\Delta\beta}{\beta}} +$$

$$+2S_{\alpha}^{I_D}S_{\lambda}^{I_D}\rho_{\frac{\Delta\alpha}{\alpha},\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\alpha}{\alpha}}\sigma_{\frac{\Delta\lambda}{\lambda}} + 2S_{\alpha}^{I_D}S_{k_{fd}}^{I_D}\rho_{\frac{\Delta\alpha}{\alpha},\frac{\Delta k_{fd}}{k_{fd}}}\sigma_{\frac{\Delta\alpha}{\alpha}}\sigma_{\frac{\Delta k_{fd}}{k_{fd}}} + \\ +2S_{\alpha}^{I_D}S_{k_{fb}}^{I_D}\rho_{\frac{\Delta\alpha}{\alpha},\frac{\Delta k_{fb}}{k_{fb}}}\sigma_{\frac{\Delta\alpha}{\alpha}}\sigma_{\frac{\Delta k_{fb}}{k_{fb}}} + 2S_{\alpha}^{I_D}S_{k_{fs}}^{I_D}\rho_{\frac{\Delta\alpha}{\alpha},\frac{\Delta k_{fs}}{k_{fs}}}\sigma_{\frac{\Delta\alpha}{\alpha}}\sigma_{\frac{\Delta k_{fs}}{k_{fs}}} + \\ +2S_{\beta}^{I_D}S_{\lambda}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\lambda}{\lambda}} + 2S_{\beta}^{I_D}S_{k_{fd}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta k_{fd}}{k_{fd}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta k_{fd}}{k_{fd}}} + \\ +2S_{\beta}^{I_D}S_{k_{fb}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta k_{fb}}{k_{fb}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta k_{fb}}{k_{fb}}} + 2S_{\beta}^{I_D}S_{k_{fs}}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta k_{fs}}{k_{fs}}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta k_{fs}}{k_{fs}}} + \\ +2S_{\beta}^{I_D}S_{\theta}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta\theta}{\theta}} + 2\sum_{i=1}^{N}[2S_{\beta}^{I_D}S_{k_i}^{I_D}\rho_{\frac{\Delta\beta}{\beta},\frac{\Delta k_i}{k_i}}\sigma_{\frac{\Delta\beta}{\beta}}\sigma_{\frac{\Delta k_i}{k_i}}] + \\ +2S_{\lambda}^{I_D}S_{\theta}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta\theta}{\theta}} + 2S_{\lambda}^{I_D}S_{k_{fd}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta k_{fd}}{k_{fd}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta k_{fd}}{k_{fd}}} + \\ +2S_{\lambda}^{I_D}S_{k_{fb}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta k_{fb}}{k_{fb}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta k_{fb}}{k_{fb}}} + 2S_{\lambda}^{I_D}S_{k_{fs}}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta k_{fs}}{k_{fs}}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta k_{fs}}{k_{fs}}} + \\ +2\sum_{i=1}^{N}[S_{\lambda}^{I_D}S_{k_i}^{I_D}\rho_{\frac{\Delta\lambda}{\lambda},\frac{\Delta k_i}{k_i}}\sigma_{\frac{\Delta\lambda}{\lambda}}\sigma_{\frac{\Delta k_i}{k_i}}] + 2S_{\theta}^{I_D}S_{k_{fd}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta k_{fd}}{k_{fd}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta k_{fd}}{k_{fd}}} +$$

$$+2S_{\theta}^{I_D}S_{k_{fb}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta k_{fb}}{k_{fb}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta k_{fb}}{k_{fb}}}+2S_{\theta}^{I_D}S_{k_{fs}}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta k_{fs}}{k_{fs}}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta k_{fs}}{k_{fs}}}+$$

$$+2\sum_{i=1}^{N}[S_{\theta}^{I_D}S_{k_i}^{I_D}\rho_{\frac{\Delta\theta}{\theta},\frac{\Delta k_i}{k_i}}\sigma_{\frac{\Delta\theta}{\theta}}\sigma_{\frac{\Delta k_i}{k_i}}]+2S_{k_{fd}}^{I_D}S_{k_{fb}}^{I_D}\rho_{\frac{\Delta k_{fd}}{k_{fd}},\frac{\Delta k_{fb}}{k_{fb}}}\sigma_{\frac{\Delta k_{fd}}{k_{fd}}}\sigma_{\frac{\Delta k_{fb}}{k_{fb}}}+$$

$$+2S_{k_{fd}}^{I_D}S_{k_{fs}}^{I_D}\rho_{\frac{\Delta k_{fd}}{k_{fd}},\frac{\Delta k_{fs}}{k_{fs}}}\sigma_{\frac{\Delta k_{fd}}{k_{fd}}}\sigma_{\frac{\Delta k_{fs}}{k_{fs}}}+2S_{k_{fb}}^{I_D}S_{k_{fs}}^{I_D}\rho_{\frac{\Delta k_{fb}}{k_{fb}},\frac{\Delta k_{fs}}{k_{fs}}}\sigma_{\frac{\Delta k_{fb}}{k_{fb}}}\sigma_{\frac{\Delta k_{fs}}{k_{fs}}}+$$

$$+2\sum_{i=1}^{N}[S_{k_{fd}}^{I_D}S_{k_i}^{I_D}\rho_{\frac{\Delta k_{fd}}{k_{fd}},\frac{\Delta k_i}{k_i}}\sigma_{\frac{\Delta k_{fd}}{k_{fd}}}\sigma_{\frac{\Delta k_i}{k_i}}]+2\sum_{i=1}^{N}[S_{k_{fb}}^{I_D}S_{k_i}^{I_D}\rho_{\frac{\Delta k_{fb}}{k_{fb}},\frac{\Delta k_i}{k_i}}\sigma_{\frac{\Delta k_{fb}}{k_{fb}}}\sigma_{\frac{\Delta k_i}{k_i}}]+$$

$$+\sum_{\substack{j=1\\j\neq i}}^{N}\sum_{i=1}^{N}[S_{k_i}^{I_D}S_{k_j}^{I_D}\rho_{\frac{\Delta k_i}{k_i},\frac{\Delta k_j}{k_j}}\sigma_{\frac{\Delta k_i}{k_i}}\sigma_{\frac{\Delta k_j}{k_j}}]\}^{\frac{1}{2}} \tag{4.80}$$

In [23], the model verification has been performed by comparing $\sigma_{\Delta I_D/I_D}$ to its reference ($\sigma_{\Delta I_D/I_D}\big|_{ref}$) obtained by using the Monte-Carlo simulation based on BSIM4 and 65 nm CMOS technology which is more deeply scaled than the 90 nm technology adopted in the previous work [22]. The graphical results can be displayed here in Fig. 4.13-4.16. By the graphically observed strong agreements and very small average deviations of $\sigma_{\Delta I_D/I_D}$ and $\sigma_{\Delta I_D/I_D}\big|_{ref}$ as summarized in Table 4.5, the accuracy of the model has been verified. In addition, this model is able to fit $\sigma_{\Delta I_D/I_D}\big|_{ref}$ obtained from a deeper scaled technological basis compared to that adopted in [22] because the formerly neglected θ and λ have been now taken into account.

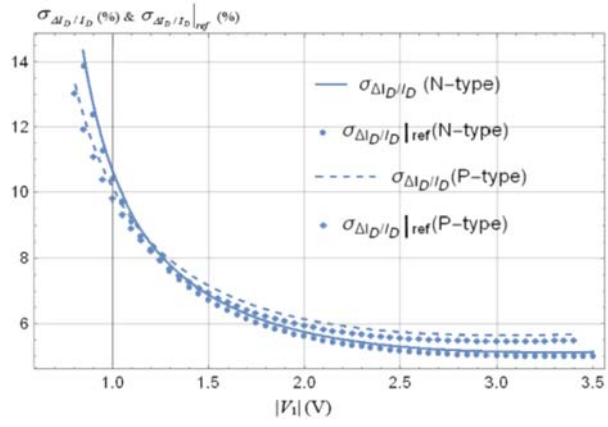

Fig. 4.13. The triode nanometer FGMOSFET based comparative plots against $|V_1|$, where $|V_2| = 0$ [23].

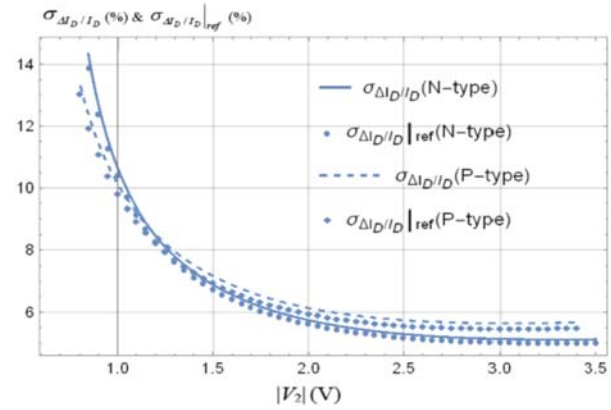

Fig. 4.14. The triode nanometer FGMOSFET based comparative plots against $|V_2|$, where $|V_1| = 0$ [23].

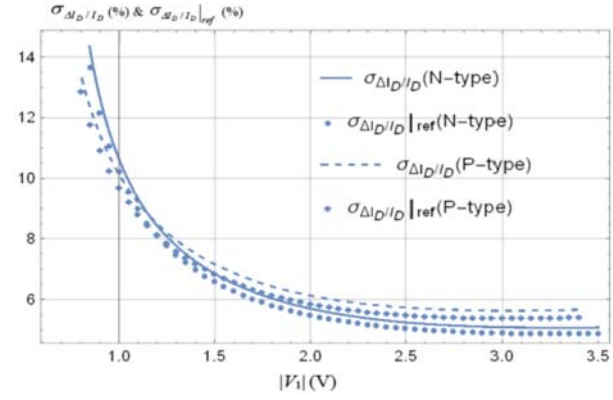

Fig. 4.15. The saturation nanometer FGMOSFET based comparative plots against $|V_1|$, where $|V_2| = 0$ [23].

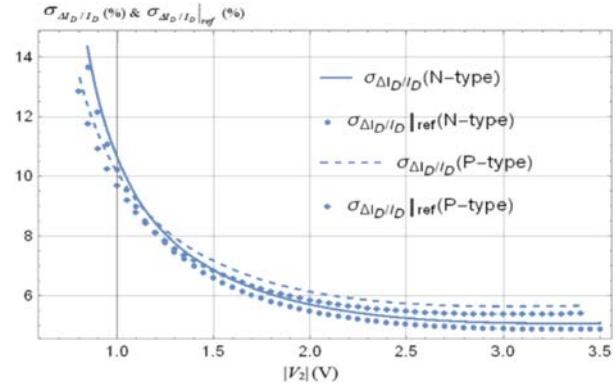

Fig. 4.16. The saturation nanometer FGMOSFET based comparative plots against $|V_2|$, where $|V_1| = 0$ [23].

Table 4.5. The average deviations of $\sigma_{\Delta I_D/I_D}$ and $\sigma_{\Delta I_D/I_D}\big|_{ref}$ [23].

N-type		P-type	
Triode	Sat	Triode	Sat
4.63 %	4.49 %	4.48 %	4.36 %

Beside the statistical models, the probabilistic models of ΔI_D of nanometer FGMOSFET have also been proposed in terms of $f(\delta I_D/I_D)$ where the RDF and LER have been once again emphasized [24, 25]. In [24], the simplified alpha power law based equations of I_D with k_{fd}, k_{fs} and k_{fb} neglected have been applied for simplicity. Such equations for FGMOSFET in triode and saturation regions can be respectively given by [24]

$$I_D = \beta\left[\frac{V_{DS}}{V_{DS,sat}} - \frac{1}{2}\left(\frac{V_{DS}}{V_{DS,sat}}\right)^2\right](\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})^{\alpha}, \tag{4.81}$$

$$I_D = \frac{\beta}{2}(\sum_{i=1}^{N} k_i V_i - V_S - V_{TH})^{\alpha} \tag{4.82}$$

As a result, $\Delta I_D/I_D$ can be commonly given for both regions as follows [24]

$$\frac{\Delta I_D}{I_D} = \frac{\alpha[2\varphi_F + C_{ox}^{-1}\sqrt{2qN_a(2\varphi_F + V_S - V_B)\varepsilon_s} - (V_{TH} - V_{FB})]}{\sum_{i=1}^{N} k_i V_i - V_S - V_{TH}}, \tag{4.83}$$

where N_a, V_{FB}, V_B, ε_s and ϕ_F denote accepter doping concentration, flat band voltage, body voltage, dielectric constant of Si and Fermi potential respectively. Thus $f(\delta I_D/I_D)$ can be found as [24]

$$f(\frac{\delta I_D}{I_D}) = \frac{\sum_{i=1}^{N} k_i V_i - V_S - V_t}{\alpha(2N_a(2\varphi_F + V_S - V_B)\varepsilon_s)^{0.25}} \times$$
$$\times\sqrt{\frac{3WLC_{ox}C_{inv}}{2\pi q^{1.5}}}\exp\left[-\frac{1.5WLC_{ox}C_{inv}(\sum_{i=1}^{N} k_i V_i - V_S - V_t)^2(\delta I_D / I_D)^2}{(2N_a(2\varphi_F + V_S - V_B)\varepsilon_s)^{0.5} q^{1.5}\alpha^2}\right] \tag{4.84}$$

Unfortunately, only the N-type FGMOSFET has been considered in [24]. Actually, the nanometer N-type and P-type devices employ different physical level and device level characteristics e.g. carrier type and noise immunity etc. [24]. Therefore an improved model which the P-type FGMOSFET, the effects of k_{fd}, k_{fs} and k_{fb} and the physical level differences of nanometer N-type and P-type devices have also been considered, has been proposed in [25]. Since k_{fd}, k_{fs} and k_{fb} have been now taken into account, I_D as given by (4.45) has been applied for the FGMOSFET in saturation region and [25]

$$I_D = \beta\left[\frac{V_{DS}}{V_{DS,sat}} - \frac{1}{2}\left(\frac{V_{DS}}{V_{DS,sat}}\right)^2\right](\sum_{i=1}^{N} k_i V_i + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - V_{TH})^{\alpha} \quad (4.85)$$

has been used as the basis for the triode region device.

As a result, it has been found that [25]

$$\frac{\Delta I_{DN}}{I_{DN}} = \frac{\alpha[2\varphi_F + C_{ox}^{-1}\sqrt{2qN_a(2\varphi_F + V_S - V_B)\varepsilon_s} - (V_{TH} - V_{FB})]}{\sum_{i=1}^{N} k_i V_i + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - V_{TH}}, \quad (4.86)$$

$$\frac{\Delta I_{DP}}{I_{DP}} = \frac{\alpha[2|\varphi_F| + C_{ox}^{-1}\sqrt{2qN_d(2|\varphi_F| - V_S + V_B)\varepsilon_s} + (V_{TH} - V_{FB})]}{V_S + V_{TH} - \sum_{i=1}^{N} k_i V_i - k_{fd}V_D - k_{fs}V_S - k_{fb}V_B}, \quad (4.87)$$

for the FGMOSFET in either triode region or saturation region. Note that $\Delta I_{DN}/I_{DN}$, $\Delta I_{DP}/I_{DP}$ and N_d denotes $\Delta I_D/I_D$ of N-type and P-type FGMOSFET and the donor doping concentration respectively.

Thus we have the following probability density functions for N-type and P-type FGMOSFET [25]

$$f_N(\frac{\delta I_{DN}}{I_{DN}}) = \frac{\sum_{i=1}^{N} k_i V_i + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - V_{TH}}{\alpha(2N_a(2\varphi_F + V_S - V_B)\varepsilon_s)^{0.25}}\sqrt{\frac{3WLC_{ox}C_{inv}}{2\pi q^{1.5}}} \times$$
$$\times \exp\left[-\frac{1.5WLC_{ox}C_{inv}(\sum_{i=1}^{N} k_i V_i + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - V_{TH})^2(\frac{\delta I_{DN}}{I_{DN}})^2}{(2N_a(2\varphi_F + V_S - V_B)\varepsilon_s)^{0.5}q^{1.5}\alpha^2}\right], \quad (4.88)$$

$$f_P(\frac{\delta I_{DP}}{I_{DP}}) = \frac{\sum_{i=1}^{N} k_i V_i + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - V_{TH}}{\alpha(2N_d(2|\varphi_F| - V_S + V_B)\varepsilon_s)^{0.25}}\sqrt{\frac{3WLC_{ox}C_{inv}}{2\pi q^{1.5}}} \times$$
$$\times \exp\left[-\frac{1.5WLC_{ox}C_{inv}(\sum_{i=1}^{N} k_i V_i + k_{fd}V_D + k_{fs}V_S + k_{fb}V_B - V_S - V_{TH})^2(\frac{\delta I_{DP}}{I_{DP}})^2}{(2N_d(2|\varphi_F| - V_S + V_B)\varepsilon_s)^{0.5}q^{1.5}\alpha^2}\right] \quad (4.89)$$

where $\delta I_{DN}/I_{DN}$ and $\delta I_{DP}/I_{DP}$, stand for the sample variable equivalents of $\Delta I_{DN}/I_{DN}$ and $\Delta I_{DP}/I_{DP}$, respectively.

In both [24] and [25], the model verifications have been performed by the comparison of the derived probability density functions with their SPICE BSIM4 based references obtained by using Monte-Carlo simulations with 3000 runs and the KS-test with 99 % confidence level. Thus the critical value is given by 0.0297596. The *KS*'s can be summarized here in Tables 4.6 and 4.7 where it has been found that the improved model proposed in [25] is more accurate than its predecessor [24]. This is because k_{fd}, k_{fs} and k_{fb} have been taken into account. The graphical comparisons of $f_N(\delta I_{DN}/I_{DN})$ and $f_P(\delta I_{DP}/I_{DP})$ with their SPICE BSIM4 based references ($g_N(\delta I_{DN}/I_{DN})$ and $g_P(\delta I_{DP}/I_{DP})$) can be depicted here in Figs. 4.17-4.20 where strong agreements can be observed.

Table 4.6. Values of *KS* of the model proposed in [24].

Triode (N-type)	Sat (N-type)
0.024671	0.026817

Table 4.7. Values of *KS* of the model proposed in [25].

N-type		P-type	
Triode	Sat	Triode	Sat
0.01832	0.01941	0.01866	0.01891

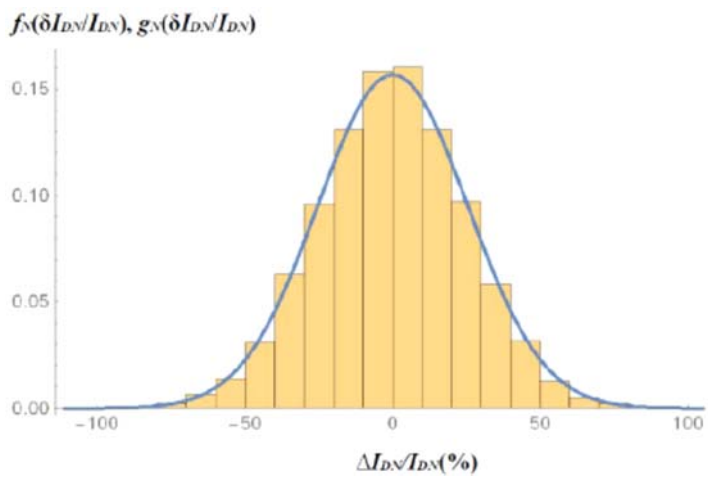

Fig. 4.17. The triode region operated nanometer FGMOSFET based $f_N(\delta I_{DN}/I_{DN})$ (line) and $g_N(\delta I_{DN}/I_{DN})$ (histogram) [25].

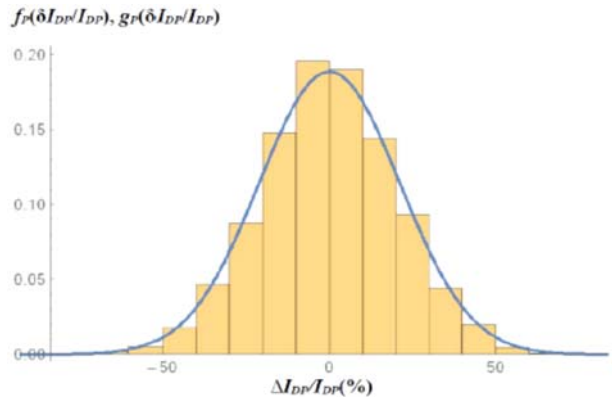

Fig. 4.18. The triode region operated nanometer FGMOSFET based $f_P(\delta I_{DP}/I_{DP})$ (line) and $g_P(\delta I_{DP}/I_{DP})$ (histogram) [25].

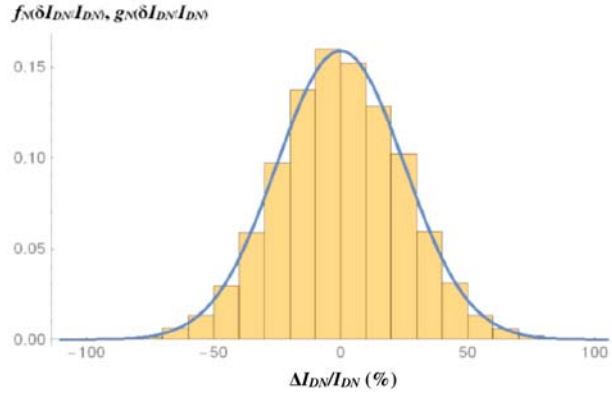

Fig. 4.19. The saturation region operated nanometer FGMOSFET based $f_N(\delta I_{DN}/I_{DN})$ (line) and $g_N(\delta I_{DN}/I_{DN})$ (histogram) [25].

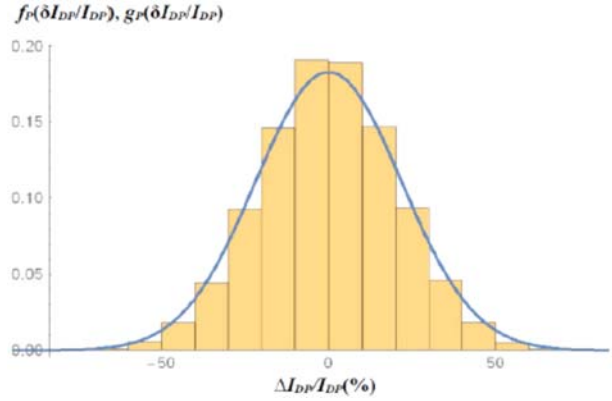

Fig. 4.20. The saturation region operated nanometer FGMOSFET based $f_P(\delta I_{DP}/I_{DP})$ (line) and $g_P(\delta I_{DP}/I_{DP})$ (histogram) [25].

4.5. Concluding Remarks

Thus far a revision of the models of ΔI_D of FGMOSFET [18-25] has been presented where the subthreshold FGMOSFET has been focused in [21]. For those above threshold FGMOSFET dedicated models, the probabilistic ones [19, 20, 24, 25] are mathematically superior to their statistical counterparts [18, 22, 23]. This is because they are in terms of the probability density functions thus any statistical parameter not limited to only the standard deviation and variance, can be obtained by simply applying the mathematical statistic. However only ΔV_{TH} and $\Delta\beta$ have been focused in these probabilistic models as merely RDF and LER have been emphasized as stated above. On the other hand, all related process induced device level random variations and their statistical correlations have been focused in those statistical models which in turn become their advantages over the probabilistic ones. At this point, it can be seen that the probabilistic modelling of ΔI_D of nanometer subthreshold FGMOSFET has been left untouched and thus has been found to be an interesting open research question.

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Chapter 5

Effective Young's Modulus of Electrodeposited Gold for Design of MEMS Accelerometers

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5.1. Introduction

Performance of a microelectromechanical systems (MEMS) accelerometer is largely affected by thermal-mechanical noises, such as the Brownian noise. An example of a MEMS accelerometer is shown in Fig. 5.1 [1]. The Brownian noise is inversely proportional to overall weight of the key components [2], hence low noise and high sensitivity can be achieved by increasing overall mass of the key components. Though, continuous miniaturization of MEMS devices is another important task, and the size of the key component is a crucial factor limiting dimensions of a MEMS device. One solution to realize high performance (low noise) and the miniaturization simultaneously is through utilization of high-density materials in the key component. MEMS accelerometers are conventionally composed of Si-based materials [3]. Density of pure gold (19.3 g/cm^3) is about 10 times higher than that of silicon (2.3 g/cm^3), and gold materials are commonly used in electronic devices due to the high electrical conductivity, chemical stability, corrosion resistance, and ductility [4]. In addition, micro-components composed of gold-based materials can be fabricated by electrodeposition, and electrodeposition process can be easily integrated with MEMS fabrication processes. In fact, application of gold-based micro-components in MEMS accelerometers is reported to have sub 1g (g = 9.8 m/s^2) sensing performance and low Brownian noise at 0.78 μg/√Hz [2].

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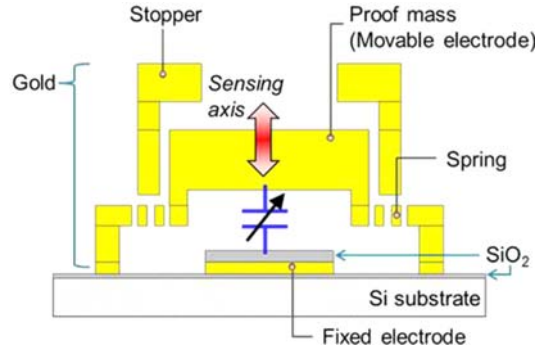


Fig. 5.1. Schematic design of a gold-based MEMS accelerometer.

In the design of MEMS components, mechanical properties of the material are important parameters affecting the structure stability [1, 5-7] and overall reliability of the MEMS device. On the other hand, the mechanical property could change with the shape or dimension of the component [8-11]. For instance, Young's modulus is an intrinsic property of materials, but Young's modulus of micro-components composed of the same material could change when the geometry varies [8-16]. The Young's modulus obtained for a specimen with a specific geometry is called effective Young's modulus (E_e). Therefore, effective Young's modulus evaluation of specimens with various geometry in micrometer scale is required for the design of MEMS components.

The effective Young's modulus of cantilever-type specimens can be evaluated by a non-destructive resonance frequency method [15-18]. The resonance frequency (f_c) is determined from damping oscillations of the cantilever measured by a laser Doppler, and vibrations of the cantilever are achieved by applying a pulse voltage between a fixed electrode and the cantilever. The effective Young's modulus is calculated using the following equation:

$$f_c = 0.162 \frac{t}{L^2} \sqrt{\frac{E_e}{\rho}}, \tag{5.1}$$

where L is the length of a micro-cantilever, t is the thickness, and ρ is the density. Through preparation of cantilevers with various lengths and measurement of the resonance frequencies, a plot of f_c versus $1/L^2$ can be prepared, and the asymptote should a straight line with a positive slope. Then the effective Young's modulus can be calculated from the slope of the asymptote.

As indicated in Eq. (5.1), the resonance frequency is linearly related to the thickness of a micro-cantilever and assumed to be independent of the width. In a resonance frequency measurement, the vibration direction of a cantilever would be parallel to the thickness direction of the cantilever and perpendicular to the width direction. Also, the yield strength of cantilevers in micro-meter order is reported to be dependent on the sample geometry [10, 19-21]. Therefore, it is necessary to confirm effects of the geometry on the effective Young's modulus. In this chapter, the width dependency of the effective Young's modulus

of gold-based micro-cantilevers is investigated by the resonance frequency method and FEM (finite element method) simulations to provide information for design of MEMS components.

5.2. Effective Young's Modulus of Gold Micro-cantilevers by Resonance Frequency Method

Fig. 5.2 shows a schematic view of the pure gold micro-cantilever evaluated in this study. The titanium layer was formed by evaporation to be used as the adhesive layer on the SiO_2 layer. Then a thin layer of gold was evaporated to be used as the seed layer in the gold electrodeposition. A series of lithography and electrodeposition processes was conducted to fabricate the micro-cantilevers. More details of the lithography and electrodeposition processes could be found in a previous study [22]. The micro-cantilevers were annealed at 310 °C during the fabrication process.

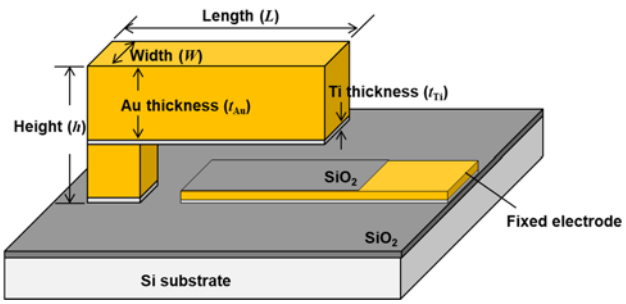


Fig. 5.2. Schematic view of the pure gold micro-cantilever evaluated in this study.

Micro-cantilevers with different dimensions were prepared, details are given in Table 5.1. The designed length (L) of the micro-cantilevers was varied from 200 to 1000 μm. The designed thickness of the Ti layer (t_{Ti}) was 0.1 μm. Two designed thicknesses of the gold layer (t_{Au}) were prepared, which were 10 and 12 μm. Four different designed widths (w_D) of the micro-cantilevers were prepared, and the exact width (W) was measured by a 3D optical microscope (OM) for the width dependency study.

Table 5.1. Dimensions of the pure gold micro-cantilevers.

L (μm)	w_D (μm)	t_{Au} (μm)	t_{Ti} (μm)
200 ~ 1000	10	10 & 12	0.1
	15		
	20		
	25		

An image of the micro-cantilevers observed by a scanning electron microscope (SEM) is shown in Fig. 5.3. The constraint condition at the fixed-end of a micro-cantilever is reported to have an influence on the deformation behavior when forces are applied on the micro-cantilever [5]. Therefore, as shown in Fig. 5.3, fixed ends of the micro-cantilevers evaluated in this study were constrained with layered structures to ensure the deformation mainly takes place over the cantilever body as the micro-cantilevers vibrate during the resonance frequency measurement.

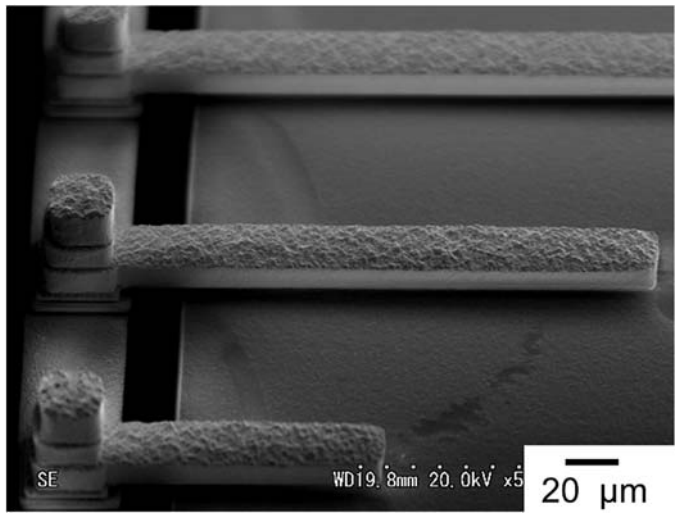


Fig. 5.3. An SEM image showing the micro-cantilevers having the width at 20.5 μm.

Fig. 5.4 illustrates the effective Young's modulus evaluation system by the resonance frequency method. Arrays of the micro-cantilevers were prepared on a silicon substrate, and the silicon substrate was mounted in a chip. After setting the into a custom-made holder and alignment of the laser spot light to tip of a micro-cantilever. The resonance frequencies were experimentally obtained as described in the following procedures. First, a voltage pulse (amplitude: 10~40 V, pulse width: 100 s) was applied between the cantilever and a fixed electrode to initiate free vibration mode. Next, a laser Doppler vibrometer was used to measure displacements of the cantilever tip. Finally, the resonance frequency was obtained from a fast Fourier transform (FFT) analyzer. An example of waveforms of the damped oscillation of the cantilever tip and the FFT analysis waveform is shown in Fig. 5.5. The first peak in the FFT wave form is the resonance frequency. The effective Young's modulus was calculated using Eq. (5.1). Thickness of the gold layer and density of gold (19.3×10^3 kg/m^3) were used in the calculation since thickness of the titanium layer is only 0.1 μm hence it was assumed to be insignificant in this analysis.

The resonance frequencies of the micro-cantilevers with the length varying from 200 to 1000 μm were plotted against $1/L^2$ as shown in Fig. 5.6. The effective Young's modulus was evaluated from the slopes of the linear asymptotes in Fig. 5.6 by Eq. (5.1). The results are summarized in Table 5.2. The effective Young's moduli of the 10 μm-thick

micro-cantilevers were ranged from 69.1 to 79.2 GPa as the exact width increased from 10.3 to 26.2 μm, and the effective Young's modulus increased from 57.2 to 65.9 GPa as the width increased from 8.9 to 25.2 μm for the 12 μm-thick micro-cantilevers. Generally, the width is suggested to have no influence on the effective Young's modulus [12-14, 17, 18], since the effective Young's modulus is calculated from the resonance frequency and the width information is not considered in Eq. (5.1). To the best of our knowledge, our group is the first report the width dependency of the effective Young's modulus.

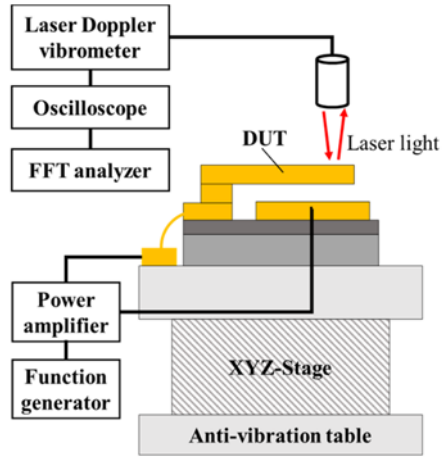


Fig. 5.4. Effective Young's modulus evaluation system by the resonant frequency method.

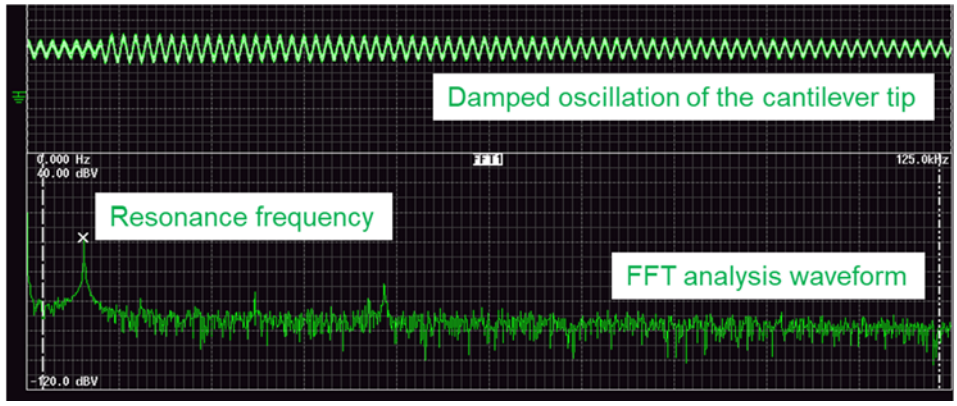
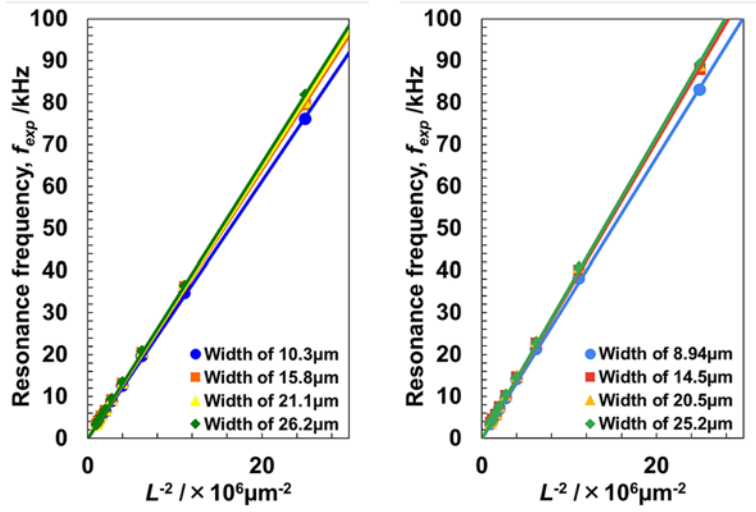


Fig. 5.5. The damped oscillation of the cantilever tip and the peak by FFT analysis waveform on the screen of the oscilloscope.

Causes of the width dependency observed in this study is still not fully understood yet. One possible explanation is the change in the surface-to-volume ratio, which an increase in the width leads to a decrease in the surface-to-volume ratio and results an increase in

the effective Young's modulus. This is in some degree similar to the sample size effect reported for the yield strength of small size metallic materials [8-10].



(a) (b)

Fig. 5.6. Experimental resonance frequency results of the micro-cantilever with the gold thickness of (a) 10 and (b) 12 µm.

Table 5.2. A Summary of experimental results of the effective Young's modulus of the pure gold micro-cantilevers.

	Designed gold thickness, t_{Au} (µm)							
	10				12			
Exact width, *W* (µm)	10.3	15.8	21.1	26.2	8.9	14.5	20.5	25.5
Effective Young's modulus, E_e (GPa)	69.1	75.4	76.9	79.2	57.2	64.1	65.8	65.9

On the other hand, effective Young's moduli obtained in this study were all smaller than the Young's modulus of bulk gold (79 GPa) [23, 24]. One explanation is the difference in specimen size, which specimens evaluated in this study had dimensions much smaller than bulk-size materials. Another explanation is the difference in the crystallinity [25]. Reduction in the Young's modulus or effective Young's modulus of gold materials is reported when the crystallinity is low, that is when the average grain size is small. Metals prepared by electrodeposition often have average grain size in nano-scale order [11, 26-28]. This could also contribute to the low effective Young's modulus.

5.3. FEM Simulations of the Pure Gold Micro-cantilever

FEM simulations were performed using a simulation software (COMSOL Multiphysics) to analyze the resonance frequency of pure gold micro-cantilevers having the same dimensions as those studied by the resonance frequency method. The equations of linear elastic material were selected in the category of solid mechanics. Constants of linear elastic materials such as Young's modulus, thermal expansion coefficient, Poisson's ratio and density were applied in the simulation. The constants were provided by the database embedded in COMSOL Multiphysics [23].

FEM simulations were used to compare with the width dependency result observed from the resonance frequency measurement. Fig. 5.7 shows an example of the micro-cantilever with the length of 300 µm, the width of 20 µm and the gold thickness of 12 µm generated by the simulation software. Results of the resonance frequency obtained from the FEM simulation are summarized in Table 5.3. The resonance frequency's was found to increase as the width increased. According to Eq. (5.1), the effective Young's modulus has a positive relationship with the resonance frequency, which is an increase in the resonance frequency leads to an increase in the effective Young's modulus. Hence, the increase in the resonance frequency observed from the FEM simulation confirmed the width dependency of the effective Young's modulus.

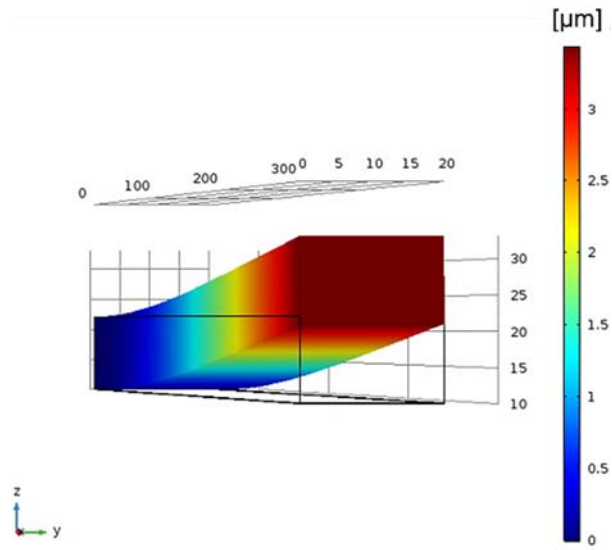


Fig. 5.7. 3D image of the micro-cantilever with the length of 300 µm, the width of 20 µm and the gold thickness of 12 µm used in FEM simulation.

The difference in the resonance frequency when the width changed from 8.9 to 25.2 was smaller when the length of the micro-cantilever increased. For instance, the resonance frequency increased by 0.70 % when the length was at 200 µm, and it was only 0.15 % when the length was 1000 µm. This finding indicates the width dependency is more significant when the specimen length is short.

Table 5.3. A Summary of the resonance frequencies, in kHz, from FEM simulations.

Width, W (μm) / Length, L (μm)	8.9	14.5	20.5	25.2
1000	3.995	3.997	3.989	4.001
900	4.933	4.935	4.938	4.941
800	6.244	6.245	6.251	6.256
700	8.157	8.162	8.168	8.174
600	11.10	11.11	11.12	11.13
500	16.00	16.01	16.03	16.04
400	24.94	25.03	25.06	25.09
300	44.46	44.53	44.59	44.69
200	100.1	100.3	100.5	100.8

5.4. Equation for Width Dependency of the Effective Young's Modulus

Equation (5.1) can be modified to include the width dependency into the resonance frequency as shown in the following:

$$f_{exp} = 0.162\frac{t_{Au}}{L^2}\sqrt{\frac{E_e(W)}{\rho}} = 0.162\frac{t_{Au}}{L^2}\sqrt{\frac{E\times[E_e(W)/E]}{\rho}} =$$

$$= 0.162\frac{t_{Au}}{L^2}\sqrt{\frac{E}{\rho}}\times\sqrt{E_e(W)/E} = f_c\times\sqrt{E_e(W)/E}, \quad (5.2)$$

where f_{exp} is the resonance frequency obtained from the resonance frequency measurement, $E_e(W)$ is the effective Young's modulus in a function of the width, L is the length of the micro-cantilever, t_{Au} is the gold layer thickness, and ρ is the density of gold. f_c is the resonance frequency calculated using constants from database and literature. E is the Young's modulus of bulk gold, which is 79 GPa. Eq. (5.2) can be simplified into the following equation:

$$\frac{f_{exp}}{f_c} = \sqrt{\frac{E_e(W)}{79}}, \quad (5.3)$$

Fig. 5.8 shows a plot of the f_{exp} against the f_c for the micro-cantilevers having the width at 8.9 μm. f_{exp} can be obtained from resonance frequency method, and f_c is a known value when all the constants are available. Along with Eq. (5.3), E_e can be readily calculated.

Fig. 5.9 shows a plot of the ratio between the effective Young's modulus and the Young's modulus of gold (E_e/E) against the width, and linear relationship between E_e/E and the width is observed. From this plot, the E_e/E in a function of the W can be obtained as shown in Eq. (5.4).

$$E_e/E = 0.0065W + 0.6883, \quad (5.4)$$

The finding of the width dependency of the effective Young's modulus is impactful for the design of MEMS components utilizing electrodeposited pure gold. Also, to the best of our knowledge, this is the first repot on the width dependency of the effective Young's modulus.

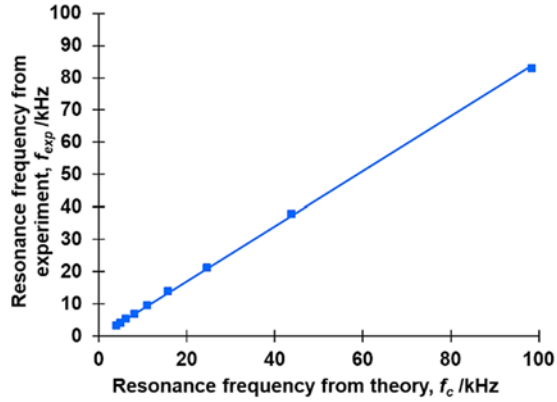


Fig. 5.8. A plot of the experimental resonance frequency against the resonance frequency calculated using constant values.

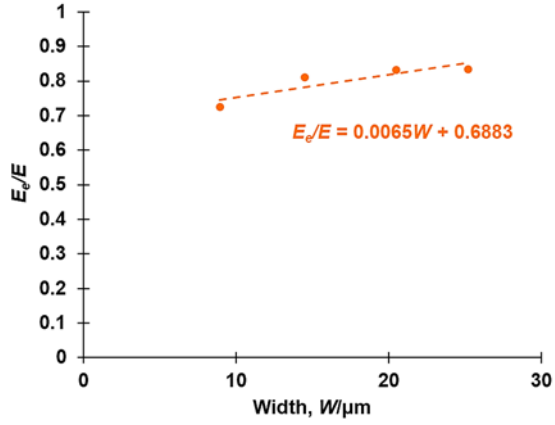


Fig. 5.9. A plot showing the relationship between the ratio of the effective Young's modulus and Young's modulus of gold and the width.

5.5. Conclusions

The effective Young's modulus of micro-cantilevers composed of electrodeposited pure gold was evaluate by a non-destructive resonance frequency method. The designed length of the micro-cantilever was ranged from 200 to 1000 μm, the designed thickness was 10 and 12 μm, and the designed width was varied from 10 to 25 μm. Exact widths of the

micro-cantilevers were measured to evaluate the width dependency. An increase in the effective Young's modulus was confirmed from the resonance frequency method. Similar tendency was observed from the FEM simulation, which the resonance frequency increased with an increased in the width. The increased resonance frequency implied an increased in the effective Young's modulus. Based on the experimental and FEM results, an equation showing the width dependency of the effective Young's modulus was developed. This equation could contribute to design of MEMS components development of next generation MEMS devices.

Acknowledgements

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Chapter 6

Sensor for Seamless Integrated Electrophotonics Circuits

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6.1. Introduction

Silicon photonics has been recently gaining momentum in the field of optical sensors for several applications, including chemical and biological. Its obtainment using low-priced planar silicon technology has been demonstrated, but several limitations exist when trying to achieve the low costs and high scalability of electronics. One main issue is the lack of a monolithically integrable silicon light source, as silicon is an indirect bandgap semiconductor and therefore a poor light emitter. The usual approach to overcome this is using external sources on top of the silicon chips [1, 2], which is complicated and expensive as compared to standard Complementary Metal Oxide Semiconductor (CMOS) electronics. Most frequently, the photonic integrated circuits (PICs) use silicon on insulator substrates, and combine different technologies usually non-compatible to standard MOS circuits [3].

However, in the past few years light sources based on silicon nanomaterials have been developed, such as those based in silicon rich oxide (SRO) [4] or silicon implanted oxide [5]. These light sources are fully compatible with silicon technology and can be integrated directly into the photonic chips, giving rise to a new area of research: seamless electrophotonics. The goal of electrophotonics is the integration of optical and electrical operations in a single silicon chip. This involves the simultaneous control and detection of electrons and photons in the same silicon substrate. An electrophotonic circuit is composed by at least three basic elements: an electronically driven light source, a waveguide that transmits light, and a photodetector. The fabrication methods must be

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seamless and compatible with complementary metal-oxide-semiconductor (CMOS) circuits technology [6-10].

Applications in chemical or biological sensors could take significant advantage of the development of fully integrated silicon electrophotonic chips. Nevertheless, it must be considered that the silicon compatible light sources developed so far present low light emission powers as compared to non-monolithically integrable ones, such as external or heterogeneous lasers [11]. Despite this, systems using light sources with relatively low luminous power have already been demonstrated to be viable [12-14]. To further improve the efficiency of the complete systems, we propose the use of light detectors with high sensitivities which take advantage of the direct coupling between the light source, the waveguide, and the detector, an exclusive feature of silicon electrophotonics. These include devices with MOS and bipolar technologies that integrate waveguides and detectors to form electrophotonic devices [15].

Then, we propose a light sensor to be used in seamless integration with an SRO-based light emitter and a silicon nitride waveguide for Si integrated electrophotonics circuits. The photodetector is called WAVESENSOR (WS) and it is a Metal-Insulator-Semiconductor (MIS) like structure which takes advantage of direct coupling to the waveguide. A unique feature of this photodetector is the close integration of the core waveguide, which is at the same time the insulator in the MIS architecture. The other end of the waveguide is seamlessly integrated with a SRO-based source that emits light with wavelengths λ from 450 nm to 850 nm [5]. The nitride core waveguide transmits the visible light directly to the depleted zone of the WS, which is enlarged by the biasing of the device to operate in a specific regime. The produced photocurrent can be then amplified by the same device to detect irradiance values in the wavelength range of the light source.

In this chapter, characteristics of the light emitter and the waveguide are presented, and the physics involved in the amplification of photocurrent by the proposed WS photodetector are explained. Computational simulations are used to validate our results. The simulation outcomes show that technological and design parameters, such as substrate dopant concentration and length between source and drain, can be adjusted to modify the electrical current gain.

6.2. Light Source

Si-based light sources for electrophotonics can be obtained with an emissive layer of SRO electrically stimulated in a capacitor-like structure. These sources are called Light Emitting Capacitors (LEC), and several configurations for the emissive layers with single or multiple SRO layers can be used. LECs have been extensively studied in the past, and for more details the reader can refer for example to [16]. They present broad emission spectra, with λ between 450 nm and 850. The usual structure of the LECs is shown in Fig. 6.1.

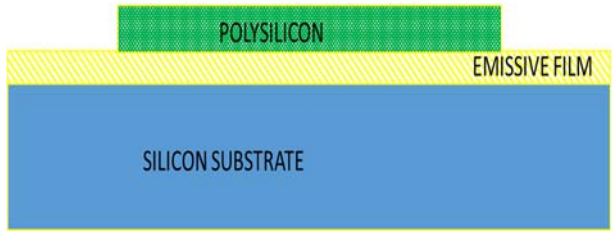

Fig. 6.1. Typical structure of LECs. The emissive film can be a monolayer of SRO, or an array alternating different nanometric films of SRO with different Ro.

The spectrum of a LEC is mainly controlled by the characteristics of the SRO in it. When obtained by Low Pressure Chemical Vapor Deposition (LPCVD), the parameter dominating the emission characteristics of SRO is Ro, which is defined as the partial pressures ratio of the reactive gases during the deposition. Typical gases are Nitrous oxide and silane, then:

$$Ro = \frac{P_{N_2O}}{P_{SiH_4}}, \tag{6.1}$$

where Ro determines the silicon excess in the SRO, Ro = 10 has around 12 % at., and Ro = 30 has around 4.5 % at. After annealing at around 1100 °C, light emission is promoted. The characteristic of Ro = 10 is high conduction and low intensity light emission, as compared to Ro = 30, which presents higher light emission and lower electrical conductivity [17]. It has been demonstrated that SRO can emit photoluminescence, electroluminescence, cathodoluminescence and thermoluminescence [17-20]. Fig. 6.2 shows electroluminescence spectra for LEC made of monolayers and multilayers.

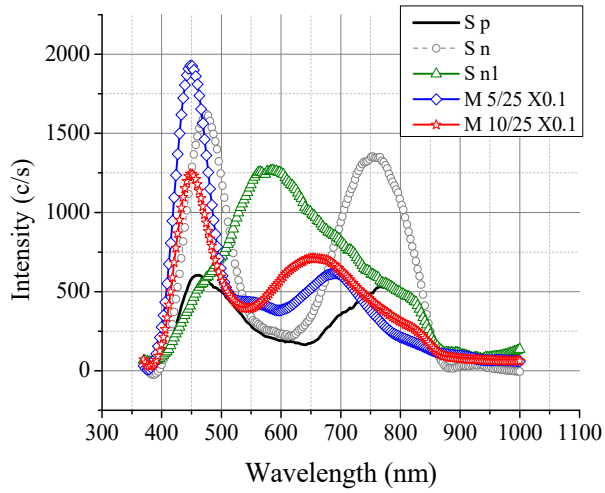

Fig. 6.2. Electroluminescence spectra of LECs with different emissive layers. S means single layer, M means multilayer, for more details see [20, 22].

The required thermal treatment for light emission in SRO can be considered a technological drawback. However, it has been demonstrated that it is not a problem to fabricate SRO structures with CMOS technology [21]. Perhaps the main drawback of LECs is the low electrical to optical conversion efficiency, in the order of 1×10^{-6}, [22]. However, LECs designed with multilayer arrays on textured silicon are under study to have more efficient structures [23].

6.3. Optical Waveguide

Silicon nitride (Si_3N_4) is compatible with Si technology, widely used in CMOS electronics, and has low optical absorption for λ from 400 nm to 800 nm [24, 25]. In addition, it is possible to couple films of this materials to the SRO LECs mentioned before, making the Si_3N_4 waveguides a natural selection.

The LPCVD technique is commonly used to fabricate silicon nitride because optical losses related to defects in films can be controlled by both high temperature during deposition and increasing Si content on the film, thus obtaining silicon rich nitride (SRN) [24-27].

Like with SRO, precursor gases ratio (RN) during SRN deposition characterizes the SRN films:

$$RN = \frac{P_{NH_3}}{P_{SiH_4}}, \tag{6.2}$$

where P_{NH3} and P_{SiH4} are the partial pressures of ammonia and silane, respectively. In [22] it was demonstrated that SRN deposited with RN from 100 to 120 produces films with high transmittance in the visible range, no photoluminescence response, low residual stress, and thermal stability.

A broad variety of waveguide geometries has been studied; however, the ones drawing more attention are those with simple fabrication process, such as planar and rib [27, 28]. Rib geometry represents a step forward to monolithically integration with Si light sources [12], [15]. This kind of geometry allows to confine the light below the rib, and is propagated either mono or multimode by modifying sizing properties: the rib width and height. Therefore, the field distribution is well known and the point with the highest electric field is easily located, both are important features during WS design.

In [27], computational simulations highlighted features of rib waveguides. The structure was comprised of silicon nitride as core material and SiO_2 as cladding. Fig. 6.3 shows the simulated waveguide. The main factor studied was the height, which was varied from 0.5 μm to 2 μm. The fractional height was set to r = 0.8. Simulation results demonstrated that waveguides propagate light of wavelengths from 480 nm to 750 nm with monomodal field distribution. However, the best results were obtained on waveguide sizing 0.5 μm height and 5 μm width, such that the losses of electric field were minimized.

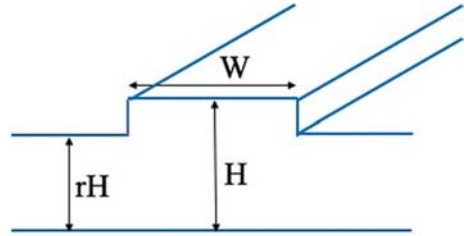

Fig. 6.3. Description of rib waveguides. H, r and W refers to height, fractional height and width, respectively.

Using the simulation results, rib waveguides were fabricated on Si substrates. A 2 μm-thick SiO_2 film was thermally grown as inferior cladding, to avoid losing electromagnetic energy by evanescent field going to silicon substrate [12, 22, 28]. Then, a SRN layer of 0.5 μm was deposited by LPCVD. RN of 100 and 120 were used as core material, and then a rib was etched by reactive ion etching (RIE). The rib width was defined by lithography. Fig. 6.4 presents surface topography of the waveguides obtained by profilometry, and Fig. 6.5 is the SEM image of the cross-section of a fabricated rib waveguide. Well defined boundaries for substrate, cladding and core materials are observed.

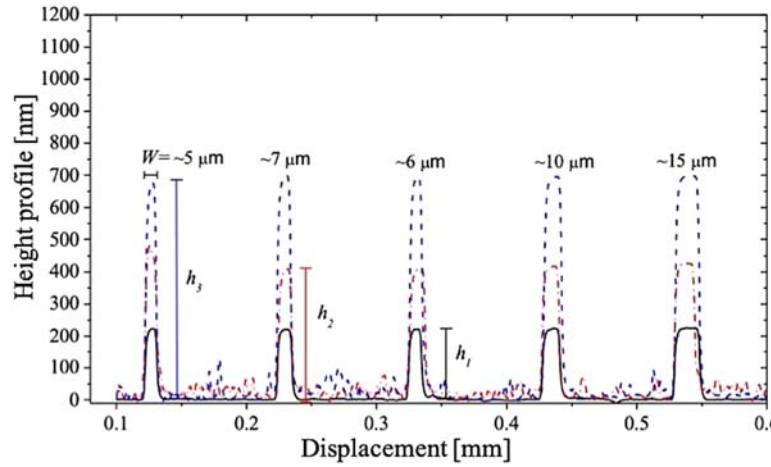

Fig. 6.4. Surface profile of rib waveguides using RN = 100 at different etching times. In the profile, outside height is defined as h = H-H*r, being h_1 the lowest and h_3 the highest etching times. Different rib widths were fabricated [22].

Electromagnetic field distribution propagating into optical waveguides was measured using a free space setup, as reported on [15]. Two light sources were used: A He-Ne JDS Uniphase laser model 1125 with optical power of 5 mW and λ = 633 nm (red), and an OEM diode laser model LSR473NL-80 with optical power of 70 mW and λ = 473 nm (blue). The waveguide output was measured by a CCD BC106-VIS Thorlabs beam analyzer with a detection range from 350 nm to 1100 nm.

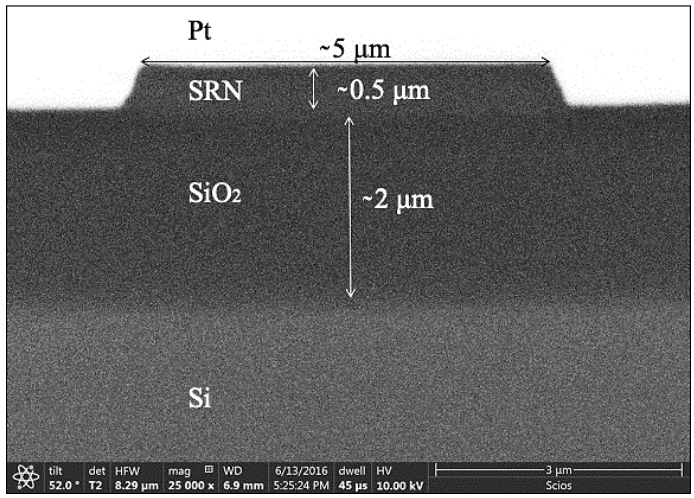

Fig. 6.5. Cross section view obtained by SEM. Three grey colors can be observed, attributed to substrate, cladding and core materials. From bottom to the top, these are silicon, SiO_2 and SRN [15].

Fig. 6.6 shows the energy distribution coming out of waveguides with RN = 100 and r = 0.5, and for both red and blue light sources. As observed, waveguide has a multimodal operation. Depending on coupling conditions, energy is distributed as TEM_{00} fundamental mode or superior modes. The performance of waveguides using RN = 100 or RN = 120 is similar [22]. In either case, maximum energy is located under the rib width.

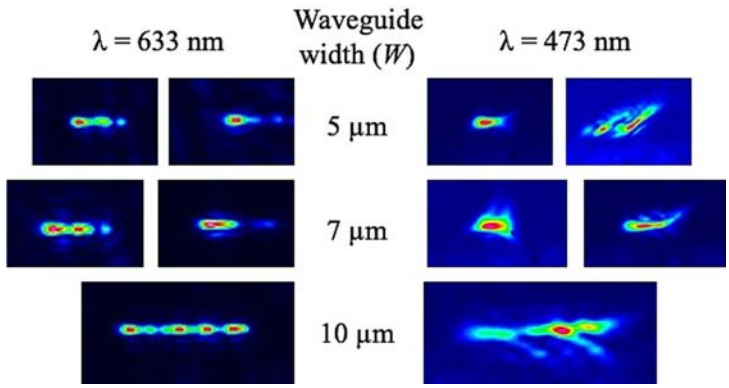

Fig. 6.6. Field distribution in the output port of the rib waveguide, showing multimodal field distribution for both red and blue light source. Fractional height was r = 0.5, height of 0.5 µm and length of 1 mm.

For an optical waveguide with fractional height of r = 0.5 and both RN the attenuation coefficient (α) was determined by edge light coupling. Table 6.1 presents α and waveguide size for the better case when using either RN = 100 or RN = 120. Despite both core materials exhibit similar properties and can confine and propagate light in the visible

range, there is a differentiated outcome when blue or red light is the main contribution of the light source.

Table 6.1. Attenuation coefficient as a function of Rib waveguide width and SRN core material [22].

SRN	Width, μm	α [dB/cm] λ = 473 nm	α [dB/cm] λ = 633 nm
RN = 100 (r = 0.5)	5	–	11.06
	7	–	13.26
RN = 120 (r = 0.56)	3	12.84	30.26
	9	23.44	16.54

Rib waveguides confine and guide visible light successfully. The losses are relatively small and adequate for the length required in silicon electrophotonic circuits. Then, light sources based on SRO emitting in the visible range, as those already analyzed, can be integrated and auto-coupled in a simple way.

Nowadays, in order to improve the performance and simplicity of the overall fabrication process, new integrated waveguide structures are under study. One of them is shown in Fig. 6.7. As can be seen, the cladding is made of air instead silicon dioxide.

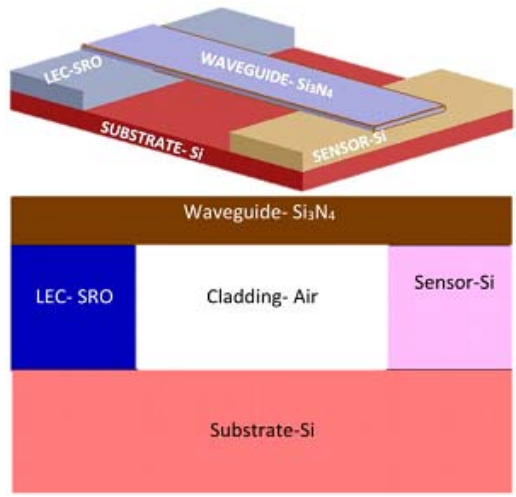

Fig. 6.7. Schematic of an integrated waveguide with the core of air instead oxide, the waveguide edges are on the LEC and the light sensor. The bottom schematic shows the profile of the electrophotonic circuit.

Fig. 6.8 shows a comparison of the modal losses between cladding of air and SiO_2. The modal loss was calculated numerically by the Finite Difference Eigenmode (FDE) solver of the software Lumerical [29, 30]. Where the calculation of modal losses is based on the imaginary part of its effective index and is computed with the well-known eq. (6.3):

$$Loss\left(\frac{dB}{m}\right)=\frac{10n_i 4\pi}{\lambda_0 \ln 10}, \tag{6.3}$$

where n_i is the imaginary part of the effective index and λ_0 is the transmitted wavelength.

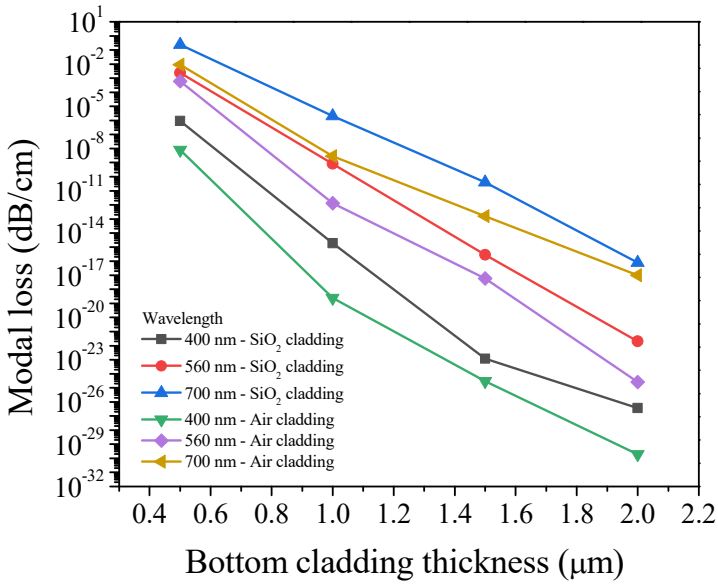

Fig. 6.8. Modal losses (dB/cm) of waveguides made either with cladding of air or silicon oxide at λ = 400 nm, λ = 560 nm, and λ = 700 nm.

As expected, the air cladding exhibits lower modal losses as compared to SiO_2 cladding (Fig. 6.8), allowing for a shallower bottom cavity. This is important because the main goal of such structures is to be used as electrophotonic chemical sensors, and the full cavity can be used as a reservoir for the potential analyte.

6.4. The Optical Sensor

As previously described, the light detecting device is formed by a MIS like structure in a Si wafer, with a Si_3N_4 film as insulator, which at the same time is the core of the waveguide transmitting the light from an integrated LEC. Fig. 6.9 shows a schematic of the system, with the integrated light emitter, the waveguide and the wavesensor.

The light sensor is also obtained using silicon CMOS standard processes. The waveguide section has a cladding formed by silicon dioxide. This can be made through thermal oxidation with Local oxidation steps LOCOS and etching techniques in order to obtain the buried cladding and good surface planarization. The core/insulator is deposited using LPCVD as explained in the previous section.

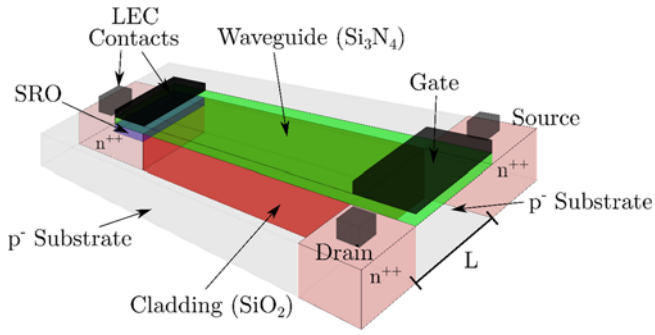

Fig. 6.9. Wavesensor: MIS like photodetector with the monolithically integrated waveguide and emitter.

The photocurrent from the absorption of the transmitted light is driven by the voltage bias between source and drain. The gate voltage should be kept in accumulation regime with the sole purpose of avoiding surface currents. The drain-source voltage is operated at Punch-Through in such a way that all the area under the gate is sensing light. The photocurrent is generated in this depleted zone.

Fig. 6.10 shows a transversal section of the sensor structure, which was simulated using the Athena – Silvaco TCAD platform [31-34]. The selected substrate was crystalline p-doped silicon with [100] orientation. The boron substrate doping concentration (N_A) was varied from 1×10^{12} cm^{-3} to 1×10^{15} cm^{-3}; however, for this analysis we use $N_A = 1\times10^{12}$ cm^{-3}. The separation between source and drain, L, and width, W, of the wavesensor were respectively 10 µm and 1 µm. Drain and source regions were obtained using phosphor ion implantation with high dose prior to a thermal annealing at 1100 °C for 180 min, which as mentioned, is required for the SRO-based light emitters. The waveguide/insulator silicon nitride film was obtained using chemical deposition with a thickness of 140 nm. The metal for the contacts is aluminum with a thickness of 1 µm. The substrate contact is achieved through the back of the substrate.

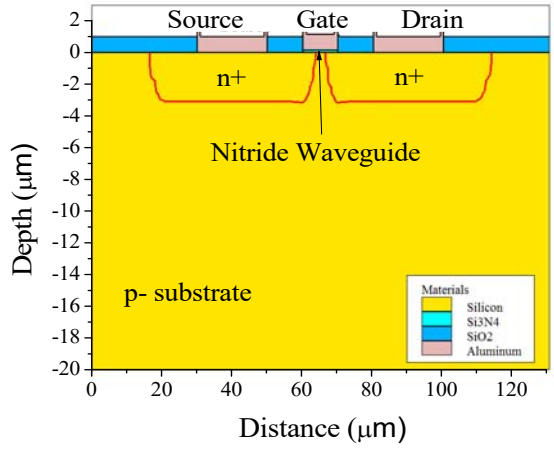

Fig. 6.10. Transversal section of the wavesensor obtained through computational simulation.

The light is produced by the LEC and directly injected into the waveguide, then transmitted through the silicon nitride/oxide core/cladding structure until it reaches the gate area [35]. On the surface of the WS, the waveguide core is in direct contact with the silicon, promoting the absorption of the guided light right below the gate. The photons transfer energy to the substrate to produce electron-hole pairs, which results in drain current variations.

6.4.1. Optical and Electrical Behavior

6.4.1.1. Electrical Behavior

The Fig. 6.11 shows the schematic of the transversal cut of the device with acceptors substrate concentration $N_A = 1\times10^{12}$ cm^{-3} and L = 20 µm. It is biased with $V_B = V_S = V_D = 0$ V; The gate is biased with V_{GS} = -5 V in order to obtain strong accumulation on the surface.

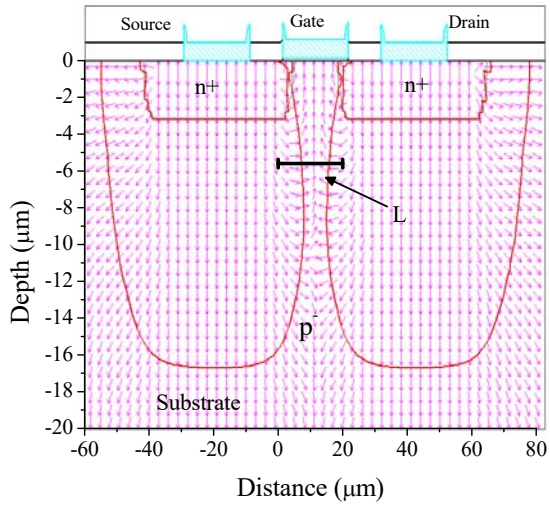

Fig. 6.11. Transversal section of the WS when $V_{DS} = 0$ V and V_{GS} = -5 V, obtained from the simulator. It is shows the depletion zone and the direction of the electric field.

Substrate-source and substrate-drain form pn junctions and their respective built-in voltage. A depletion zone is formed at source and drain. The depletion width can be computed using (6.4) [36].

$$W_{D0} = \sqrt{\frac{2\varepsilon_S V_{bi}}{qN_A}}, \tag{6.4}$$

where V_{bi} is the built-in potential, q, electron charge constant and ε_s, the silicon permittivity. Drain and source are highly doped contacts. For a substrate concentration of 1×10^{12} cm^{-3} the depletion width is approximately 17 µm. V_{bi} can be calculated using (6.5):

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}, \tag{6.5}$$

where k is the Boltzmann constant, T, the absolute temperature, N_D, the donor concentration and n_i, the intrinsic concentration. A wide depleted zone is observed.

Fig. 6.12 shows the depletion zone when the drain is biased with a drain voltage V_{DS} = 5 V and the V_{GS} = -5 V.

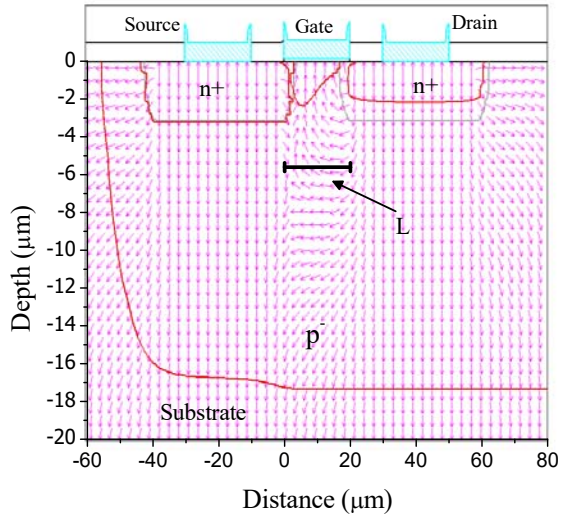

Fig. 6.12. Partial transversal section of WS with V_{DS} = 5 V, V_{SB} = 0 V and V_{GS} = -5 V. The drain depletion zone increases all the way through L and until merge with the source depleted zone. This condition is known as Punch-Through.

When the reverse voltage in the drain-substrate junction is increased, the drain depletion region widens (6.6):

$$W_D = \sqrt{\frac{2\varepsilon_S \left(V_{bi} + V_{DS}\right)}{qN_A}} \tag{6.6}$$

At Punch-Through voltage, the lateral depletion zone of the drain-substrate junction increases and reaches the source region, as shown in Fig. 6.12. This phenomenon produces an excess of leakage current when drain voltage is increased [37-40].

On the surface region, as the gate voltage moves towards a positive voltage the surface is also depleted and the whole volume under the gate is depleted. Fig. 6.13 shows this event.

The fully depleted region on the substrate between drain and source can be a current path if the drain voltage is increased, producing an excess of surface leakage drain current across this substrate region.

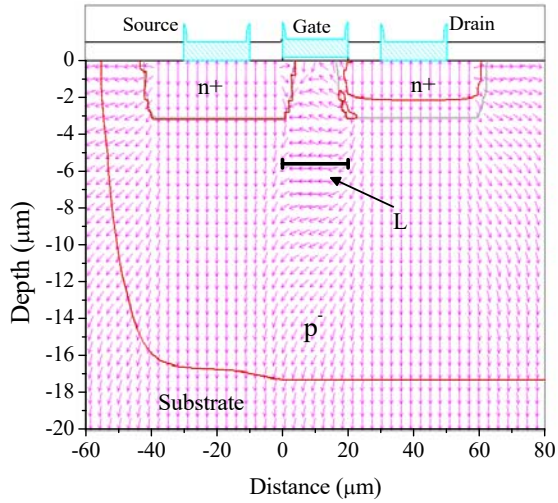

Fig. 6.13. Partial transversal section of WS biased with V_{DS} = 5 V and V_{GS} = 0 V, note that there is a wide and deep depleted zone.

Fig. 6.14 shows the electric current characteristic of the device. The drain current in dark condition increases as a function of V_{DS}.

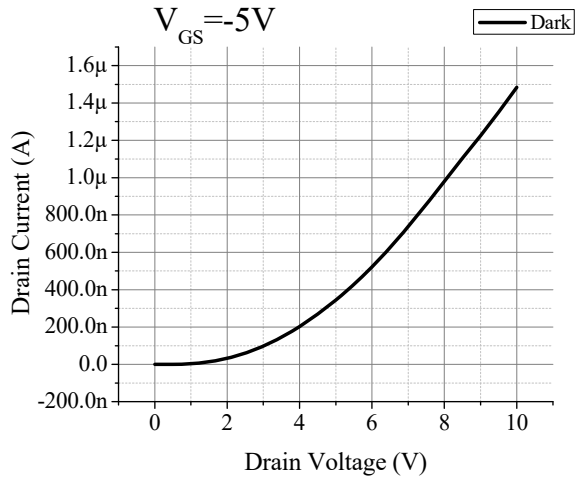

Fig. 6.14. WS Drain Current as a function of V_{DS} under dark current. The substrate concentration is $N_A = 1\times10^{12}$ cm^{-3} and L = 10 μm.

The current has a quadratic behavior for drain voltage above 1 V. In this bias condition, Punch-Through is reached and the current is increased. Under these conditions, the drain current is dominated by space charge current limited and can be modelled for the quadratic equation (6.7) [37, 41-43]:

$$I_D = I_{SCR} = \frac{9}{8}\frac{\varepsilon_s \mu_n A}{L^3}\left(V_{DS} - V_{PT}\right)^2, \tag{6.7}$$

μ_n is the electron mobility, A is the cross-sectional area and L the drain to source separation. V_{PT} is the Punch-Through voltage. V_{PT} can be computed using (6.8):

$$V_{PT} = \frac{qN_A L^2}{2\varepsilon_s} - V_{bi} \tag{6.8}$$

If light is guided to the surface of the gate region by a waveguide, it will be absorbed and produce an excess of drain current by effect of the optical power. The drain current under light stimulation is increased with the drain voltage increment.

6.4.1.2. Physics of the Light Detection

Fig. 6.15 shows the energy diagram for a WS on P substrate considering a substrate section on the WS detector between drain and source under thermal equilibrium, and at a depth relatively far from the surface to avoid its effects; the gate effects are also neglected.

Conduction band energy (E_C), valence band energy (E_V) and the Fermi level (E_F) along the length is shown. Under this initial condition, no drain current exists.

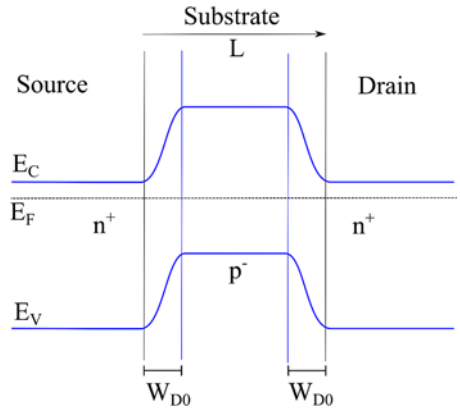

Fig. 6.15. Energy band diagrams on thermal equilibrium for a WS between drain and source on the substrate.

Fig. 6.16 depicted the band diagram out of equilibrium. A drain voltage has been applied ($V_{DS} > 0$ V).

When the device is biased with a $V_{DS} >> 0$ V, a pronounced band bending is produced. Fig. 6.17 shows the band bending at Punch-Through voltage, V_{PT}.

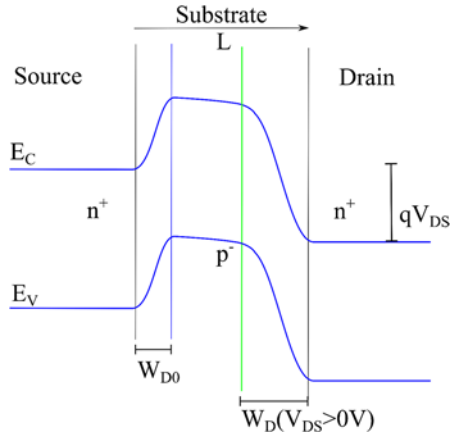

Fig. 6.16. Energy band diagrams for a WS between drain and source on the substrate when is biased with $V_{DS}>0$. Band bending is produced, and the depletion width is increased.

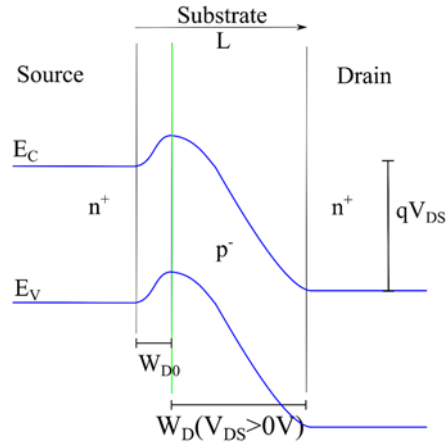

Fig. 6.17. Energy band diagrams of a WS at Punch-Through condition.

At V_{PT} the barrier height is decreased respect to the equilibrium, and the depleted volume is the whole detection zone. The drain voltage induces a barrier height reduction in the source-substrate junction allowing a flow of current.

Photons arriving the depleted zone will produce photogenerated electron-hole pairs, contributing to the current drain. Fig. 6.18 shows the band diagram under illumination.

The electron hole pairs are separated by the electric field and a photocurrent I_{opt} in the substrate is produced. If it is assumed that each photon generates an electron-hole pair (e-h), the ideal current of photons I_{ph} can be calculated with (6.9):

$$I_{ph} = q\frac{P_{in}\lambda}{hc}, \tag{6.9}$$

where P_{in} is the optical power, λ is the wavelength of the light, h, the Planck's constant and c, the speed of the light. This is the maximum current that can be generated in an ideal photodetector without current gain. However, light absorption in silicon presents different loss mechanisms [44]. Only a fraction of the electron-hole pairs photogenerated are converted on photocurrent, I_{opt}. I_{opt} can be expressed in the simple form (6.10) [36, 45]:

$$I_{opt} = \eta q \frac{P_{in}\lambda}{hc}, \tag{6.10}$$

where η is the que quantum efficiency and involves all losses of light, such as reflection, absorption, and recombination losses.

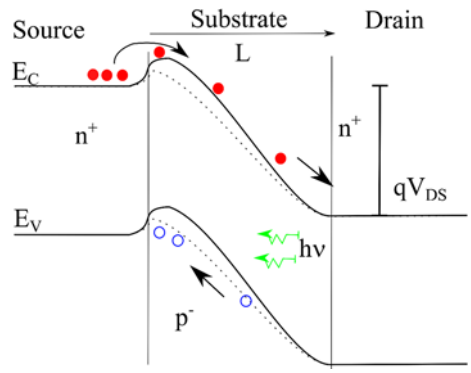

Fig. 6.18. Energy band diagrams of a WS on Punch-Through condition and illumination. The first barrier reduction is caused by the high voltage in the drain (solid lines), and the second barrier reduction is caused by the high density of e-h pairs generated by light (dotted line).

Minority carrier excess on the depletion zone produces a variation of the Fermi quasi level [44, 46-48]. This means that the potential barrier height is lowered, and more electrons are injected from the source to the drain, producing an additional optical current I_{Dopt}. Added to this reduction of the junction barrier, the excess of photogenerated e-h further increases the forward source voltage and reduces the height of the barrier, as shown in fig. 6.18. It can be said that an effective forward voltage V_{FS} is applied to the source junction, which is due to the drain voltage and the excess of the photogenerated electron hole pairs [40, 49].

The total current in the drain I_D is caused by electrons injected from the source I_{DS}, photogenerated electrons I_{opt}, and the dark electrons current.

$$I_D = I_{dark} + I_{DS} + I_{opt} = I_{dark} + I_{topt} \tag{6.11}$$

Then, a total electron drain due to generation is defined as (6.12):

$$I_{topt} = I_{DS} + I_{opt} \tag{6.12}$$

Because the magnitude of I_{topt} is higher than the current generated only by e-h, a current gain term β is proposed, and then:

$$I_D = I_{dark} + \beta I_{opt} \tag{6.13}$$

6.4.2. Electrical – Optical Simulation Results

Electrical and optical simulations were performed using SILVACO-Atlas [32, 34, 50]. Substrate and source contacts were biased to 0 V and the gate voltage was -5 V. The drain voltage was varied from 0 V to 10 V. The light source was modelled using a uniform beam with λ = 600 nm and light power Pin varied from 0 nW to 80 nW accordingly with reported SRO-based light sources [4, 5].

Fig. 6.19 shows the electric current as a function of the drain voltage and the light stimulation.

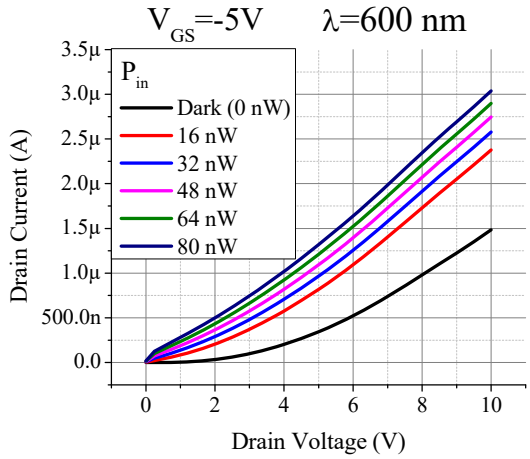

Fig. 6.19. Drain current as a function of drain voltage. Dark and under light stimulation curves are shown.

The 0 nW trace is for dark condition with only drain voltage modulation, a parabolic behavior is observed. This is consistent with the space charge current limited model exposed in previous section. Around 1 V, the drain current increases with drain voltage. An excess of drain current is observed for all the optical powers.

To obtain only the optical drain current component I_{topt}, the dark current I_{dark} (Drain current for 0 nW) is subtracted from the total drain current I_D. In order to quantify the amplification factor or gain, a ratio between I_{topt} and I_{opt} is obtained in the equation (6.14):

$$\beta = \frac{I_{topt}}{I_{opt}} = \frac{I_D - I_{dark}}{I_{opt}} \tag{6.14}$$

Fig. 6.20 shows the photocurrent ratio β as a function of the drain voltage for different optical powers, and a gain of current is observed. That is, the photocurrent ratio is greater than one, and it increases with the drain voltage. At V_{DS} = 10 V, the gain factor is above 110 for 16 nW and 40 for 80 nW.

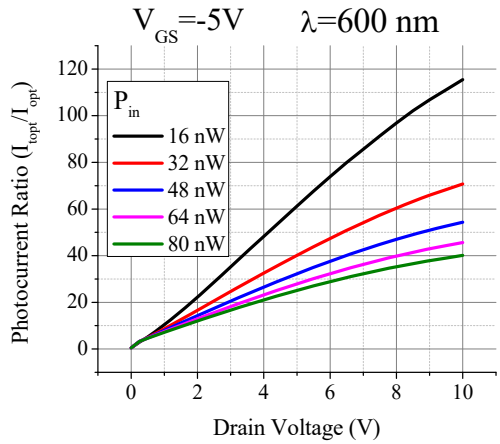

Fig. 6.20. Electro-optical gain for the WS for different optical powers as function of V_{DS}.

Gain varies with the optical power, and presents a non-linear behavior. As light power increases, more drain current is obtained, although the gain is reduced. This effect can be explained by the non-linear variation effect on the substrate potential for the excess of electron-hole pairs during the light stimulation. Fig. 6.21 shows the simulation of the potential variation in the WS under light stimulation.

The gain increases with the voltage; however, the dark current also increases. Then, the technological and design parameter must be carefully chosen.

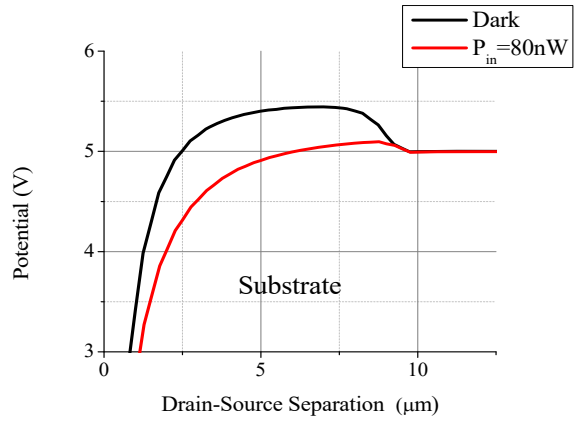

Fig. 6.21. Source junction barrier reduction due to illumination as a function of the separation length for VDS = 5 V, VGS = -5 V and VSB = 0 V, Pin = 80 nW.

6.5. Conclusions

A revision of light emitting capacitors (LECs) was done, and experimental emission curves were presented. LECs can be used as a light source in seamless electrophotonic circuits. LECs compatible waveguides were also reviewed. Experimental result showing that visible light can be transported by the waveguides were also presented. Then, LECs and waveguides can be used in a seamless electrophotonic circuits and they are auto-coupled. In addition, the waveguides can be auto-coupled to light silicon sensors. These structures provide the basic elements of seamless integrated electrophotonic silicon circuits. The elements mentioned are CMOS technology compatible, assuring a low-cost production technology.

A new detector named WAVESENSOR (WS) was also presented. The WS is a MIS like device, and the waveguide core is at the same time the dielectric of the gate allowing light transference straightforward from the waveguide to the sensor.

The analysis of the physics indicates that the WS is a bulk device and works under the Punch-Through regime. Due to the drain voltage and the photogeneration in the depleted zone, the drain-source potential barrier reduces, causing a photocurrent gain.

The simulation results corroborate that the drain current increases as the light intensity increases according to a quadratic behavior, and the drain current under dark condition shows the space charge limited conduction mechanism. Under illumination, a current gain factor up to 110 was obtained.

Acknowledgements

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Chapter 7

Fabrication of Aluminium Nanostructures for Microwave Detectors Based on Tunnel Junctions

A. A. Gunbina, M. A. Tarasov, M. Yu. Fominskii, A. M. Chekushkin, R. A. Yusupov and D. V. Nagirnaya

7.1. Introduction

The development of instruments for millimeter and submillimeter astronomy [1-3] is largely determined by the development of new methods for creating micro- and nanostructures used in the fabrication of receiving systems. The receiving systems on the modern observatories require the receiver comprising a large number of pixels with arrays of detecting elements with low level of intrinsic noise. The intrinsic Noise Equivalent Power (NEP) should be below 10^{-16} W/Hz$^{1/2}$ for ground-based observatories and three orders better for space observatories [3-4]. For reducing the intrinsic noise of the receiver it is essential to lower the operating temperature of the receiver below 1 Kelvin. That is why, in recent decades, most of the receiving systems are based on superconducting structures, which operate at ultra-low temperatures [5-7]. A separate class includes detectors based on tunnel junctions [8], which are also actively used for creating sub-Kelvin thermometers [9-11] and electron coolers [12-15]. A detailed overview of tunnel structures is presented in [16].

One of the important applications of NIS junctions is developing of receiving arrays of planar antennas with integrated SINIS (Superconductor – Insulator – Normal metal – Insulator – Superconductor) bolometers, which can be used as a sensitive element of the receivers for different tasks of radioastronomy [17-19]. For creation of a matrix receiver with a large array of tunnel junctions (> 1000), reliable technology for their fabrication and the possibility of varying the area of junctions in the wide range are required. For calibration of received signal the essential element is independent thermometer based on series array of NIS junctions which can be made on-chip with receiving array [20]. Normal

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metal – Insulator – Normal metal – Insulator (NININ) tunnel structures can also be used as a microwave and IR detectors [21-22].

Another promising direction for increasing of the sensitivity of the receiving system is the creation of a readout system based on Superconducting Quantum Interference Devices (SQUIDs) [23]. The theoretical and practical implementation of traveling wave parametric amplifier based on SQUID for readout system of signal from receiving arrays, which has a number of advantages compared to JFET readout, are presented in [24-25]. Of course, the development of new methods for SQUIDs fabrication is interesting for the researching of superconducting elements of nanoelectronic not related with astrophysics [26-28]. The bridge-free technology allows to make SQUIDs with the possibility of varying the diameter of the loop and the area of the Josephson junctions in a wide range from 0.01 μm^2 to few μm^2.

It should be noted that one of the the main engine for the development of nanotechnologies of microwave detectors is already becoming, and in the coming decade will be dominated by the telecommunications both satellite and mobile of the seventh generation (7G) [29-31].

The methods described in this article for creating tunnel structures are universal, and can be used in the development of microwave elements of the terahertz range.

7.2. Investigation of Propertis of Thin Aluminum Films and Multylayer Structures Based on Them

Aluminum is one of the most common materials for fabrication of various superconducting nanostructures: from detectors, thermometers and electron coolers to measuring systems and amplifiers based on SQUIDs. On its basis, it is convenient to create both tunnel barrier, by oxidation, and films of normal metal (which is technologically advanced for some fabrication techniques) by deposition of a sublayer of different materials. A detailed study of various thin-film structures based on aluminum (pure films that are oxidized under different regimes and multilayer hybrid structures with silicon and chromium) is given in [32]. The main results of the work [32] will be given in the subsections below.

7.2.1. Granularity of Aluminum Film and Tunneling Junctions on Their Basis

Studies with an atomicforce microscope were per formed to obtain the dependences of the characteristics of films on the properties of their surfaces. The surface images of thin aluminum films substantially differ from the surfaces of thicker films (Fig. 7.1). Forfilms with thicknesses of ≥20 nm, rather large round grains with diameters of up to 50 nm are observed, whereas films with oxygen are characterized by dips and flaws surrounded by aluminum crests. Typical images of the surfaces of aluminum films 20 and 6 nm thick are shown in Fig. 7.1a and Fig. 7.1b, respectively. The dimensions of large grains in the first and second figures are ~50 and ~15 nm, respectively. The cross sections of films 20 and

3 nm thick are shown in Fig. 7.1c and Fig. 7.1d, respectively. The values of the surface roughness averaged over the area and along a line are presented in Table 7.1. At the last stage of this study, we manufactured superconductor-insulator-normal metal-insulator-superconductor (SINIS) tunneling structures with dimensions of tunneling junctions of 0.3×1.0 μm. As the normal metal absorber, aluminum films 5 nm thick with a chromium sublayer 0.5 nm thick were deposited. Then the system was oxidized in oxygen at a pressure of 5×10^{-2} mbar for 5 min. For all manufactured samples, we obtained a quality parameter (the ratio of the resistance at a zero bias to the nor mal resistance) $R(0)/R(1\ mV) \geq 1000$ at $T \leq 280$ mK. The structures manufactured earlier (Fig. 7.1a) had an appreciably lower yield of samples with the required quality parameter even for junctions of smaller dimensions, 0.2×0.1 μm. As a rule, the quality parameter for such structures was at most 300.

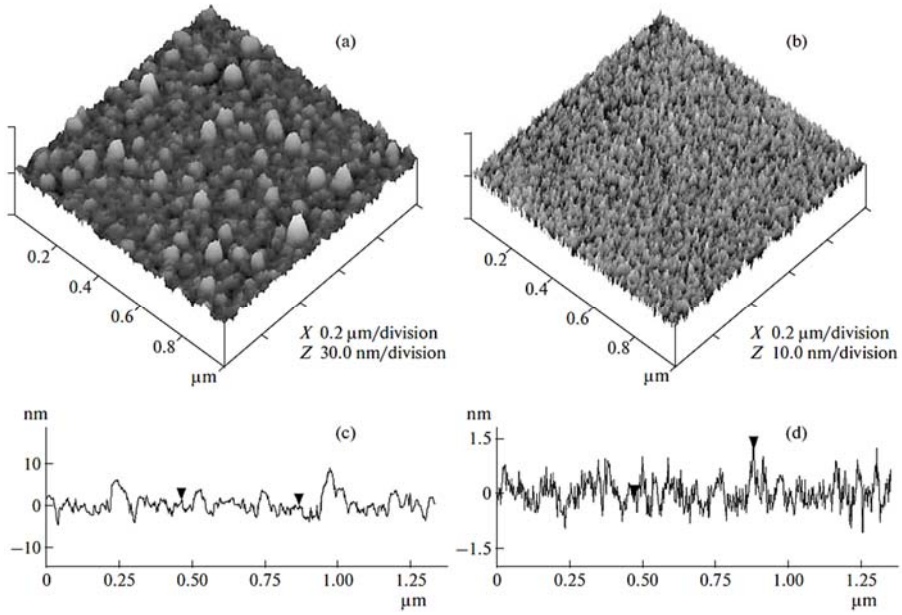


Fig. 7.1. Images [32] of the surfaces of aluminium films (a) 20 and (b) 6 nm thick obtained with an atomic force microscope; cross sections of the surfaces of aluminium films (c) 20 and (d) 3 nm thick.

Table 7.1. Results of average roughness measurements [32].

Thickness, nm	Area averaged deviation from the mean, nm; maximum deviation, nm	Deviation from the mean averaged along a line, nm; maximum deviation, nm
20	2.28; 23.3	1.2; 6.7
6	0.73; 6.1	0.57; 3.4
3	0.43; 9.2	0.29; 1.87

7.2.2. Superconductivity in Thin Aluminium Films and Multilayer Structures

To study the possibility of controlling the critical temperature of aluminium based film structures, such structures with different combinations of aluminium with silicon, chromium, and oxygen were manufactured. The total thickness of the multilayer structures was usually at a level of 20 nm. All films were deposited via thermal evaporation in a Balzers high vacuum evaporation facility. The results of measuring Al-Si multilayer structures are presented in Table 7.2. The main tendency for these films involves an increase in critical temperature Tc of the superconducting transition, at which a zero resistance is observed, from 1.50 to 2.43 K, when the aluminium film thickness decreases from 18 to 3 nm. In this case, the film resistance per square at T = 2.7 K increases from 1.6 to 20 Ω. Presumably, the resistance of the structure is determined by the conductivity of the upper aluminium layer, and the underlying layers in the absence of flaws in the insulating silicon layer have virtually no effect on the resistance. Hereinafter, all resistances and critical currents are presented for a sample with dimensions of 7×7 mm; i.e., the resistances are indicated for a film square. The results of measuring 20 nm thick aluminium films deposited on oxidized silicon substrates in the presence of oxygen are presented in Table 7.3. As the oxygen pressure increases in the process of evaporation of an aluminium film, an increase in the film resistance is observed, accompanied by a simultaneous increase in the critical temperature to 2.4 K. A further increase in the oxygen concentration leads to a transition of films to the insulator state. The results for films with oxygen are not quite reproduced stably, but the main trends are observed quite definitely. Note that there is a correlation between the data of both tables: the highest critical temperature near 2.4 K is observed for samples with higher resistances of 25 Ω at room temperature for a 3 nm thick film of pure aluminium and 56 Ω for a film deposited in the presence of oxygen.

Table 7.2. Results of measuring R and Tc of Al–Si multilayer structures [32].

№	Thickness of Al-Si layers, nm	Tc, K	R, Ω/□	
			T = 300 K	T = 2,7 K
1.	18	1.5	2.44	1.6
2.	9 – 0.5 – 9	1.8	2.66	2.0
3.	9 – 1 – 9	2.0	2.93	2.66
4.	9 – 1.5 – 9	1.88	3.22	2.28
5.	9 – 2 – 9	2.0	3.3	3.0
6.	9 – 2.7 – 9	1.86	2.2	1.6
7.	6 – 1 – 6 – 1 – 6	2.3	8.16	7.69
8.	6 – 2 – 6 – 2 – 6	2.1	3.33	3.07
9.	6 – 1	1.97	10	8
10.	4.5 – 1 – 4.5 – 1 – 4.5 – 1 – 4.5	2.4	13.5	13
11.	4.5 – 2 – 4.5 – 2 – 4.5 – 2 – 4.5	2.3	12	11.3
12.	3 – 3 – 3 – 3 – 3 – 3 – 3	2.43	25.4	20

Table 7.3. Results of measuring resistance R and critical temperature Tc of films deposited on oxidized silicon substrates in the presence of oxygen [32].

№	O2 pressure, 10–5 mbar	R, Ω/□ (T = 300 K)	Tc, K
1.	2.5	∞	-
2.	2	∞	-
3.	1	150000	0
4.	1.5	5.1	1.7
5.	0.5	20	1.9
6.	0.3	56	2.4

The last group of aluminium film structures was deposited on a thin chromium sublayer that had been evaporated from a tungsten boat with a chromium powder, which was placed in a ceramic tube with a 2 mm diameter hole both in the presence of oxygen and in its absence. The results are presented in Table 7.4. The results of measuring the critical temperature were found to be highly dependent on the sublayer deposition conditions, the presputtering time, the presence of oxygen, and the temperature of a chromium containing rod or a refractory crucible with a chromium powder. For some samples (№. 2, 4, and 5), superconductivity did not arise until 50 mK, and others (№ 1, 3, and 6) were superconducting. When the hole in the ceramic tube increased to 5 mm and the presputtering time decreased, the thickness of the chromium layer being 0.3-0.5 nm, only nonsuper conducting Cr/Al films were produced. Such a great spread in suppressing superconductivity of aluminium by a chromium sublayer may be due to different fractions of chromium oxides. Chromium dioxide being a semi metallic ferromagnet seems to be the most efficient impurity for suppressing superconductivity. Note that the melting temperature of CrO_2 is only 400 °C. There are other chromium oxides – CrO_3, Cr_2O_3, Cr_3O_4 – that are nonmagnetic dielectrics at low temperatures. Oxide Cr_2O_3 (chromia, chrome green) is an antiferromagnetic dielectric with a corundum structure and a melting temperature of 2435 °C. Chromium itself melts at 1880 °C and becomes antiferromagnetic at T < 312 K. During evaporation, as the temperature increases, first, at 400 °C, the CrO_2 ferromagnetic oxide evaporates; then, a proper Cr film is deposited by evaporation at 1880 °C, and by this moment, CrO_2 3 has already entirely evaporated or been decomposed. If the shutter is opened at the beginning of heating, a part of CrO_2 is deposited on a substrate. Under certain conditions, during deposition of chromium in the presence of oxygen, a certain amount of CrO_2 can also be formed and may be sufficient for suppressing superconductivity in the Al film.

If chromium was evaporated from a tungsten boat placed inside a ceramic tube with a hole and with preliminary evaporation with the closed shutter, CrO_2 was removed during preevaporation and, as a result, a metal chromium film was predominantly deposited. In an aluminium/chromium two layer structure, a proximity effect arose and superconductivity was slightly suppressed when a decreased critical current was observed (Table 7.4, rows 1, 3, 6).

In conclusion of this paragraph: the results show that, as the thickness of an aluminium film increases, its resistance per square decreases simultaneously with a decrease in the

temperature of the superconducting transition, accompanied by an increase in the film granularity. When films are deposited in an oxygen atmosphere or when their thickness decreases, their properties are in the transition region where the surface resistance increases very rapidly upon small changes in the film thickness or the oxygen pressure. The critical temperature first increases and then abruptly falls, and superconductivity vanishes. The deposition of a thin chromium sublayer under certain conditions completely suppresses superconductivity; this effect is evidently associated with the presence of a CrO_2 ferromagnetic oxide. A decrease in the film thickness leads to a smaller size of grains and a higher quality of the tunnelling junctions based on them.

Table 7.4. Results of measuring resistance R and critical current Ic of aluminium films deposited on a thin chromium layer [32].

№	Thickness of Cr layer, nm	O2 pressure, mbar	R, Ω/□			Ic, μA (T = 50 mK)
			T = 3 K	T = 280 мК	T = 50 мК	
1.	2	0	1.66	0.95	3	120
2.	4	0	1.87	1.82	3.24	0
3.	2	1×10^{-5}	1.72	1.6	3	600
4.	2	2×10^{-5}	2.17	2.05	3.78	0
5.	1	0	-	-	3.86	0
6.	1	2×10^{-5}	1.86	0	0	>1000

7.3. The Direct-write Technology

7.3.1. Simplest Technology

The simplest technology for fabrication of tunnel structures is direct lithography and lift-off process [33]. This technology with different modifications has long been used for the fabrication of tunnel structures, for example [34]. In our case, the first layer consists of the contact pads and wiring from a three-layer Ti/Au/Pd film (Fig. 7.2a). A resistive mask is formed by a two-layer resist: a lift-off resist (LOR) to obtain a "negative" profile and a photoresist, for example, the AZ or S18xx series. The thickness of the lift-off resist (h_{LOR}) is selected thus the ratio $h_{LOR} = 1.3*h$ is fulfilled, where h is the thickness of the deposited film. Each followed deposited film should be thicker than the previous one. The NIS-junctions are made in the second layer from Al/AlOx/Cu film (Fig. 7.2b). The last stage is the deposition of the normal metal absorber (for example, Cr/Cu/Cr) – Fig. 7.2c. SEM image of the fabricated SINIS structure by lithography technique is presented in Fig. 7.3a.

The main advantage of such technology is the possibility to make junctions of different areas and it does not require specialized evaporation setup with a tilt and turn of the substrate. It is also possible to use different types of lithography: photolithography, laser lithography or e-beam lithography, it's depending on the size of the structure.

The disadvantage of this technology is that the structure is deposited with a vacuum break, which reduces its quality (Fig. 7.3b).The quality of junctions can be improved by some modifications of this technology that are presented in [35-37].

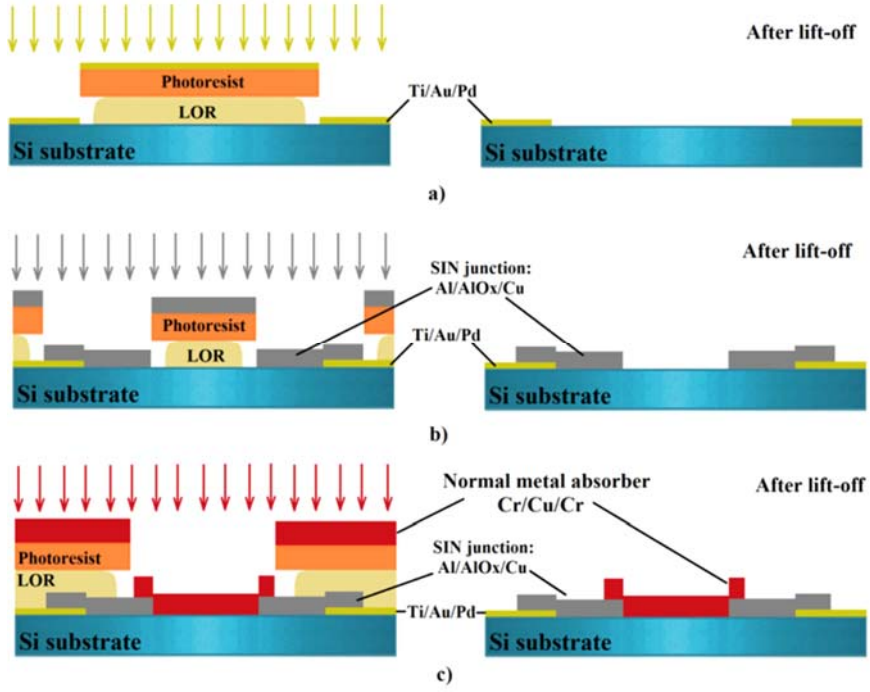


Fig. 7.2. The schematic image of direct lithography technique for fabricating NIS structures: a) – The first layer: contact pads and wiring; b – Formation of NIS junctions; c) – Deposition of the normal metal absorber.

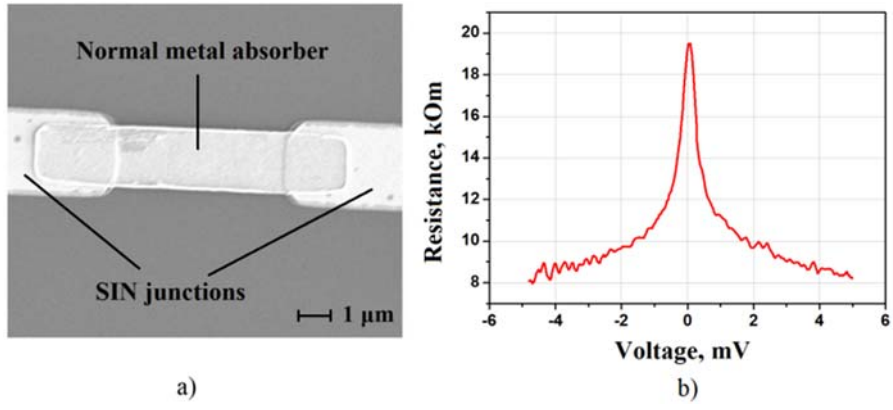


Fig. 7.3. SINIS structure made by direct lithography technique: a) SEM image of the structure; b) Measured dynamic resistance.

7.3.2. Direct-write Trilayer Technology

A brief description of the process of fabrication a NIS tunnel junction from [36], is following: both the trilayer structure and the normal metal absorber were patterned by lithography followed by deposition and lift-off. As a final step, parts of the gold and normal metal covering the trilayer structure were removed by ion-beam etching. For patterning the superconductive electrode, a lift-off resist and e-beam resist were spun over the wafer (Fig. 7.4 a), exposed in the e-beam lithography system, and developed (Fig. 7.4 b). Then an Al layer was deposited at a pressure of 4×10^{-7} mbar and oxidized for 2 min in oxygen ambient at 5×10^{-2} mbar to create the tunnel junction. Then Cu was evaporated as a normal metal electrode of a tunnel junction and covered by Au for passivation (Fig. 7.4 c). Next, the normal metal Cu absorber was patterned by ebeam lithography and thermal evaporation (Fig. 7.4 d and Fig. 7.4 e). Finally, argon ion-beam etching was used to remove Cu and Au from the top of the trilayer structure; see Fig. 7.4f and Fig. 7.4 g. The optical image and result of measurements of 30 SIN tunnel junctions are shown in Fig. 7.4 h-i.

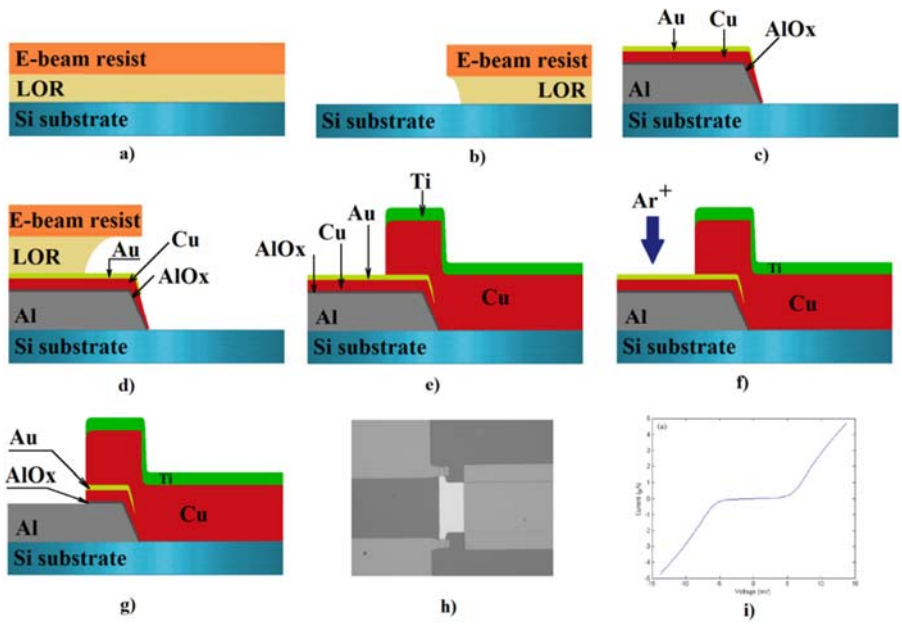
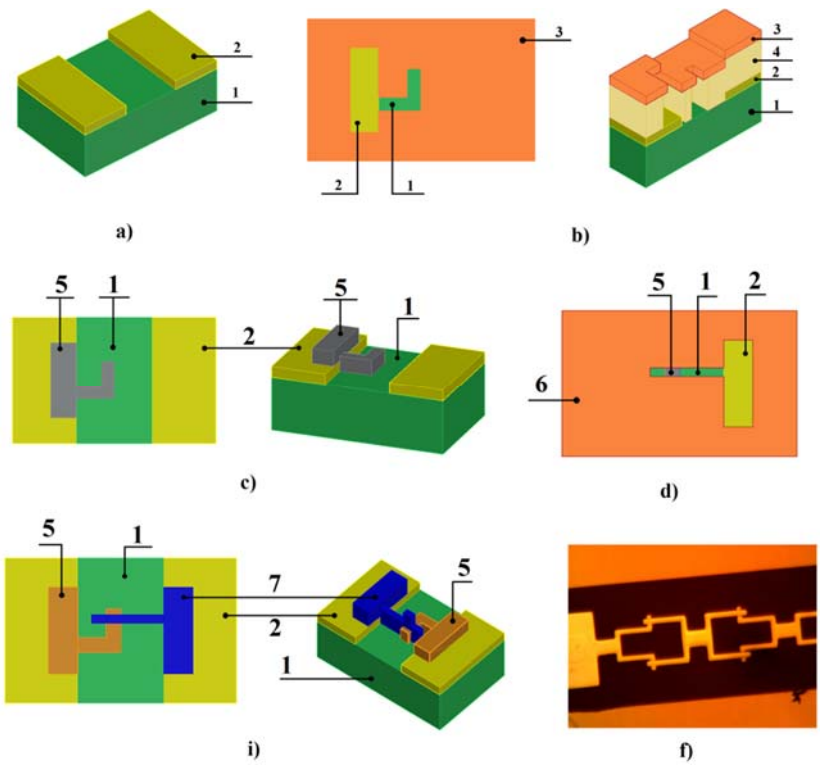


Fig. 7.4. Fabrication process of SIN tunnel junction with Ar etching [36]: a) Two layer resist; b) Resist after developing; c) Evaporation of NIS junction; d)-e) Formation of Cu absorber; f)-g) Argon ion-beam etching; h) Fabricated structure; i) Results of measuring.

7.3.3. Sputtering with Separate Direct E-beam Lithography

Such technology [38] includes two technological cycles for the fabrication of a tunnel junction. First, two-layer resist (Fig. 7.5b) for lift-off lithography was coated on the silicon substrate with conducting electrodes (Fig. 7.5a), exposed and developed. The firs layer (superconducting aluminium for SIS and SIN junction or any normal metal for NIS and

NIN junction) was sputtered Fig. 7.5c. Second, the same two-layer resist was coated, exposed and developed (Fig. 7.5d). The main step of this technology is ion milling of the first deposited layer. This process is used to remove the oxide on the first deposited film surface formed due to the break of vacuum. Next, the tunnel barrier can be formed by oxidation of aluminium into vacuum chamber. For SIS and SIN junctions the first deposited film is oxide after ion millin. For NIN and NIS junction the thin aluminium film (few nanometers) is sputtered before oxidation. After that, the second film can be sputtered (aluminium for SIS and NIS junction and any normal metal for NIN and SIN junctions). It should be noted that for NIN and SIN junctions, a buffer layer of palladium must be sputtered before normal metal. Optical image of fabricated sample (SQUID loops with two SIS junctions) is shown in Fig. 7.5f. The result of measurements (IV curves) of single SQUID loop and chains of 10, 20 and 100 SQUID loops are presented in Fig. 7.6.

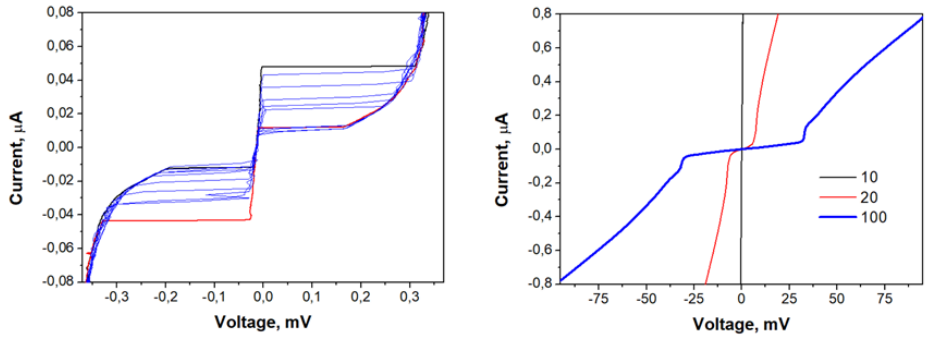


1 – Silicon substrate; 2 – Conducting electrodes; 3 – First resist mask for the first layer; 4 – First resist layer creation of counter slope; 5 – First deposited layer; 6 – Second resist mask for the second layer; 7 – Second deposited layer.

Fig. 7.1. Schematic image of separate lithography technique [38]: a) 3D view of silicon substrate with conducting electrodes; b) Top view and 3D view of resist mask for the first superconducting layer of aluminium; c) Top view and 3D view of the first deposited layer; d) Top view of resist mask for the second superconducting layer; i) Top view and 3D view of deposited SIS structure; f) Optical image of fabricated structure.

The main advantages of this technology are:

- High quality of tunnel junction (SIS, NIS, SIN or NIN);
- Any shape and area of tunnel junction;
- The complex equipment for deposition with tilting and rotating of substrate is not required.



a) b)

Fig. 7.2. Measured IV curves: a) Single SQUID; b) Chains of 10, 20 and 100 SQUIDs.

7.4. The Dolan's Bridges

The Dolan's deposition technique [39] is a shadow evaporation (evaporation at an angle) of the films through a suspended resist bridge. This technology has been widely used for fabrication of the structures with tunnel barriers and has been used for a long time for fabrication of SINIS bolometers developed by our team [17]. In comparison with the direct lithography technique, this technology made it possible to form submicrometer normal metal absorbers metal and NIS junctions without breaking the vacuum. Schematically, the formation of a SINIS bolometer through suspended resist bridges is shown in Fig. 7.7. The typical dimensions of such structure are: absorbers 0.1×1 μm, NIS-junctions – 0.5×2 μm (design with explanations – Fig. 7.7a). The first step is to coat a two-layer Copolimer MMA/PMMA resist to the cleaned substrate (ZEP or a cheaper analog – ARP, can be used instead of a PMMA resist. Using these resists instead of PMMA makes it possible to do selective developing of each layer). After developing and cleaning in the oxygen plasma, the substrate with the resistive mask is loaded into the deposition chamber and additionally cleaned in argon plasma. The first layer is the normal metal by layer absorber (in our case it is aluminum with a sublayer of iron 1.2 nm Fe/ 14 nm Al, which supress the superconductivity of aluminum, Fig. 7.7b) that deposite at the normal angle. For making the insulator layer, the oxygen is entered into the chamber and the aluminum is oxidized. Next, the superconducting aluminum electrodes (70 nm and 80 nm) are evaporated at the angles of ±45° – Fig. 7.7c. The schematic image of the SINIS structure after lift-off is presented in Fig. 7.7d. The images of various designs of SINIS bolometers made by Dolan's technology are shown in Fig. 7.8. The results of

measurements of the single SINIS structure and array of series-connected ring antennas with integrated detectors are presented in Fig. 7.9. For NININ detector deposition [22]. of superconducting aluminum is substituted by normal metal – Fig. 7.10. In the case of SIS junction fabrication (Fig. 7.11) by this technology, the first layer is superconductor (for example, aluminum without a sublayer of iron) that deposited at the normal angle.

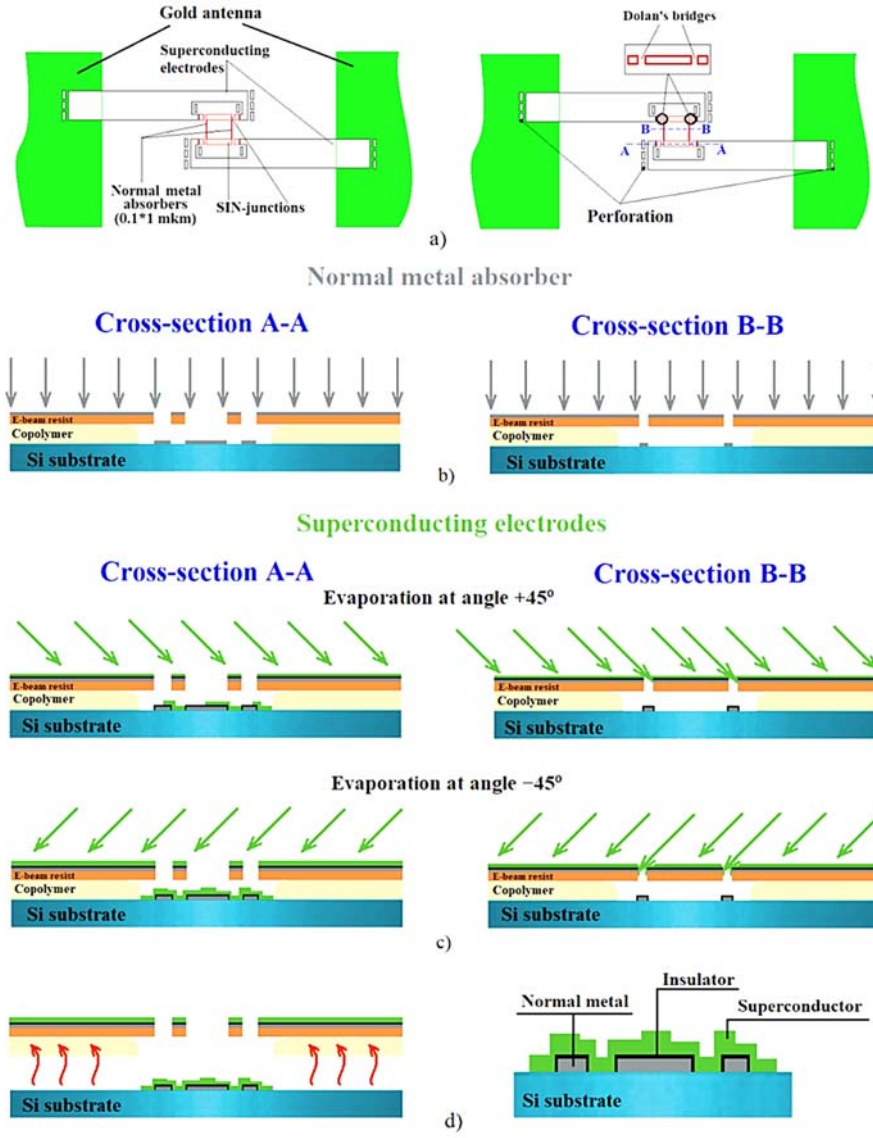


Fig. 7.3. The schematic image of the SINIS bolometer fabrication by the Dolan's technique: a) Typical design of the SINIS bolometer; b) Deposition of the first layer (normal metal 14 nm Al/1.2 nm Fe) at the right angle; c) Deposition of the superconducting electrodes at angles of ±45 after oxidation; d) Removing of the resist mask (left) and enlarged schematic image of deposited NIS junction (right).

Limitations of the technology:

1. Possibility of slacking or breaking off of the resistive bridge;

2. If the copolymer layer is not sufficiently developed, the resistive wall is deposited by a material, which in the process of lift-off can break off together with the deposited structure or remain as a wall (Fig. 7.12a);

3. If the copolymer layer is overdeveloped and there is a possibility of bending of the upper resist (Fig. 7.12b), which also negatively affects the quality of the fabricated structure;

4. There is difficult to create junctions with submicron size;

5. A narrow range of doses for exposure (deviation not more than 10 %).

Recommendations to the technology:

1. The substrate cleaning in the oxygen plasma and immediately before deposition with argon should take place in a "soft" regime so as not to damage the suspended resistive bridges.

2. If possible, to avoid the slant lines in the design (Fig. 7.8b). In such designs, it is likely that the material will be deposited on the resist wall with subsequent problems during the lift-off process. The using of the straight lines in the design significantly improves the quality of fabricated structures (for example, on Fig. 7.8a).

3. To avoid deposition of the material to the resist walls, it is necessary to add perforation on the problem areas of the structure (Fig. 7.13) that make the necessary undercut of the lower copolymer. During developing, the lower layer (copolymer) is removed, but in the evaporation process the material does not deposit into this narrow window in the resist (0.2-0.3 μm). When a window in resist is longer than 1 μm, the edge of the resist can bend (similar to Fig. 7.12b), so it is suggested to make "crutches" with a width of at least 0.2 μm between the windows.

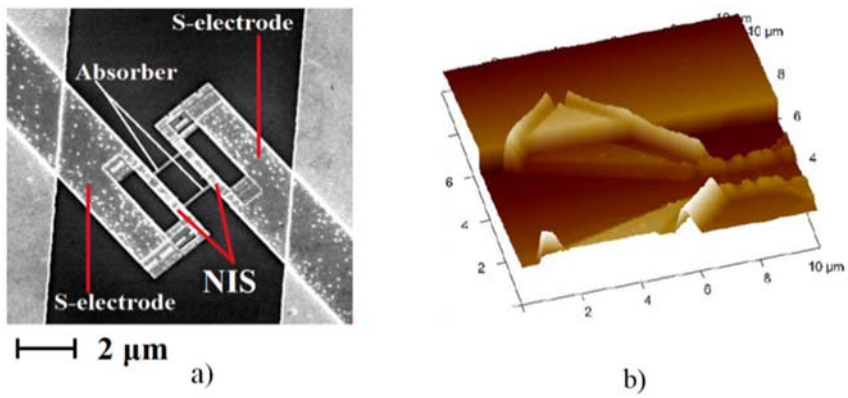


Fig. 7.4. Images of different SINIS bolometers, made by Dolan's technology a) SEM image of SINIS bolometer; b) AFM image of SINIS bolometer of wrong design with slant superconducting electrodes.

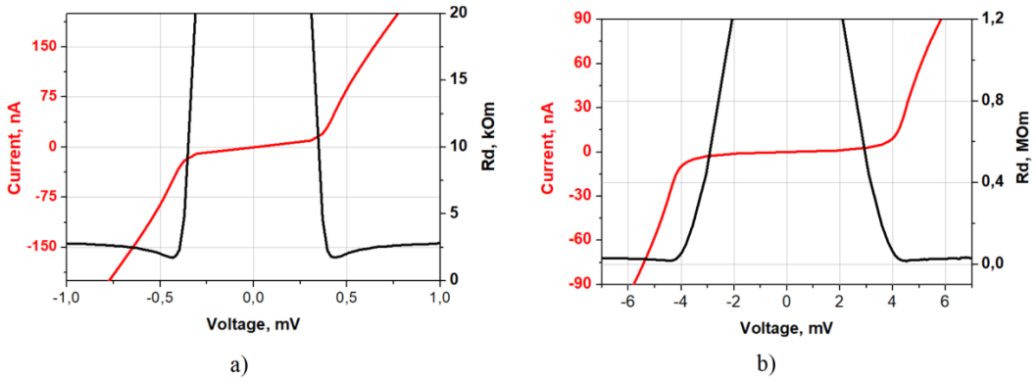


Fig. 7.5. Measured I-V curves and dynamic resistance of fabricated samples at a temperature of 280 mK: a) Single SINIS structure (two series connected SIN junctions); b) An array of 25 series connected annular antennas, each containing two SINIS bolometers connected in parallel.

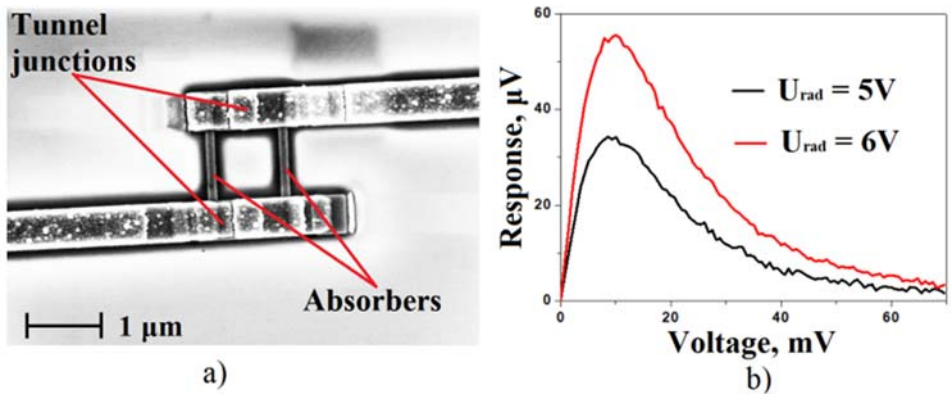


Fig. 7.6. NININ detector [22]: a) – SEM image of the fabricated structure; b) – Response of the array of NININ detectors to incoming radiation at a two heating voltages at the source.

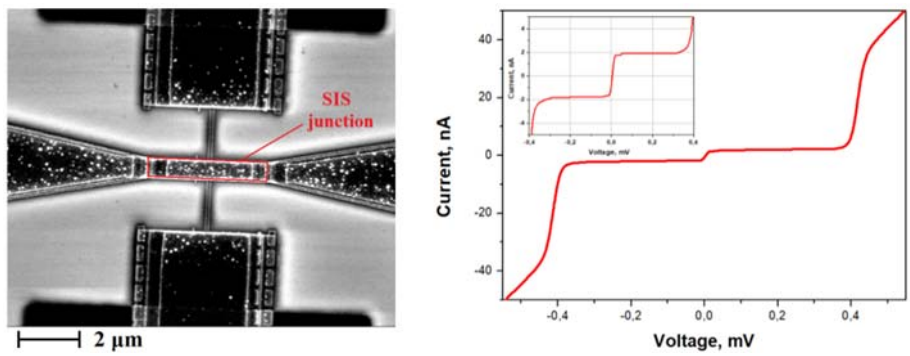


Fig. 7.7. SEM image of the fabricated SIS junction (top) and results of experimental measurements (bottom) [38].

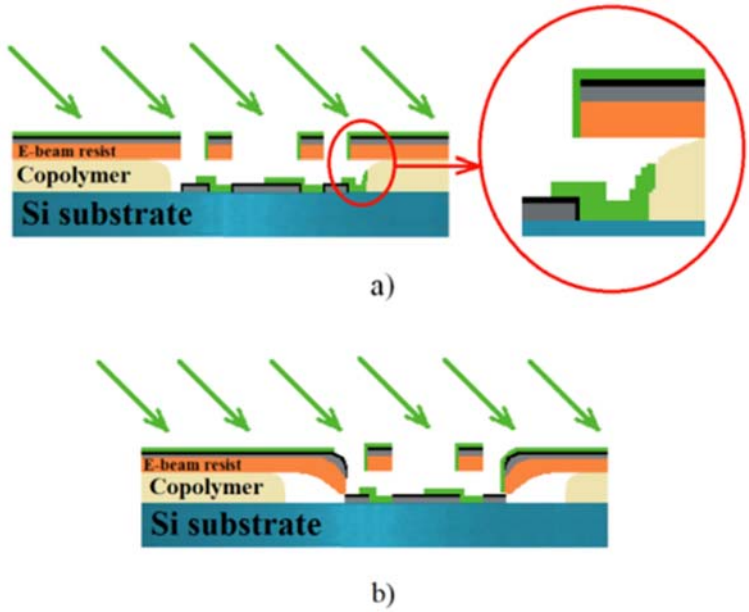


Fig. 7.8. The schematic representation of some of disadvantages of this fabrication technology: a) Deposition on the resist wall; b) Bending of the edge of the resist.

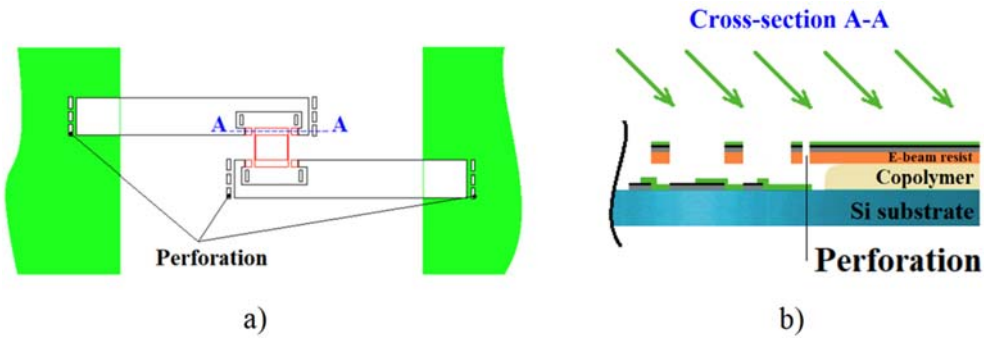


Fig. 7.9. Schematic image and explanation of the perforation: a) Design of layout with explanatory inscriptions; b) Cross-section A-A during shadow evaporation.

7.5. Bridge-free Technology

As noted above, we need to create a large (hundreds and thousands of identical elements) arrays for working under relatively high (tens of picowatts) background load, and therefore we need a reliable technology for fabrication of tunnel structures. Despite the fact that the Dolan's technology has been well developed, it has the disadvantages presented in the previous section. Our experience in fabrication of single SQUIDs by using the technology with suspended resist bridges have shown that for junction with a

width of more than 0.5 μm, the yield of non defective samples is less than 20 %. To avoid this technology problems, a bridge-free technology with deposition into two narrow orthogonal grooves was developed. Currently, this technology is widely used, and some of examples of this fabrication technology are presented in [40-46]. The main addition to initial technology [47-48] is deposition of each film (normal metal and superconductor) at two angles for improving of the contact with the wiring electrodes and for improving of heat sink throught superconductor.

The key element of bridge-free technology is in separate deposition of two different layers of metals into two orthogonal deep grooves in a two-layer resist. While the deposition of the first film along the first groove does not deposit into the orthogonal groove, since the deposition angle is chosen so that in the direction of the second groove, the deposition occurs on the resist wall with subsequent removal together with the resist. Similarly, when another film is deposited along the second orthogonal groove after rotation of the substrate by 90° around the axis, film is deposited only in the second groove. The using of separate exposure for two resist layers allows to accurately control the size of the undercut of profile and to avoid the formation of vertical walls of films after their deposition.

A schematic image of the fabricated structure is shown in Fig. 7.14. The most successful combination of resists is Copolymer MMA/PMMA. When the ARP resist was used instead of PMMA, often there were problems with its "bending" and the corresponding low quality of the fabricated structures. The grooves for deposition were exposed with a high dose (400 μC/cm^2). For forming of a controlled undercut, the necessary areas were exposed with a low dose (75 μC/cm^2) that does not affect the upper resist layer. Into the first groove the layer of normal metal is deposited at angle of +45°. For improving the contact, it was also deposited at opposite angle – 45° (Fig. 7.14 b, left). The thicknesses of the deposited films are: Iron – 2 nm, Aluminium 20 and 30 nm. In an orthogonal groove, a layer of normal metal is deposited on the resist wall and does not fall into it (Fig. 7.14 b, right). The oxidation (Fig. 7.14 b) is performed at the same parameters as for the previous technologies. After that, the substrate is rotated by 90° around the axis for deposition of the superconductor film into an orthogonal groove. Deposition is carried out similarly to a normal metal film; the result of deposition is schematically shown in Fig. 7.14 d. The thicknesses of the deposited superconducting aluminium films are 60 and 80 nm. The images of fabricated samples of NIS junctions by using this bridge-free technology and the results of experimental measurements are presented in Fig. 7.15. This technology can also be used for creation of SINIS bolometers integrated into superconducting antennas in a single process cycle (Fig. 7.16). Also, this approach is convenient for making structures like SQUID – Fig. 7.17 a. Fabrication of a SQUID using the technology with suspended resist bridges (Fig. 7.17 b) is possible only with a small width of the bridge (up to 0.5 micrometers). There are also problems, as can be seen in the image, with the deposition of the material on the resist wall, which is not completely removed after lift-off. The result of measurement of the single SQUID that was made by bridge-free technology is presented in Fig. 7.17 b.

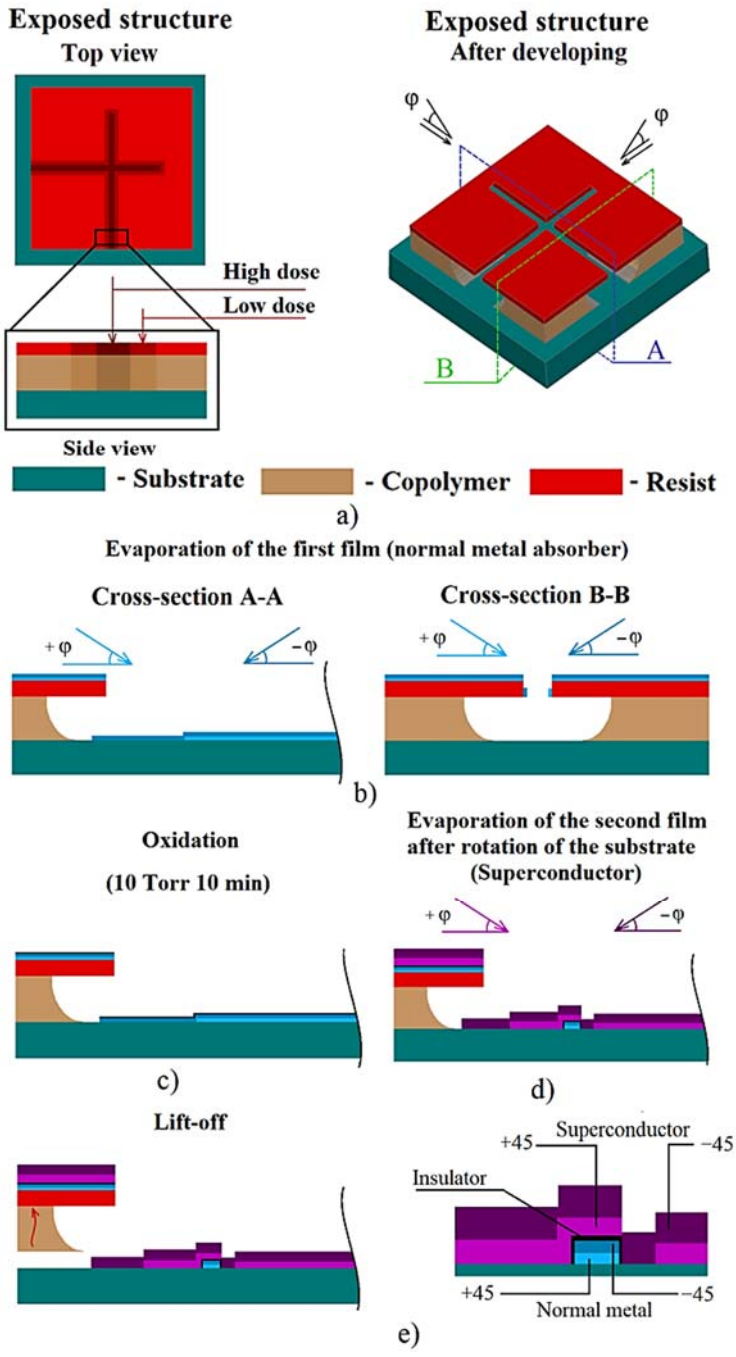


Fig. 7.10. The schematic image of bridge-free cross deposition [47-49]: a) Exposed structure before (left) and after development (right); b) Deposition of the normal metal film along the first groove: cross-section A-A (left) and orthogonal groove cross-section B-B (right); c) Oxidation of the normal metal film for tunnel barrier formation; d) Deposition of the superconductor film after rotation of the substrate by 90º around the axis; e) Lift-off after the structure deposition (left) and an enlarged fragment of the deposited structure (right).

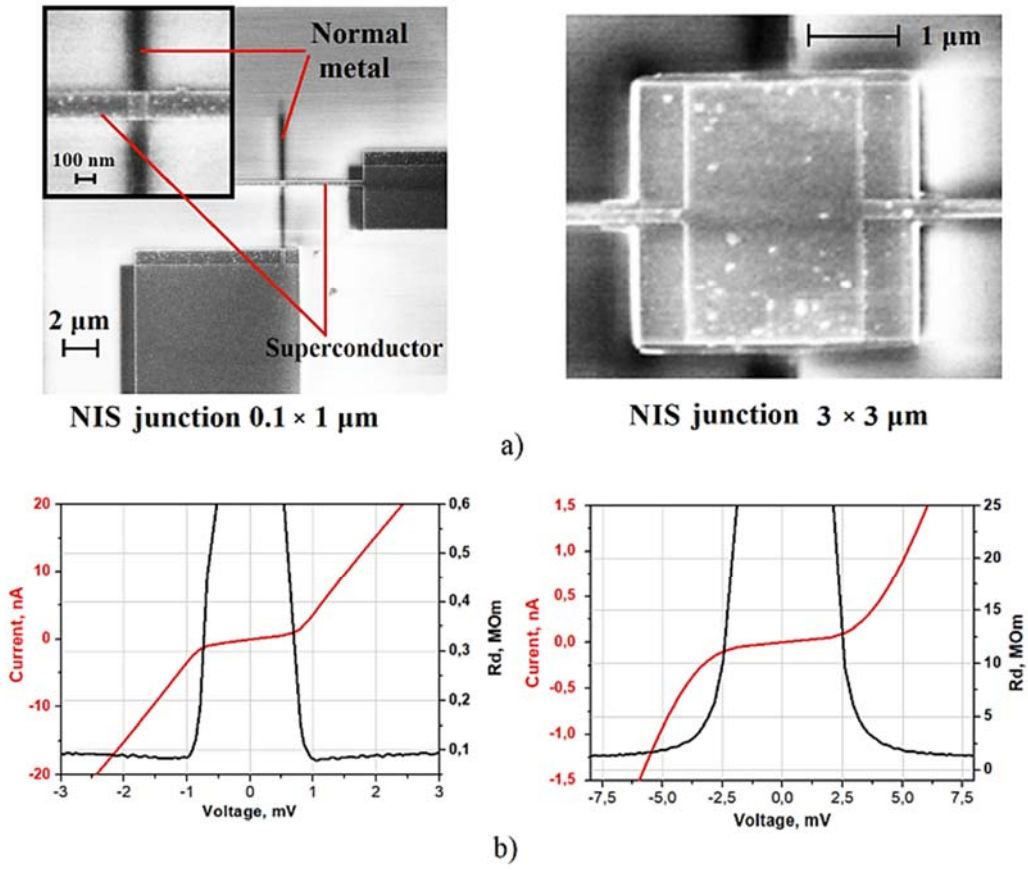


Fig. 7.11. NIS structures made by bridge-free technology: a) SEM image of SIN junction with an area of 0.1×0.1 μm (left) and 3×3 μm (right); b) I-V curves and differential resistance of four series NIS junctions with an area of 0.2×0.2 μm (left) and a chain of 20 junctions with an area of 0.1×0.1 μm (right).

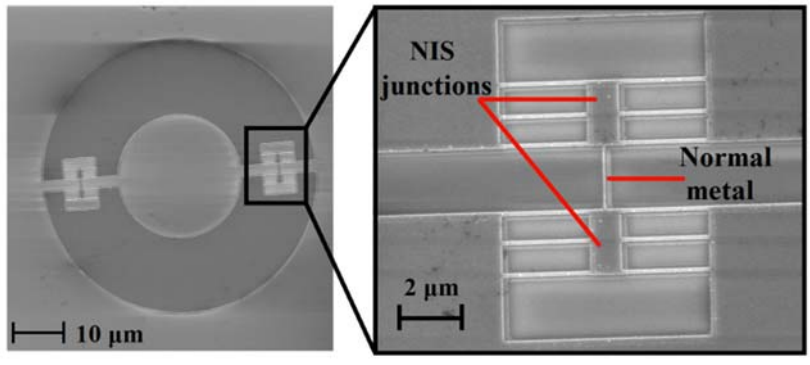


Fig. 7.12. SEM image of a superconducting aluminium antenna (left) with two integrated SINIS bolometers (right).

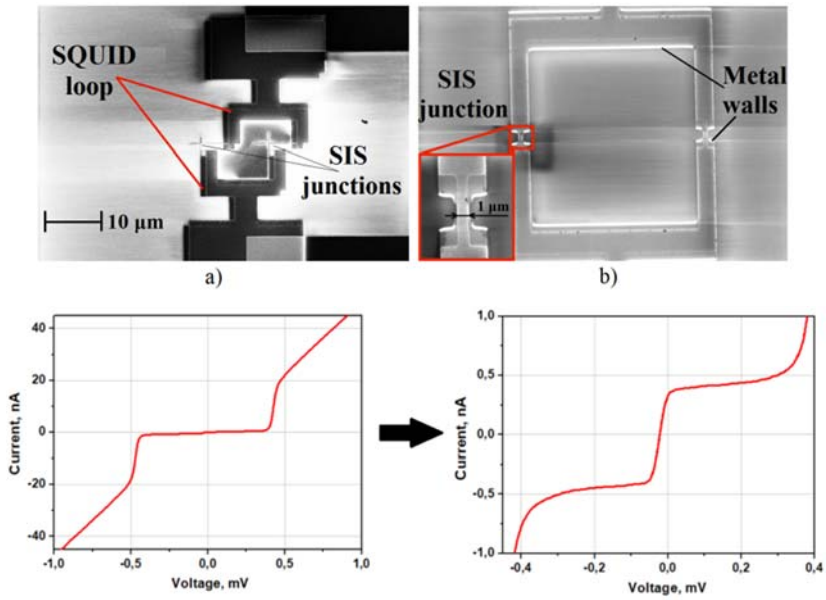


Fig. 7.13. SQUID: a) Made by bridge-free technology; b) Made by technology with Dolan's bridges; c) The result of measurements of single SQUID with a 10×10 μm loop and 0.15×0.15 μm junctions.

7.6. Fabrication Technique of SINIS Detectors with a Suspended Absorber by a Direct Write Lithography

The need to fabricate detectors with a suspended absorber is related intended to reduce the losses of the received signal sinking into the substrate, and to increase the quantum efficiency of such receiver. The first SINIS detectors with a suspended absorber were presented in [50-51].

The idea of the technology [52] is following: in one vacuum cycle a three-layer superconductor/insulator/normal metal film (Fig. 7.18 a) is deposited at normal angle. Film thicknesses are: aluminum is about of 70 nm and normal metal – 30 nm. In the next step, the window in resist is opened by optical lithography at the area where it is intended for aluminum etching under the absorber (Fig. 7.18 b). The aluminum etching is made in a weak alkaline solution (for example, 10 % KOH or photoresist developer like MF-CD-26). After that the resist is removed. The results of measurement of NIS structures (Fig. 7.19 a, black curve) that was made by this technology showed that the superconducting gap is suppressed due to proximity effect (the value must be 200 μV for a single aluminum junction and, accordingly, 400 μV for a single SINIS structure). To avoid such suppression of superconductivity the additional technological step was added – etching of normal metal (Fig. 7.19 b). It's allowed us to get junctions of a good quality (Fig. 7.19 a, red curve), but the additional technological step reduces the yield of usable samples. Also, such etching is only possible for copper (in nitric acid) and therefore we are limited in the choice of the absorber materials (the using of high-resistance materials

like hafnium or palladium is preferable). Another disadvantage of copper is that the material is too soft and during the etching of aluminum, the bridge can sag (Fig. 7.20 a). The example of successful realization of such bolometer is presented in Fig. 7.20 b.

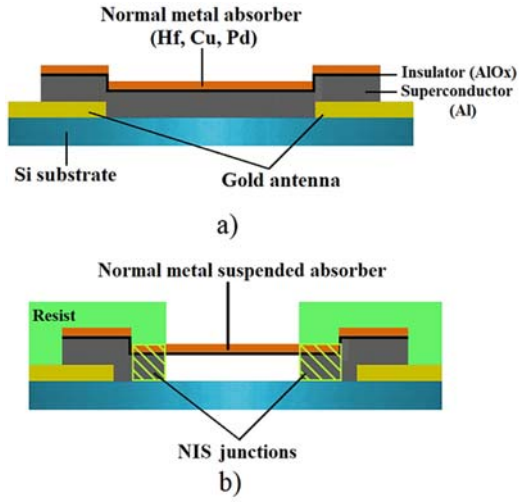


Fig. 7.18. Schematic image of fabrication of SINIS detector with suspended absorber: a) SIN junction of a large area made by direct lithography; b) Resistive mask for etching and the result of aluminum etching throught open window in resist.

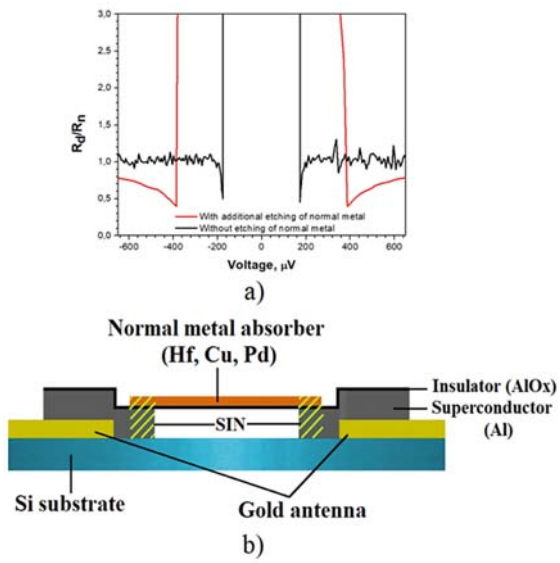


Fig. 7.19. Additional etching of normal metal: a) Experimentally measured dynamic resistance of samples with and without additional etching; b) Schematic image of a SINIS detector with a suspended absorber and additional etching of normal metal.

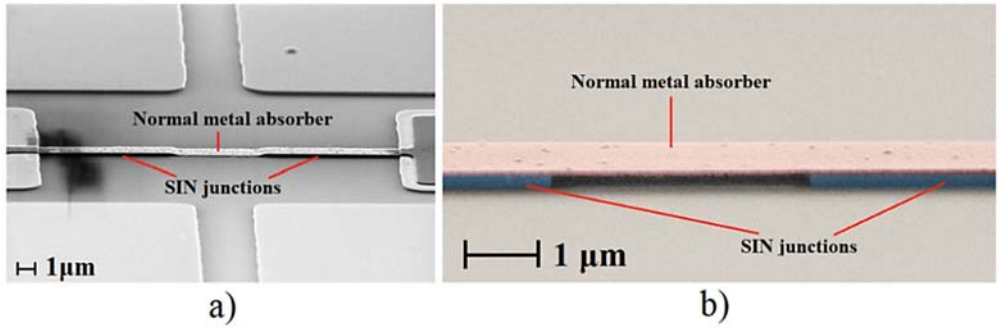


Fig. 7.14. SEM image of fabricated SINIS structures with a suspended absorber: a) Sagging bridge made of copper after aluminum etching; b) Suspended bridge made of hafnium [50].

7.7. Fabrication Technique of SINIS Detectors with Suspended Absorber by a Shadow Evaporation of Normal Metal

To avoid the problems with normal metal etching, as shown in the previous section, we add a shadow evaporation method to form a normal metal absorber only in the given area. The schematic image of structure deposition is shown in Fig. 7.21. For this technology, it is necessary to choose resists of a large thickness (in total, not less than 900 nm). Schematically, the exposed and developed structure in a two-layer Copolymer MMA/PMMA is given in Fig. 7.21 b (left). The first step is deposition of a superconductor (aluminum) at a right angle and oxidation of it for making of the insulator layer (Fig. 7.21 b, right). The oxidation parameters are the same as for the other technologies presented above. Next, as shown in Fig. 7.21 b, a film of normal metal (any) is evaporated at the angle of 45º. The film of absorber is formed in the required area (wider than other), due to the fact that in a narrow area (width of about 1 mkm, it's depending on the required designg and thickness of the resists), the material is deposited on the resist wall (Fig. 7.21 g) and then removed with the resist in the lift-off process. The etching process is the same as in the previous section. The images of fabricated samples are shown in Fig. 7.22 and results of measurements in Fig. 7.23.

7.8. Evolution of the Theory and Characteristics of the SINIS Detector with the Development of Its Fabrication Technology

The development of technology of SINIS structures has progressed in several stages with according to available methods and development of understanding of the physicsl processes in such structures. The typical SINIS detector consists of two NIS junctions connected in series with a normal metal absorber (N). The schematic image of different constructions of detectors based on SINIS structures are shown in Fig. 7.24.

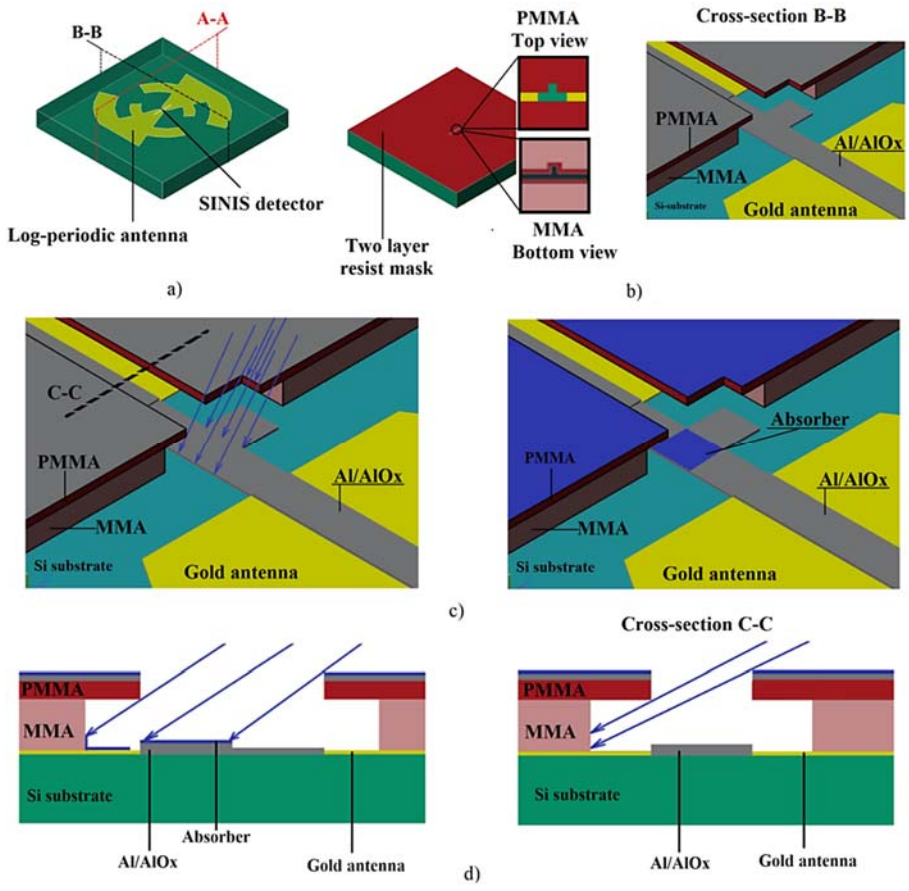


Fig. 7.15. Schematic image of fabrication of SINIS bolometer with a suspended absorber with shadow evaporation: a) Schematic illustration of a log-periodic antenna with integrated SINIS detector; b) The resistive mask for the deposition of a SINIS structure (left) and 3D view of this resistive mask after evaporation of the superconductor at right angle and oxidation; c) Schematic representation of the deposition of the normal metal layer at an angle; d) Schematic explanation of the deposition of a normal metal layer in a wide area (left) and a narrow area (right), where the material is deposited on the resist wall

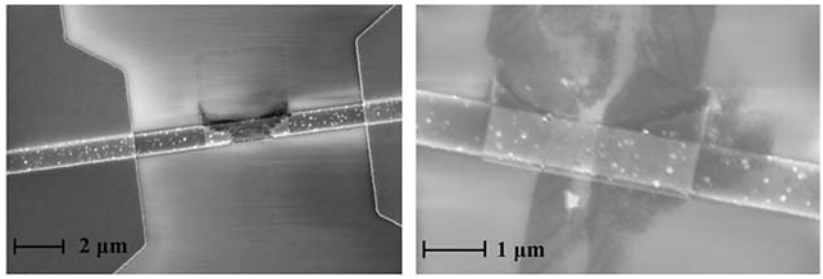


Fig. 7.16. SEM image of fabricated samples of SINIS detectors with a suspended absorber made of hafnium (left) and palladium (right).

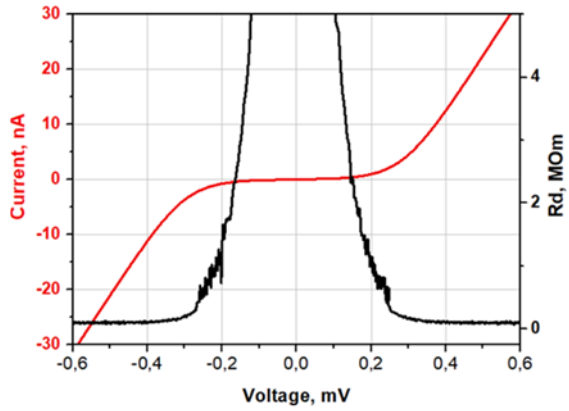


Fig. 7.17. The results of measurements of SINIS detectors with a suspended absorber fabricated by shadow deposition of absorber.

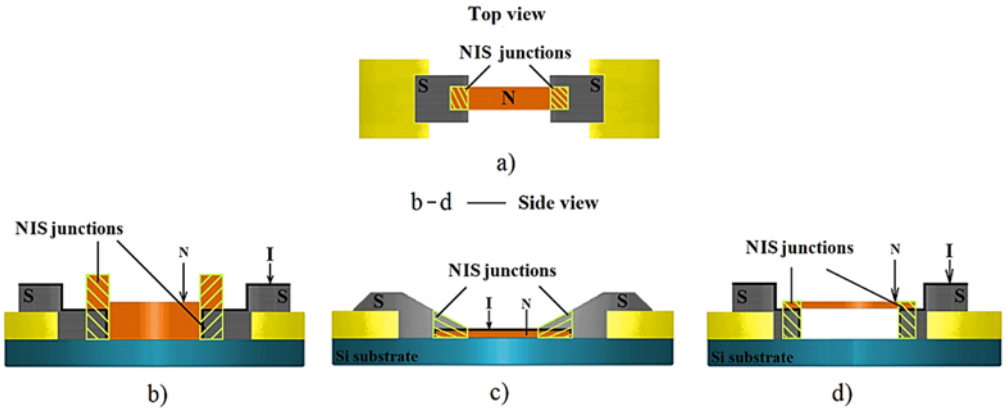


Fig. 7.18. Schematic image of different constructions of the SINIS detector: a) Top view; b) SINIS bolometer made by direct lithography technique; c) SINIS bolometer made by Dolan's technology; d) SINIS detector with a suspended absorber.

The simplest SINIS detector (Fig. 7.24 b) was made by direct lithography technique with separate deposition of SIN junctions and the absorber. According to this technology, the each next layer should be thicker than the previous one, that there are no gaps at the ends of films, so the upper layer of the absorber was quite thick. To some extent, the sensitivity of such bolometer can be increased by reducing of the volume of the absorber. This is noted in the concept of a cold electron bolometer (CEB) [53-54]. Also, the authors of this work approve that the effect of electron cooling in such structures contributes to increasing of sensitivity. Into this, the development of Dolan's technology (Fig. 7.24 b), which allows creating of a submicrometer absorber and superconducting electrodes of a large area in one technological cycle, becomes relevant for improving of electron cooling. In semiclassical theory, it was assumed that the assesment of the sensitivity of a bolometer under the influence of high-frequency radiation is equivalent to heating with a direct current of the same power. Sensitivity assessments were performed using the formula:

$$dV/dP = 2k/(e\Sigma\nu T_e^4), \quad (7.1)$$

where k is the Boltzmann constant, e is the electron charge, Σ is the electron-phonon coupling constant in absorber, ν is a volume of the absorber, T_e is an electron temperature. To substitute the values $\Sigma = 1.5$ nW/μm^{3}K^5, $\nu \approx 10^{-20}$ м^3, $T_e = 0.3$ К, we can get sensitivity about 10^9 V/W. In practice, these values were obtained by heating the absorber with a direct current. But, in the case of RF signal irradiation, the values are at least an order of magnitude worse. In reality, at the frequencies higher than 50 GHz, absorption has a quantum nature. Theoretically it was demonstrated in the later theory [55-56]. According to this theory, both the volume of the absorber and electron cooling are not fundamental, and for achievement of high sensitivity the structures with high resistance and with small thermal contact of the absorber with the substrate and superconducting electrodes are optimal. Consider the mechanism of quantum absorption in the case of irradiation by the signal with a frequency of 350 GHz Fig. 7.25 [57-58]. When an electron absorbs a photon with an energy much higher than the thermal energy, the electron energy will correspond to the electron temperature $hf = kT_e$ about 15 K. The time of electron-electron interactions at this temperature is much longer than the time of electron-phonon interactions. As a result, a high-energy photon is created. This phonon has three ways for relaxation: to the substrate, to superconducting electrodes, or to interact with electron system. In the last case high-energy pair comprising electron with energy hf/2 above the Fermi level and hole with negative energy -hf/2 is created. Excited electron hf/2 creates a phonon with equivalent temperature 7 K, again electron-hole pair is created, now with energy hf/4 each, or 3 K. At such temperature electron-electron interaction become dominating, that leads to creating of two electrons and hole with energy hf/12. After that only electron-electron interactions are involved in multiplication of excited electrons. One of the first works on the estimation of non-thermal optical response of SINIS detectors is [59].

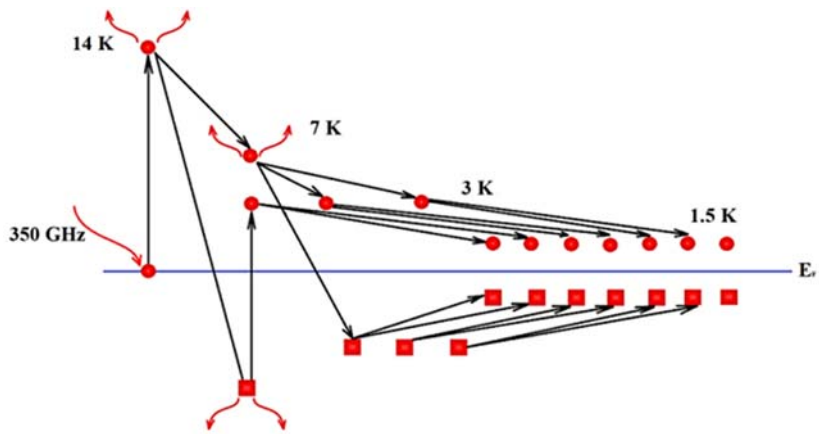


Fig. 7.19. The process of thermalization of a quantum of radiation with a frequency of 350 GHz.

The process of phonon escape [58] is very important in the case of high frequencies. For transverse phonons propagating nor-mal to absorber surface, the escape from the absorber to the substrate is $\tau_{tr} = t_{abs}/v_{sound} = 5$-10 ps, and for longitudinal phonons propagating along

the absorber, it can reach $\tau_l = l_{abs}/v_{sound}$ = 0.1-0.2 ns for a longitudinal size of 1 μm and the speed of sound 3-5×10^3 m/s. For an absorber on a substrate, τ_{tr} and a fast escape of phonons into the substrate will prevail, while for a suspended absorber that does not have contact with the substrate, only a slower process with a time constant τ_l remains. Moreover in the case of different materials phonons partly reflected from the boundary. The characteristic time scales analyzed in detail in [59-60] and presented in Table 7.5.

Table 7.5. Dynamics of 350 GHz photon relaxation [58].

Process	Equivalent temperature	Time constant	Number of particles	Phonon and electron escape from absorber
el-ph ph-el el-el	16 K	τ_{ep} = 12 ps τ_{pe} = 0.7 ps τ_{ee} = 0.25 ns	1	Transvers phonons 10 ps, Lateral phonons 1 ns
el-ph ph-el el-el	8 K	τ_{ep} = 0.2 ns τ_{pe} = 2.8 ps τ_{ee} = 1 ns	2	Transvers phonons 10 ps, Lateral Phonon 1 ns
el-ph ph-el el-el	4 K	τ_{ep} = 3.2 ns τ_{pe} = 11 ps τ_{ee} = 4 ns	4	Transvers phonons 10 ps, Lateral phonons 1 ns
el-ph ph-el el-el	2 K	τ_{ep} = 51 ns τ_{pe} = 44 ps τ_{ee} = 16 ns	24	Electron escape τ_{sin} = 40 ns
ph-el	0.6 K	τ_{pe} = 0.5 ns	Escape	Transvers phonons 10 ps
el-el	0.3 K	τ_{ee} = 700 ns	Escape	Electron escape τsin = 40 ns
el-el	0.1 K	τ_{ee} = 6.4 μs	Escape	τsin = 40 ns

The separate question is the influence of electron cooling to the characteristics of the SINIS detector. In the works that are devoted to CEB, it is claimed that due to electron cooling, it is possible to reduce the electron temperature from 300 mK to 100 mK, and thus there is no need to cool down the sample to 100 mK. However, in a recent paper [61], it was experimentally shown that the electron cooling is not a method for achievement of the maximum sensitivity of the detector. The negative effect of electron cooling can significantly reduce the quantum efficiency of the detector (less than 1) due to the fact that the excited electrons are removed from the absorber and their multiplication does not occur. The increasing of the resistance of the tunnel junctions is reduced heat losses to the electrodes. As shown in [56], the optimal resistance of the NIS junctions is 5 kOm. Thus, the estimation of the characteristics of the SINIS detector should be based on kinetic equations and collision integrals.

In this regard, the SINIS detector with a suspended absorber Fig. 7.24d was fabricated and experimentally studied [50-51, 57-58]. This allowed us to radically improve the thermophysical parameters of the SINIS detector – the quantum efficiency from one electron per quantum increased to 15 electrons per quantum at a frequency of 350 GHz. The measured voltage and current responses are shown in Fig. 7.26.

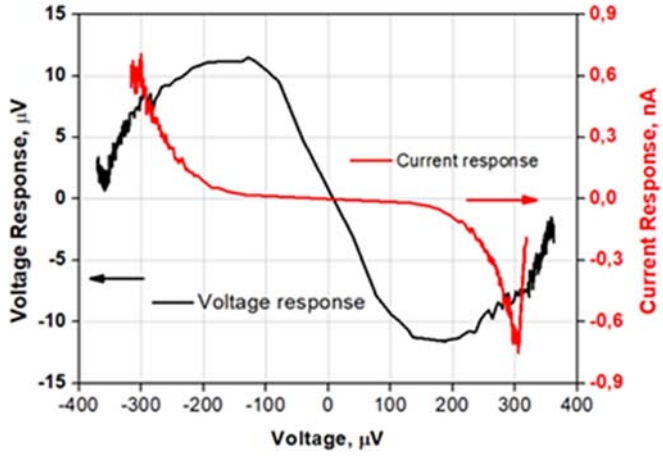


Fig. 7.20. The measured voltage and current responses of the SINIS bolometer with a suspended absorber to the black body radiation at a temperature of 4.5 K.

7.9. Conclusions

An overview of different methods for fabrication structures based on tunnel junctions: SINIS and NININ detectors with a suspended absorber and an absorber on a substrate, SIS junctions, SQUIDs with aluminium SIS junctions are presented in this chapter. Also, advantages and disadvantages of presented technologies were considered.

The change of the SINIS detector theory from the semiclassical theory based on the heat balance equation to the theory of quantum absorption based on the kinetic equation and the collision integral was done. For the SINIS detector fabrication the most promising technology is formation of suspended absorber, which allows to realize a high quantum efficiency of cryogenic bolometers. The quantum efficiency of SINIS detector was increased from 1 electron per quantum to 15 electrons per quantum at a frequency 350 GHz. The presented technologies, which include the original developments of the authors, can be widely used for fabrication of different devices based on tunnel structures and will be relevant in such promising areas as a creation of high sensitive receiving systems for astronomy, quantum computers, systems of precise quantum measurements, telecommunications and other areas of science.

Acknowledgements

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Chapter 8

CMOS UWB Differential Impulse Radio Transmitter

Jin He and Shuo Li

8.1. CMOS UWB Fifth-derivative Gaussian Pulse Generator

8.1.1. Introduction

Ultra-wideband Impulse Radio (UWB-IR) technology employs extremely short pulses of less than a nanosecond as its transmission signals, which are strictly demanded to be robust against the interference from existing wireless systems as well as not to interfere with these systems. Therefore, it is important for UWB signals to satisfy the FCC spectrum regulation that regulates the power spectral density (PSD) of UWB signals below -41.3 dBm/MHz within the 3.1-10.6 GHz frequency band [1]. Hence, the high fidelity of pulse shape must be guaranteed by the pulse generator.

As a key building block of UWB-IR systems, the pulse generator is required not only to generate accurate pulse to meet the FCC spectrum mask, but also to possess low-cost, low-power, and low-complexity features. Normally, the Gaussian pulse and its derivatives are preferable choices in published literatures. Up to date, there are several methods involving carrier-free and carrier-based pulse generation. For carrier-free pulse generation, an analog method is used to easily produce the first- or second-derivative Gaussian pulse [2, 3], however an additional filter is required to shape the pulses to satisfy the FCC spectrum mask. A digital method is employed to yield an accurate multi-cycle pulse in [4], though the generated pulse meets the FCC spectrum regulation without an additional filter, it is not easy to control the phase and the amplitude of each triangle precisely and combine all triangles into a desired pulse shape smoothly. For the purpose of easily obtaining the multi-cycle pulse, the carrier-based pulse generation is adopted. One method is that a sinusoidal carrier from an oscillator is multiplied by a triangular envelope to generate the desired pulse. Hence, the bandwidth and the center frequency of the pulse are determined by the oscillator whereas the spectrum of the pulse is controlled

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by the envelope [5]. The other is that a sinusoidal carrier is directly shaped to the multi-cycle pulse by switching on/off the oscillator, which achieves low complexity and low power consumption [6].

In this section, a fifth-derivative Gaussian pulse generator is implemented using a 0.18-μm CMOS process with low power consumption and low circuit complexity. The section is organized as follows: In Section 8.1.2, the fifth-derivative Gaussian pulse generator is introduced. The measurement results that verify the design are discussed in Section 8.1.3. Finally, the conclusion is drawn in Section 8.1.4.

8.1.2. The Fifth-derivative Gaussian Pulse Generator

Though Gaussian pulse and its derivatives are usual options used as transmission signals for UWB systems because they do not require carrier modulation, researches show that, for a Gaussian pulse, a minimum derivative of five can inherently comply with the FCC UWB indoor power spectrum regulation [7]. The fifth-derivative Gaussian pulse can be mathematically expressed as:

$$G^5(t) = A\left(-\frac{t^5}{\sqrt{2\pi}\,\sigma^{11}} + \frac{10t^3}{\sqrt{2\pi}\,\sigma^9} - \frac{15t}{\sqrt{2\pi}\,\sigma^7}\right)\exp\left(-\frac{t^2}{2\sigma^2}\right), \tag{8.1}$$

where A and σ are the parameters set to satisfy the FCC power spectrum regulation for indoor application.

Recently, several research works have been reported to develop the fifth-derivative Gaussian pulse generators in CMOS. For instance, Kim, et al firstly implemented a fifth-derivative Gaussian pulse generator with a 0.5-μm CMOS process [8]. The design exhibits simple all-digital and low-power characteristics. However, the measured pulse width is 2.4 ns, which will decrease the center frequency and -10-dB bandwidth of the pulse comparing the results stated previously in [9]. Xie, et al employed a 0.18-μm CMOS process to realize an adjustable fifth-derivative pulse generator that can achieve the shortest pulse width of 240 ps, but the inferior amplitude of 54 mV peak to peak and power consumption of 3.6 mW at the 1.8 V supply voltage [10].

In this section to avoid the deficiencies in the above two designs, a fifth-derivative Gaussian pulse generator is designed [8]. The schematic of the pulse generator is shown in Fig. 8.1, which consists of logic gates based triangular pulses generating stage, output stage, and a 50 Ω load. To produce the fifth-derivative Gaussian pulse, the voltage on nodes A+ and C+ forms the negative-peak triangular pulse from VDD to GND whereas the voltage on nodes B+ and D+ generate the positive-peak triangular pulse from GND to VDD. The peak to peak value of each triangular pulse is the same and delay time of four pulses is adjusted to ensure their proper phase relations by tuning the size and number of inverters. When the four triangular pulses operate on the gates of transistors M_1-M_4 constituting the output stage, the four triangular pulses are inverted by output stage and integrated into the fifth-derivative Gaussian pulse successfully on node E+, the amplitude of the fifth-derivative Gaussian pulse can be changed by tuning the size of transistors M_1-M_4. The output stage has virtually no static power dissipation as only one MOS

transistor switching on during operation. Likewise, Phase inverse Gaussian pulse of node E+ can be obtained by alternating corresponding locations of NANDs and NORs. The generated fifth-derivative Gaussian pulse can directly drive the antenna. The key element values are listed in Table 8.1.

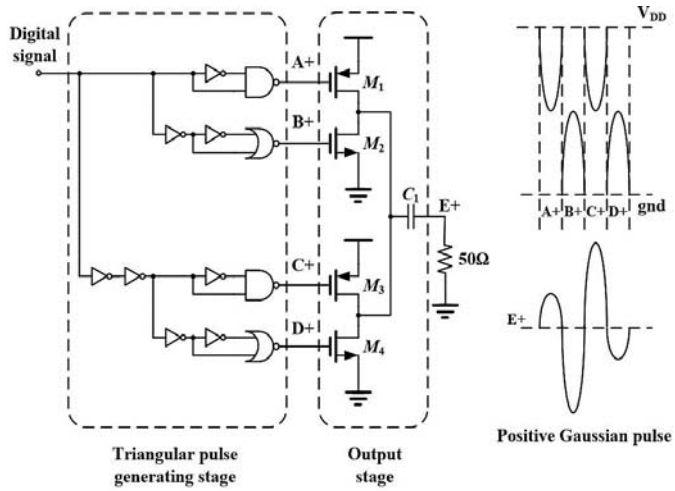

Fig. 8.1. Schematic of the fifth-derivative Gaussian pulse generator.

Table 8.1. Key element values.

M_1	M_2	M_3	M_4	C_1
20 μm/0.18 μm	6 μm/0.18 μm	15 μm/0.18 μm	6 μm/0.18 μm	1 pF

8.1.3. Measurement Results and Discussions

Cascade Summit 12000-Series Probe Station and Cascade Microtech's 100-μm GSG probes were used for on-wafer measurement. A Tektronix DG2020A data generator was employed to generate the input signal, whose frequency is 50 MHz corresponding to the period of 20 ns. A Lecroy 8600A oscilloscope was adopted to measure the output. The measurements were performed at the load impedance of 50 Ω including the parasitic of the signal pads.

The fifth-derivative Gaussian pulse generator was implemented with a 1.8-V, 0.18-μm CMOS process. The die microphotograph of the chip is shown in Fig. 8.2. The whole chip area is 408 μm × 310 μm including pads and the core area is 217 μm × 121 μm because of its all-digital design. Fig. 8.3 displays the measured fifth-derivative Gaussian pulse train at the output of the pulse generator. The pulse repetition period is 20 ns. The measured pulse shape given in Fig. 8.5 agrees well with the simulated one shown in Fig. 8.4. The measured pulse has a peak-to-peak amplitude of 158 mV with a pulse width of 800 ps whereas the simulated pulse has a peak-to-peak amplitude of 300 mV and a

pulse width of 730 ps. The discrepancy between the simulated and measured pulses is attributed to the following reasons. First, note that there is a 3-dB difference in the amplitudes. Second, the loss from the probe, coaxial cable, and SMA connector accounts for 1.5 dB. Third, the other 1.5-dB loss may be due to the parasitic effect of wire interconnects and signal pads. They will not only reduce the pulse amplitude but also cause delay and distortion to the pulse. Last, it is obviously observed that ringing occurs in the measured pulse owing to the parasitic *LC* network formed by wire interconnects and signal pads. Hence, interconnects for the pulse generator must be designed as short as possible to minimize the parasitic effect. The parasitic capacitance of the signal pads must be minimized.

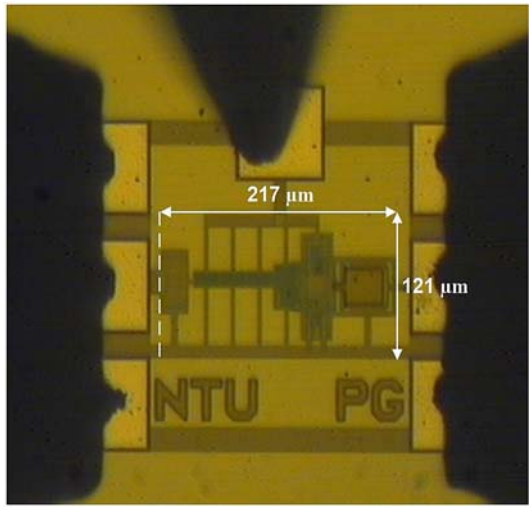

Fig. 8.2. Die microphotograph of the fifth-derivative Gaussian pulse generator.

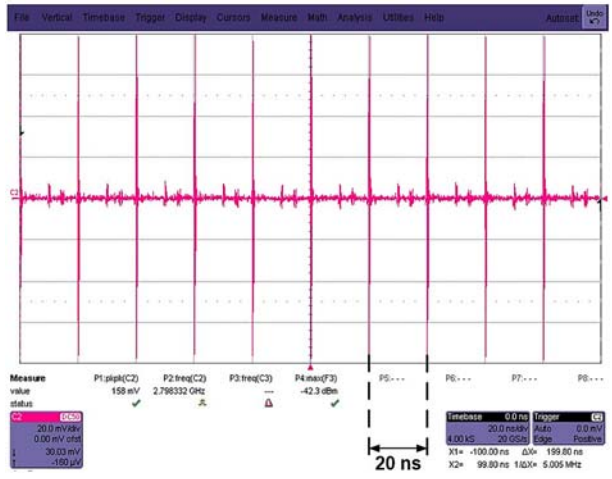

Fig. 8.3. The measured fifth-derivative Gaussian pulse train.

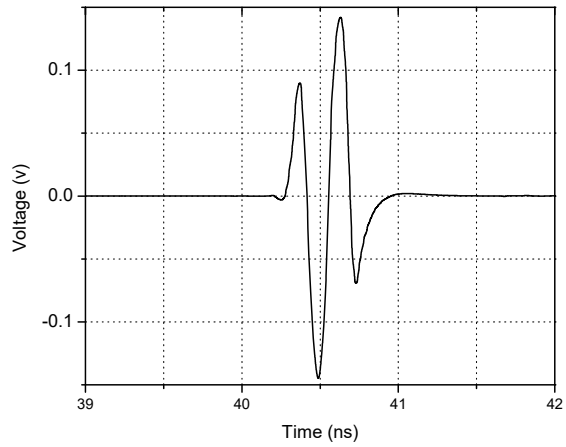

Fig. 8.4. The simulated fifth-derivative Gaussian pulse.

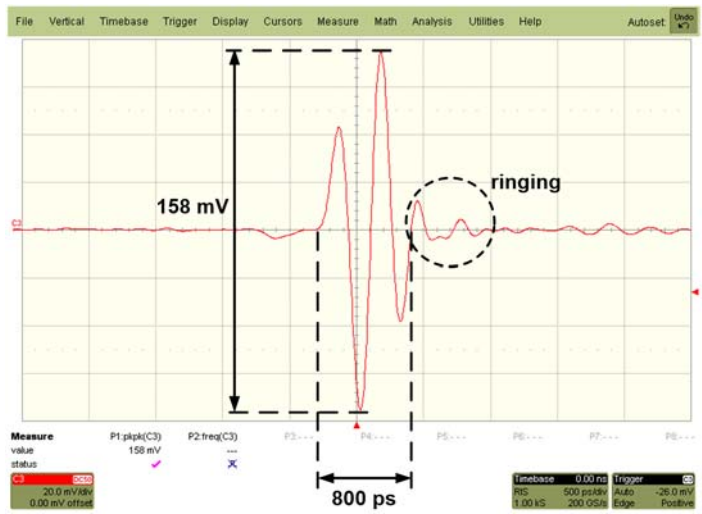

Fig. 8.5. The measured fifth-derivative Gaussian pulse.

The performance of the fifth-derivative Gaussian pulse is mainly determined by the delay time of four triangular pulses as mentioned previously, and therefore is affected by process, voltage, and temperature (PVT) variation. The impact of PVT variation on the manufacturability of the pulse generator was also investigated by post-layout simulations. Table 8.2 shows the simulated performance of the fifth-derivative Gaussian pulse vs. PVT variation. In Table 8.2, besides the above performance of the pulse simulated at the typical case with the corner of TT mode (normal threshold voltage of pMOS and nMOS), the supply voltage of 1.8 V, and the temperature of 27 ºC, the pulse achieves amplitude of 330 mV peak to peak with a pulse width of 410 ps at the best case with the corner of FF mode (low threshold voltage of pMOS and nMOS), the supply voltage of 2 V, and the temperature of –40 ºC; the pulse has a peak-to-peak amplitude of 210 mV and a pulse

width of 850 ps at the worst case with the corner of SS mode (high threshold voltage of pMOS and nMOS), the supply voltage of 1.6 V, and the temperature of 110 ºC. In both case, the generated pulses also achieve precise shapes, which are sufficient for receiver to decode the data information. Therefore, the yielded fifth-derivative Gaussian pulse is robust to sustain PVT variation.

Table 8.2. The Simulated Performance of the Output versus PVT.

P	V (V)	T (ºC)	The fifth-derivative Gaussian pulse	
			Vpp (mV)	Pulse width (ps)
FF	2	–40	330	410
TT	1.8	27	300	730
SS	1.6	110	210	850

The power spectral density (PSD) of the measured pulse complies with the FCC spectrum mask, which is shown in Fig. 8.6. It is observed from Fig. 8.6 that the center frequency is around 5.2 GHz with the peak value of -49 dBm/MHz and the -10-dB bandwidth is 4.6 GHz (from 2.6 to 7.2 GHz). Owing to the fact that the pulse generator is usually connected to the outside world through the antenna, the impedance matching of 50 Ω should be considered between them during the course of the design so that the power from the pulse generator can be maximally delivered to the antenna, the return loss (S11) on node E+ is presented in Fig. 8.7, where -10-dB bandwidth is 7.5 GHz (from 2.5 to 10 GHz), covering the PSD frequency bands of the generated pulse. At a supply voltage of 1.8 V, the average power consumption of the chip is 0.6 mW at a pulse repletion frequency of 50 MHz. The performance summary of the fifth-derivative Gaussian pulse generator and comparison with recently reported generators are given in Table 8.3.

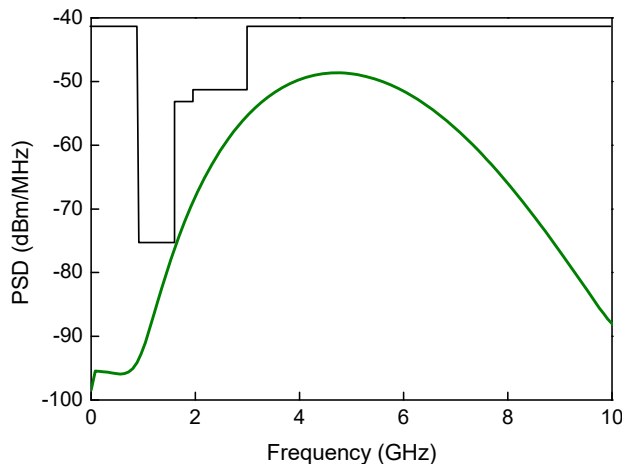

Fig. 8.6. The power spectral density of the measured fifth-derivative Gaussian pulse.

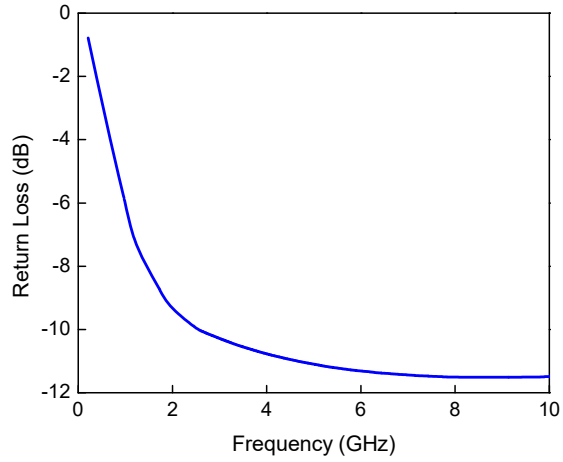

Fig. 8.7. The return loss (S_{11}) on node E+.

Table 8.3. Performance Summary and Comparison.

References	Technology (µm)	Die Area (mm^2)	Power Dissipation (mW@MHz)	Peak Amplitude (mV_{pp})	Pulse Width (ns)
[8]	CMOS 0.5	0.18	1.16@20	148	2.4
[10]	CMOS 0.18	0.13	3.6@100	51	0.42
This work	**CMOS 0.18**	**0.03**	**0.6@50**	**158**	**0.8**

8.1.4. Conclusion

A CMOS fifth-derivative Gaussian pulse generator is presented in this section. The pulse generator was fabricated using a 1.8-V, 0.18-µm CMOS process. The chip possesses a small core area of only 0.03 mm^2 and a low average power dissipation of 0.6 mW at a pulse repletion frequency of 50 MHz. The generated fifth-derivative Gaussian pulse has a peak-to-peak amplitude of 158 mV with a pulse width of 800 ps, which can automatically meet the FCC spectrum mask for UWB indoor applications without the shaping filter. Hence, the pulse generator can be well applied to UWB systems for featuring low cost, low power consumption, compact circuit design as well as the measured precise pulse shape.

8.2. CMOS UWB Differential Impulse Radio Transmitter

8.2.1. Introduction

As an emerging technology for short-range high-speed personal wireless communications, the UWB radio has developed rapidly since the Federal Communications Commission

(FCC) released the ultra-wideband spectrum of 3.1-10.6 GHz for unlicensed applications in 2002 [1].

The no-carrier nature of the impulse radio can greatly reduce its complexity and ultimately result in low-cost, low-power, and compact designs in CMOS [11-17]. Recently, several CMOS impulse radio transmitters have been reported. For example, Lee, et al designed an impulse radio transmitter that achieved triangular pulses with a peak voltage of 2.8 V at 3.3 V supply voltage. However, a bandpass filter (BPF) is required to regulate the pulses to comply with the FCC spectrum mask [18]. Tao, et al designed another impulse radio transmitter that relied on the drive amplifier to shape and amplify the pulse from the generated digital signal. The disadvantage of this transmitter is need for many inductors that ultimately require a large IC area [19]. Norimatsu, et al designed an impulse radio transmitter with a digitally-controlled pulse generator. It is found that the controlling the phase and the amplitude of each triangle precisely and combining all triangles into a desired pulse shape smoothly were formidable [20].

In this section, a fully integrated differential impulse radio transmitter has been designed based on a 1.8-V 0.18-μm CMOS process. The differential architecture was adopted for its higher linearity, lower offset, and superior immunity to power supply variations and substrate noise attributes [21-23]. The differential 5^{th}-derivative Gaussian pulses were explored because it innately satisfies the FCC UWB indoor power spectrum regulation whilst not requiring a bulky off-chip nor lossy on-chip BPF [24, 25].

In Section 8.2.2, the proposed impulse radio transmitter architecture is described. In Section 8.2.3, the impulse radio transmitter circuits are designed and simulated. The measurement results that verify the design are discussed in Section 8.2.4. Finally, the transmitter is concluded in Section 8.2.5.

8.2.2. Impulse Radio Transmitter Architecture

The design aims to realize an impulse radio transmitter that supports eight channels with a channel data transmission rate of 50 Mbps. Hence, the TH-PPM scheme has 8 possible hopping positions from 0 to 7, with the time delay interval of 2.5 ns for each position in the frame time of 20 ns. The proposed impulse radio transmitter is shown in Fig. 8.8. It mainly consists of a clock generator (CG), a pulse position modulator (PPM), and a pulse generator (PG). The CG includes a voltage-controlled oscillator (VCO), a frequency/2 divider, and voltage-controlled delay lines (VCDL). The PPM has an 8-to-1 multiplexer, a pseudorandom number sequence generator (PNSG), a δ delay cell, and a 2-to-1 multiplexer. The PG produces the 5^{th}-derivative Gaussian pulses.

In the CG, the VCO generates a 100 MHz clock signal, which is halved to produce the system clock of 50 MHz by a frequency/2 divider. The first cell of the VCDL yields the pulse train P_0, and all the pulses are located at the beginning of each 20-ns clock cycle, i.e. pulses occupying the hopping position 0 form the pulse train P_0. The pulse width is set to be 1.5 ns, which is less than the ideal time delay interval of 2.5 ns in order to avoid collisions. The block diagram of the VCDL and the corresponding timing chart are shown

in Figs. 8.9(a) and (b), respectively. It is seen that the P_0 will be accurately delayed for 2.5 ns by the second cell of the VCDL to produce the pulse train P_1 which occupies the hopping position 1. In a similar fashion, the other pulse trains P_2 to P_7 can be generated to occupy the hopping positions 2 to 7, respectively. The delay time 2.5 ns by a delay cell is denoted as T_c. Each pulse train has the same period of 20 ns denoted as T_f.

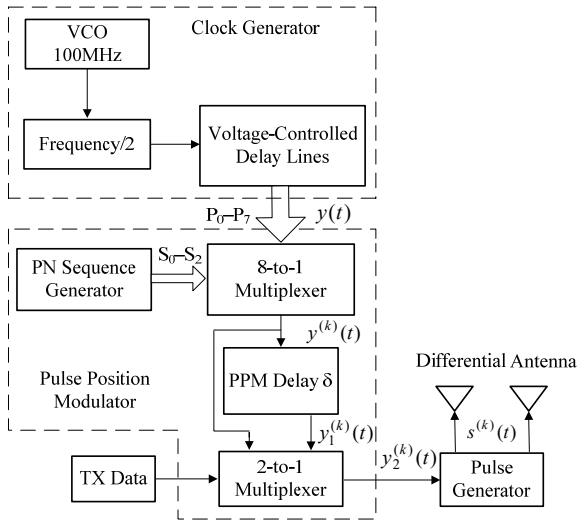

Fig. 8.8. Proposed all-digital transmitter architecture.

The digital pulse train P_0 in Fig. 8.9 (b) can be mathematically expressed as

$$y(t) = \sum_j x\left(t - jT_f\right), \tag{8.2}$$

where x(t) represents the pulse train P_0 that begins at time zero on the 50 MHz system clock, j is the j^{th} digital pulse of the pulse train.

In the PPM, the eight pulse trains P_0 to P_7 are sent to the 8-to-1 multiplexer which is an input selection circuit controlled by the PN sequence generator's output that has three binary bits S_0-S_2 representing a periodic pseudorandom time-hopping code $c_j^{(k)}$ with period N_p where index k denotes k^{th} user. Each code element is an integer in the range of $0 \le c_j^{(k)} < N_h$. Each frame time T_f is divided into N_h positions of T_c seconds. Hence, N_h is 8 occupying the hopping positions 0 to 7 for $T_f = 20$ ns and $T_c = 2.5$ ns in the design. In order to eliminate catastrophic collisions in multiple accessing environments, each user of 8 is assigned a distinct pulse-shift pattern $c_j^{(k)}$ so as to provide an additional time shift of $c_j^{(k)}T_c$ seconds to each j^{th} pulse in the pulse train of k^{th} user [26]. Therefore, the time-hopped pulse train for the k^{th} user is

$$y^{(k)}(t) = \sum_j x\left(t - jT_f - c_j^{(k)}T_c\right) \tag{8.3}$$

Since the period of the time-hopping code $c_j^{(k)}$ is N_p, the waveform described in Eq. (8.3) has a period of $T_p = N_p T_f$. If Eq. (8.3) is shifted for position modulation by the additional time δ of the PPM Delay cell which is employed to distinguish Tx data 0 and 1 [27], the corresponding equation is derived as

$$y_1^{(k)}(t) = \sum_j x\left(t - jT_f - c_j^{(k)}T_c - \delta\right) \tag{8.4}$$

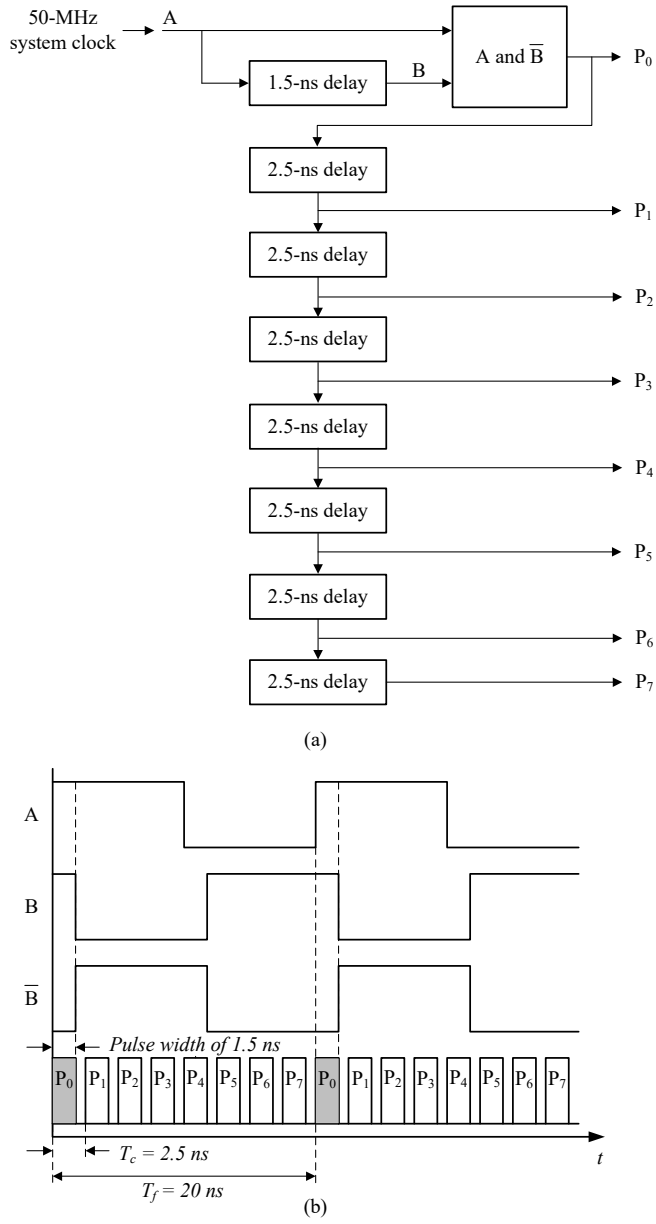

Fig. 8.9. (a) Block diagram of the VCDL, and (b) the corresponding timing chart.

The Tx data $d_j^{(k)}$ is a binary sequence represented by bit 0 or 1. The time-hopped pulse train in Eq. (8.3) and its position- modulated pattern in Eq. (8.4) are fed to the 2-to-1 multiplexer which has the Tx data as its address signal. When the Tx data is 0, the pulse train in Eq. (8.3) will be selected whereas the pulse train of time shift δ in Eq. (8.4) will be chosen when the Tx data is 1. In practice, each data bit is conveyed with N_s pulses, the index $[j / N_s]$ represents the data bit that modulates the j^{th} pulse if a new data bit starts at the pulse of $j = 0$. Therefore, the transmitter transmits the data at a rate of $R_S = 1/(N_s T_f)$. The ultimate output of the 2-to-1 multiplexer can be described as

$$y_2^{(k)}(t) = \sum_j x\left(t - jT_f - c_j^{(k)}T_c - \delta d_{[j/N_s]}^{(k)}\right) \tag{8.5}$$

The pulse train in Eq. (8.5) with time-hopping position modulation and Tx data information will pass through the pulse generator to yield the 5th-derivative Gaussian pulses

$$s^{(k)}(t) = \sum_j w\left(t - jT_f - c_j^{(k)}T_c - \delta d_{[j/N_s]}^{(k)}\right), \tag{8.6}$$

where $s^{(k)}(t)$ and $w(t)$ denote the transmitted signal for the k^{th} user and the 5th-derivative Gaussian function, respectively. The 5th-derivative Gaussian function can be written as follows:

$$w(t) = A\left(-\frac{t^5}{\sqrt{2\pi}\sigma^{11}} + \frac{10t^5}{\sqrt{2\pi}\sigma^{9}} - \frac{15t}{\sqrt{2\pi}\sigma^{7}}\right)\exp\left(-\frac{t^2}{2\sigma^2}\right) \tag{8.7}$$

The final differential 5th-derivative Gaussian pulse trains will be transmitted through a differential antenna, such as a dipole.

8.2.3. Impulse Radio Transmitter Circuits

The proposed impulse radio transmitter in Fig. 8.8 is an all-digital design.

8.2.3.1. Voltage-controlled Delay Lines

The VCDL block is an important component of the Clock Generator, which primarily includes 1.5-ns and 2.5-ns delay lines. Fig. 8.10 shows the schematic of the delay line implemented using a bias circuit, inverter delay cells, and two inverters [28]. The drain currents of transistors M_1 and M_2 in the bias circuit controlled by the input control voltage V_{ctrl} are mirrored to each inverter delay cell that can be recognized as a current-starved inverter. In the inverter delay cell, transistors M_4 and M_5 perform the function of an inverter whereas M_3 and M_6 operate as current sources that confine the current flow into M_4 and M_5, hence the inverter comprising M_4 and M_5 is starved for current.

When D_{in} operating at the node A falls from V_{DD} to GND, the load capacitance of node B is charged to V_{DD} through the current source M_3. When D_{in} rises from GND to V_{DD}, the load capacitance of node B will be discharged to GND by the current source M_6. The delay

time of each inverter delay cell is determined by the time of the current charging and discharging the load capacitance. Thus, tuning V_{ctrl} directly controls the bias current, thereby further providing a means to control the delay time.

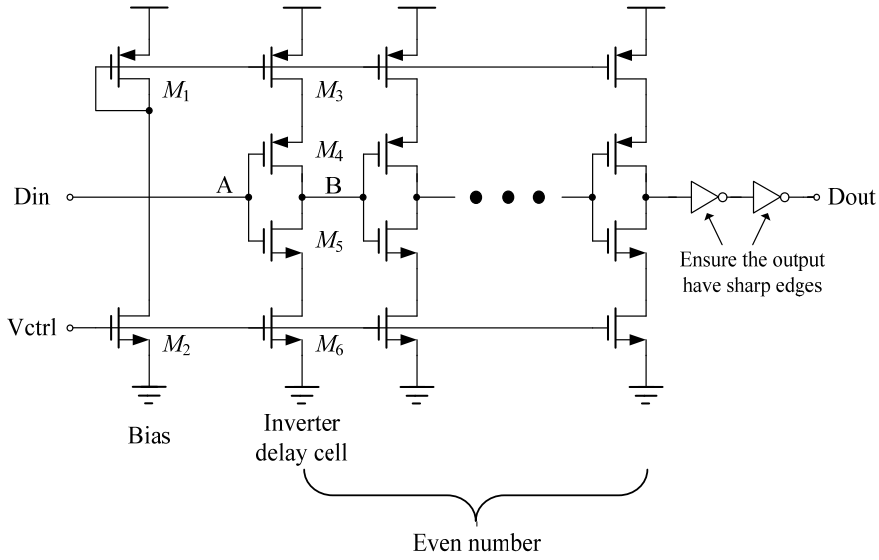

Fig. 8.10. Schematic of the delay line.

In practice, noise from CMOS devices themselves, power supply, substrate, and other circuits (cross-talk) will cause the timing to jitter which can significantly impair the quality of clock signal and the operation of circuits may be compromised if the timing is larger than a certain required threshold. The delay lines are critical blocks in the CG and their delay accuracies directly affect the performance of the transmitter. Here the eye-diagram analysis is employed to estimate the peak-to-peak jitter of the delay line output. As presented in Fig. 8.11, when D_{in} is applied to the 50 MHz clock signal, the simulated peak-to-peak jitter of the output is approximate 48 fs, which can be neglected comparing with the delay times of 1.5 ns and 2.5 ns. Therefore, the delay line can be regarded as no jitter accumulation and can be used to provide a high-quality delayed clock signal. The 1.5-ns and 2.5-ns delay lines can be precisely achieved by 3 means: adjusting the control voltage V_{ctrl}, the number of inverter delay cells as well as sizes of transistors for each delay cell. Fig. 8.12 depicts the relevant simulation results. The 1.5-ns and 2.5-ns delays are performed at 0.9 V and 0.75 V of V_{ctrl}, respectively. Fig. 8.13 shows the delay-time adjusting range of the delay line. The inverter delay cells are even numbered to enable an in-phase signal shift in the design and last two inverters are employed to sharpen the waveform edges of the output.

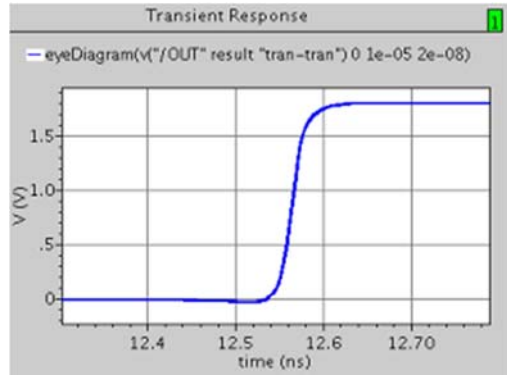

Fig. 8.11. The simulated peak-to-peak jitter of the delay line output.

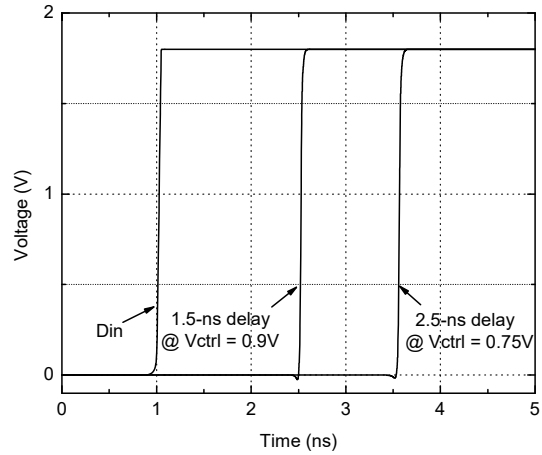

Fig. 8.12. Simulated results of 1.5-ns and 2.5-ns delay lines.

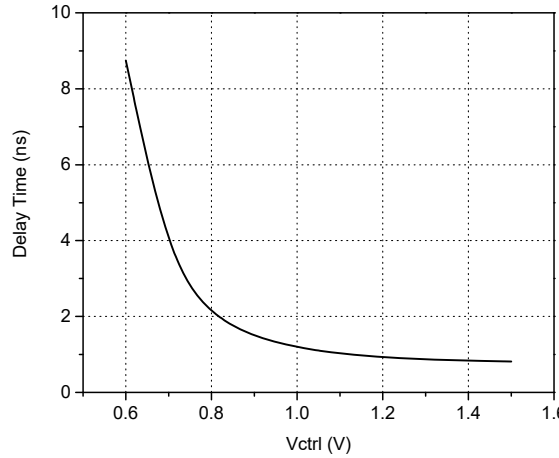

Fig. 8.13. Simulated delay-time adjusting range.

8.2.3.2. 8-to-1 Multiplexer and PPM Delay Cell

The 8-to-1 multiplexer employed in the design consists of two 2-to-4 decoders, two 4-to-1 multiplexers, and one 2-to-1 multiplexer as indicated in Fig. 8.14. Each block is a conventional circuit. The 2-to-4 decoder is a logic circuit that is basically implemented by four AND gates and two inverters. The 4-to-1 multiplexer is realized by four AND gates and three OR gates, whilst the 2-to-1 multiplexer is the simplest multiplexer constructed by one inverter, two AND gates, and one OR gate.

The PPM delay cell utilizes two inverters to yield the delay time δ for position modulation. Here, δ is set to be 150 ps, which is sufficient to distinguish the Tx data 0 and 1.

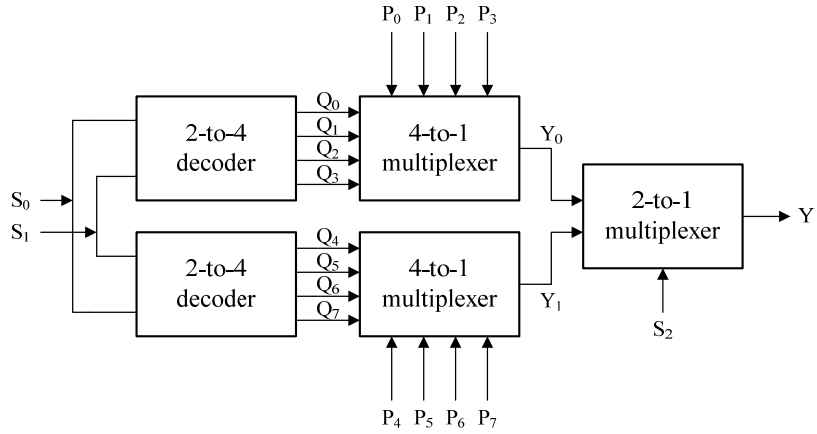

Fig. 8.14. Block diagram of the 8-1 multiplexer.

8.2.3.3. Pseudorandom Number Sequence Generator

The output of the 8-to-1 multiplexer is selected according to a sequence of pseudorandom binary numbers generated by a 4-bit PNSG, which is a special shift register with linear feedback built by four rising edge-triggered D-flip flop and one XOR as feedback.

The sequence of pseudorandom binary numbers produced by the 4-bit PNSG appears random but it is deterministic in nature so as to repeat at a period of $(2^4 - 1) = 15$. Fig. 8.15 displays the simulated results of the PNSG. As mentioned in Section 8.2.3.2, S_0-S_2 is used as pseudorandom time-hopping code $c_j^{(k)}$ for assigning a distinct pulse-shift to the k^{th} user of 8. $c_j^{(k)}$ is the decimal number corresponding to the binary output of S_0-S_2. Based on the simulation results, the relationships between S_0-S_2 and $c_j^{(k)}$ are presented in Table 8.4. Note that each code element is an integer in the range of $0 \leq c_j^{(k)} < 8$ for $N_h = 8$ and the sequence repeats at the 15th time frame, that is to say, the period N_p of the pseudorandom time-hopping $c_j^{(k)}$ is 15. Hence, the sequence repeats at the period of 15×20 ns = 300 ns.

Subsequently, three time-hopping bits S_0-S_2 will select the 8-1 multiplexer inputs and pass them on to the output.

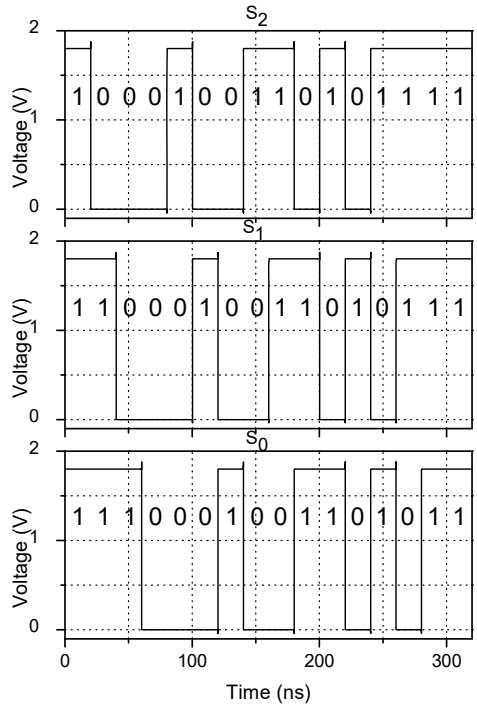

Fig. 8.15. Simulated results of the PNSG.

Table 8.4. The Relationship between S_0-S_2 and $c_j^{(k)}$.

	S_2	S_1	S_0	$c_j^{(k)}$
1st	1	1	1	7
2nd	0	1	1	3
3rd	0	0	1	1
4th	0	0	0	0
5th	1	0	0	4
6th	0	1	0	2
7th	0	0	1	1
8th	1	0	0	4
9th	1	1	0	6
10th	0	1	1	3
11th	1	0	1	5
12th	0	1	0	2
13th	1	0	1	5
14th	1	1	0	6
15th	1	1	1	7

8.2.3.4. Pulse Generator

The pulse train from the 2-to-1 multiplexer is input to the PG to generate the differential 5th-derivative Gaussian pulses. The schematic of the differential PG is shown in Fig. 8.16, which is inspired and derived from the single-ended PG given in Fig. 8.1. Although the single-ended PG that generates the positive 5th-derivative Gaussian pulse was verified in a 0.18-μm CMOS, how to produce the negative 5th-derivative Gaussian pulse and particularly how to cancel the phase difference between them are challenging. To produce the negative 5th-derivative Gaussian pulse, based on the positive pulse generator in Fig. 8.1 and interchanging the corresponding locations of NANDs and NORs, the negative fifth-derivative Gaussian pulse generator is also developed in Fig. 8.16, which is similarly implemented with a triangular pulse generating stage, an output stage, and a 50 Ω load. Note that in order to generate the negative fifth-derivative Gaussian pulse, an integrant inverter *Inv* is added in Fig. 8.16. At the terminals of the triangular pulse generating stage, the positive-peak triangular pulses from GND to V_{DD} are generated on the nodes A– and C– whilst the negative-peak triangular pulses from V_{DD} to GND are formed on the nodes B– and D–. The peak to peak amplitude of each triangular pulse is kept to be the same and the delay time of each triangular pulse is regulated to yield the sequential phase by adjusting the sizes and numbers of inverters. When operating on the gates of transistors M_5–M_8 building the output stage, the four triangular pulses are inverted by the output stage and integrated into the negative fifth-derivative Gaussian pulse smoothly on node E–. Transistors M_5 and M_8 produce small peaks of the negative Gaussian pulse whereas transistors M_6 and M_7 yield large peaks. The amplitudes of small and large peaks can be designated by tuning the sizes of transistors M_5–M_8. The output stage hardly causes static power consumption since only one MOS transistor is switched on during operation.

The simulated differential fifth-derivative Gaussian pulse is shown in Fig. 8.17, where the positive and negative Gaussian pulses are generated, respectively. It is obviously observed that compared with that of the positive one (solid line), the phase of the negative pulse (dash line) is delayed for 130 ps, which is undoubtedly owing to the joined *Inv* in Fig. 8.16. Hence, the key to precisely generate the differential output is the phase delay between the positive and negative Gaussian pulse. In order to offset the phase delay, a transmission gate (TG) is inserted in front of the positive pulse generation circuit. Combining the positive pulse generator with the negative one, the whole differential pulse generator is constructed in Fig. 8.16 to produce the differential fifth-derivative Gaussian pulse accurately. The simulations shown in Fig. 8.18 exhibits that there is almost no phase delay between the positive and negative pulses since the TG effectively compensate the phase delay caused by the *Inv.* The generated differential fifth-derivative Gaussian pulse can directly drive the dipole antenna.

Post-layout simulations of the TH-PPM pulse train and the corresponding 5th-derivative Gaussian pulse are shown in Fig. 8.1 9, respectively. The TH-PPM pulse train shows the random property. The digital pulse width is 1.4 ns. The differential output of the pulse generator is the 5th-derivative Gaussian pulse that has amplitude of 650 mV peak to peak and a pulse width of 750 ps. The performance of the differential 5th-derivative Gaussian pulse is mainly determined by the delay time of four triangular pulses as mentioned

previously, and therefore is affected by process, voltage, and temperature (PVT) variation. The impact of PVT variation on the manufacturability of the pulse generator was also investigated by post-layout simulations. Table 8.5 shows the simulated performance of the differential 5th-derivative Gaussian pulse vs. PVT variation. In Table 8.5, besides the above performance of the pulse simulated at the typical case with the corner of TT mode (normal threshold voltage of pMOS and nMOS), the supply voltage of 1.8 V, and the temperature of 27 ºC, the pulse achieves amplitude of 732 mV peak to peak with a pulse width of 428 ps at the best case with the corner of FF mode (low threshold voltage of pMOS and nMOS), the supply voltage of 2 V, and the temperature of –40 ºC; the pulse has a peak-to-peak amplitude of 453 mV and a pulse width of 873 ps at the worst case with the corner of SS mode (high threshold voltage of pMOS and nMOS), the supply voltage of 1.6 V, and the temperature of 110 ºC. In both case, the generated pulses also achieve precise shapes, which are sufficient for receiver to decode the data information. Therefore, the yielded differential 5th-derivative Gaussian pulse is robust to sustain PVT variation.

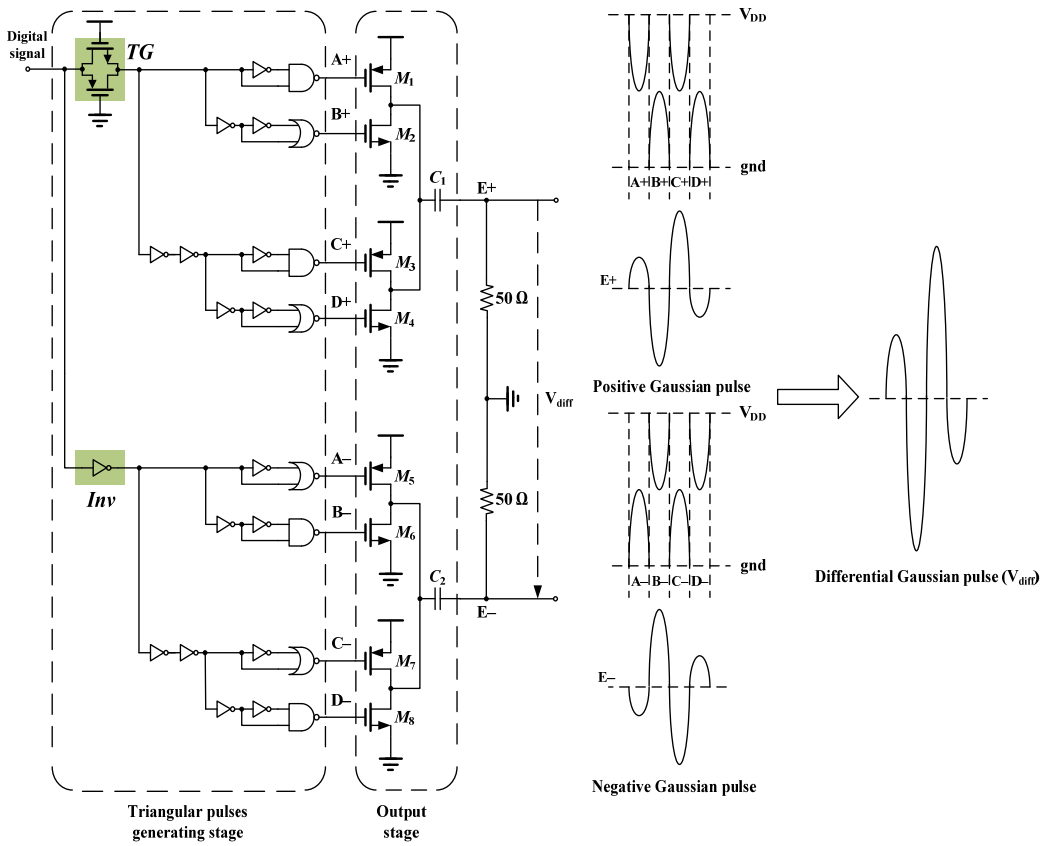

Fig. 8.16. Schematic of the differential PG.

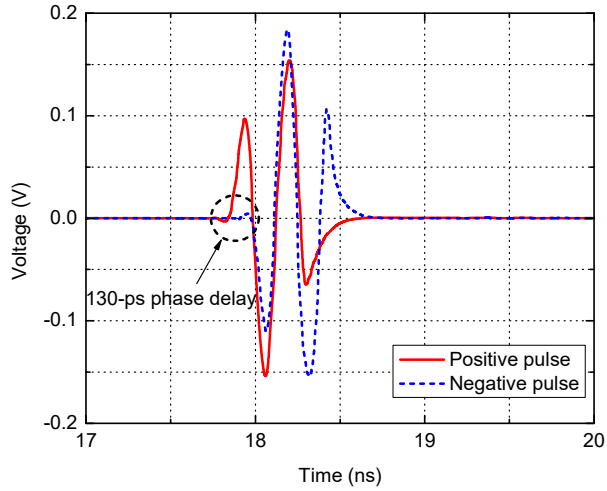

Fig. 8.17. The simulated differential fifth-derivative Gaussian pulse with 130 ps phase delay.

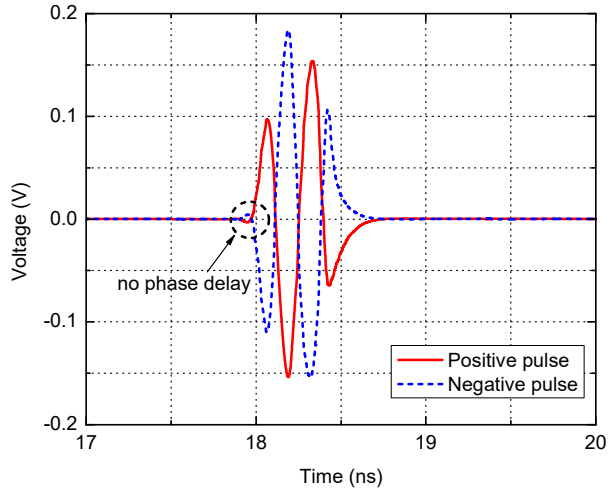

Fig. 8.18. The simulated differential fifth-derivative Gaussian pulse with the offsetting TG.

8.2.4. Measurement Results and Discussions

The fully-integrated differential impulse radio transmitter was fabricated using a 1.8 V 0.18-μm CMOS process. The die microphotograph of the IC is depicted in Fig. 8.20. The entire IC area is small, only 629 μm × 797 μm, largely because of its all-digital design.

As the available testing facilities are limited, only the positive 5^{th}-derivative Gaussian pulse was measured. A Tektronix DG2020A data generator was utilized to provide digital Tx data input with data rate of 50 Mbps. A Lecroy 8600A oscilloscope was employed to measure the output. The measurements were carried out at the load impedance of 50 Ω including the parasitic effects of the signal pads, probe, coaxial cable, and SMA connector.

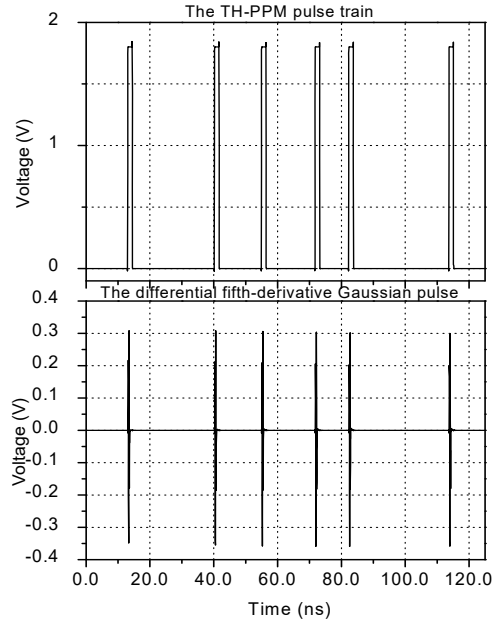

Fig. 8.19. Post-layout simulations of TH-PPM pulse train and the corresponding 5th-derivative Gaussian pulse.

Table 8.5. The Simulated Performance of the Differential Output versus PVT.

P	V (V)	T (ºC)	The differential 5th-derivative Gaussian pulse	
			Amplitude Vpp (mV)	Pulse width (ps)
FF	2	– 40	732	428
TT	1.8	27	650	750
SS	1.6	110	453	873

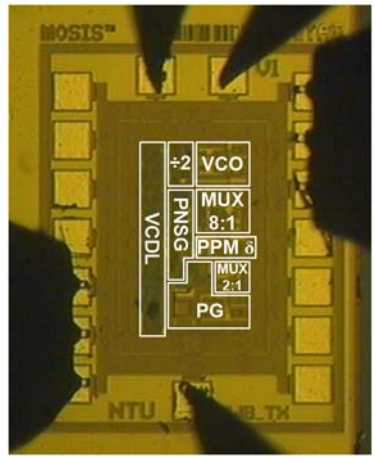

Fig. 8.20. Die microphotograph of the fully-integrated impulse radio transmitter.

Fig. 8.21 presents the measured positive 5th-derivative Gaussian pulses at the output of the transmitter, which shows the random property. The shape of the measured 5th-derivative pulse in Fig. 8.22 is well matched with that of the simulated 5th-derivative pulse in Fig. 8.23. The measured pulse has a peak-to-peak amplitude of 154 mV and a pulse width of 820 ps. The simulated pulse has a peak-to-peak amplitude of 300 mV and a pulse width of 750 ps. The discrepancy between the simulated and measured pulses is attributed to the following reasons. First, note that there is a 3-dB difference in the amplitudes. Second, the loss from the probe, coaxial cable, and SMA connector accounts for 1.5 dB. Third, the other 1.5-dB loss may be due to the parasitic effect of wire interconnects and signal pads. They will not only reduce the pulse amplitude but also cause delay and distortion to the pulse. Hence, interconnects for the pulse generator must be designed as short as possible to minimize the parasitic effect. The parasitic capacitance of the signal pads must be minimized.

The power spectral density (PSD) of the measured pulse complies with the FCC spectrum mask. The average power dissipation is 23 mW at the supply voltage of 1.8 V. The measured performance of the proposed transmitter is summarized and compared with reported key transmitters in Table 8.6.

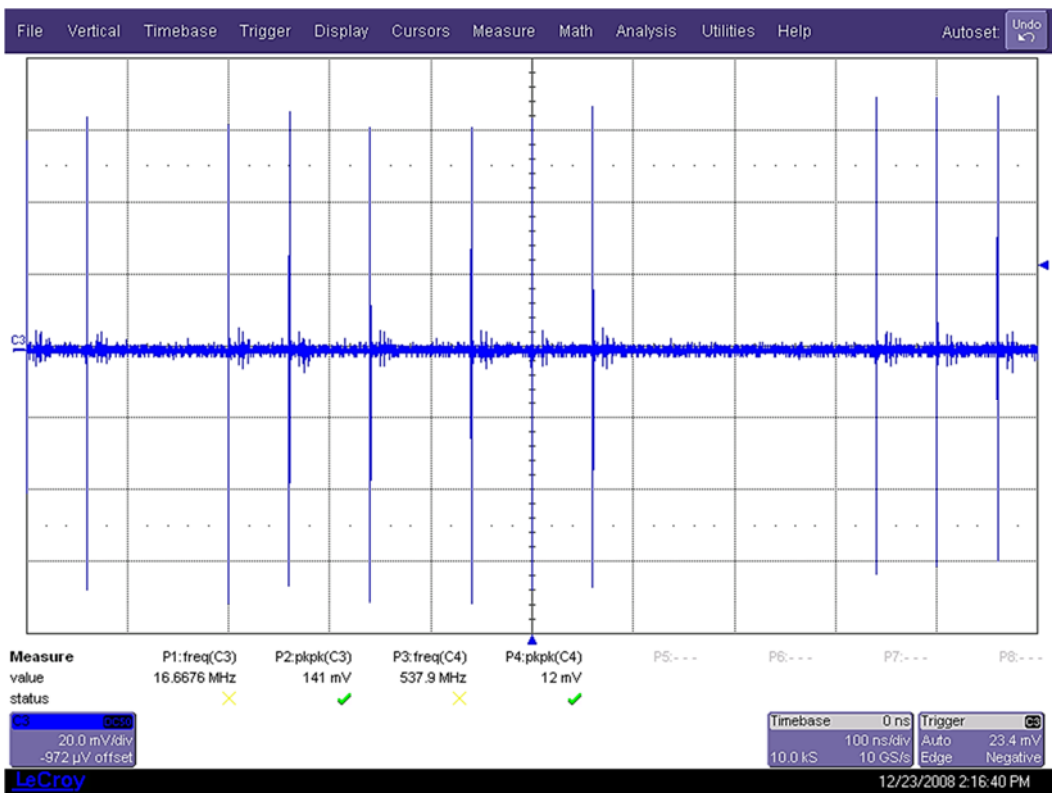

Fig. 8.21. The measured TH-PPM 5th-derivative Gaussian pulse train.

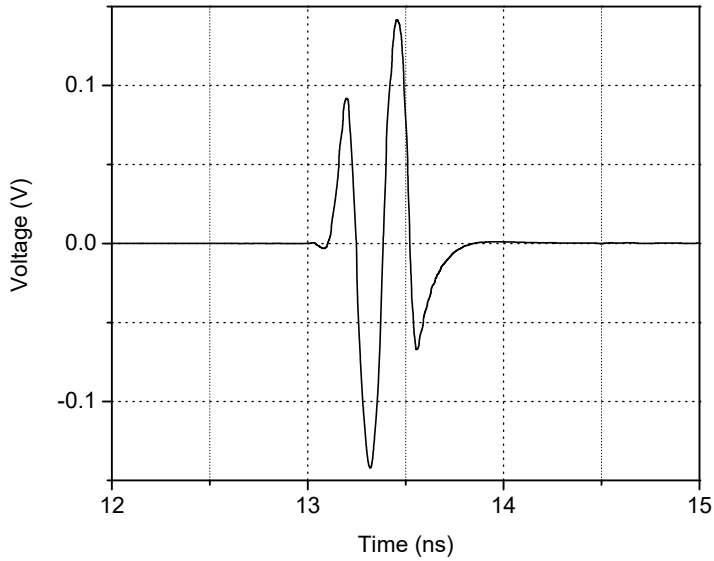

Fig. 8.22. The simulated positive 5th-derivative Gaussian pulse.

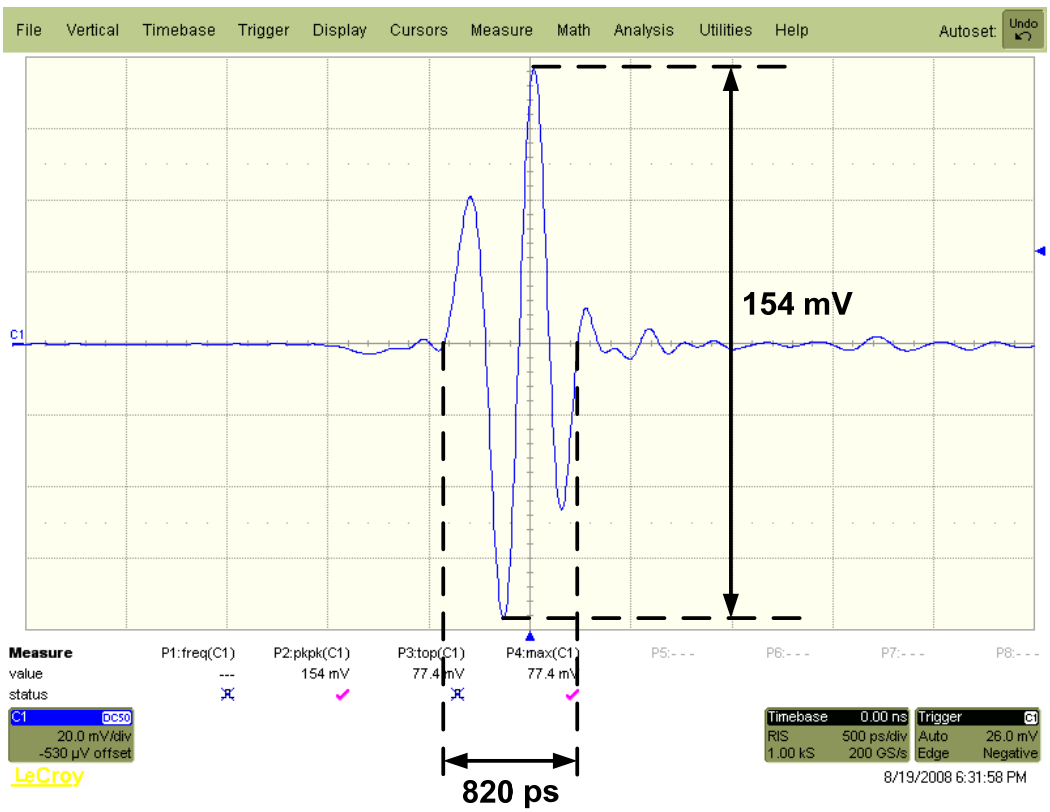

Fig. 8.23. The measured positive 5th-derivative Gaussian pulse.

Table 8.6. Measured Performance Summary and Comparison with Reported Transmitters.

References	[18]	[20]	This work
UWB Transmitter	Impulse radio	Impulse radio	Time hopping differential impulse radio
Modulation	OOK	DBPSK	PPM
Tx data rate (Mbps)	100	72 (36 MHz)	50
Transmitted pulse width (ns)	≈ 2*	1.75	**0.82**
Maximum amplitude Vpp (mV)	650*	640	**154**
Average power dissipation (mW)	N.A.	29.7	**23**
Supply voltage (V)	3.3	2.2	**1.8**
Technology	0.35-μm CMOS	0.18-μm CMOS	**0.18-μm CMOS**
Die size (mm^2)	1560#	0.40	**0.50**

* Measured values of bandpass filter (BPF) and # the whole size of system-on-package (SOP) in the reference [18].

8.2.5. Conclusion

A fully integrated differential impulse radio transmitter has been designed for UWB applications using the TH-PPM modulation scheme. Eight hopping positions which allow 8 users' simultaneous access with hopping time 2.5 ns are allocated in a frame time of 20 ns. The proposed differential impulse radio transmitter has been fabricated with a 1.8-V 0.18-µm CMOS technology. The IC area is small, only 0.5 mm^2. And the measured average power dissipation is low, ~23 mW - for its all-digital design. The transmitter complies with the FCC spectrum mask without the need for a filter because of the measured precise 5th-derivative Gaussian pulse shape. As a prototype, it transmits the data at a rate of 50 Mbps, which is sufficient for low-power sensor area network applications.

8.3. CMOS UWB Switches for Impulse Radio Transceiver

8.3.1. Introduction

A simple UWB-IR transceiver front-end block diagram is presented in Fig. 8.24. The UWB signals are switched to the receiver (Rx) after received by an antenna. Contrarily in the transmission path, the UWB signals are generated and amplified by an all-digital transmitter (Tx) in Section 8.2 and then switched to the antenna for transmission. A transmit/receive (T/R) switch is employed here to turn on/off the transmission and reception path to the antenna. Hence, the T/R switch is an important function block in an RF transceiver front-end. In particular, a T/R switch can be found in any time-division duplexing (TDD)-based radio front-end [37]. A TDD radio system can inherently offer a lot of advantages and flexibilities that a frequency-division duplexing (FDD) radio system cannot. These advantages include channel reciprocity, dynamic bandwidth allocation, and higher frequency diversity.

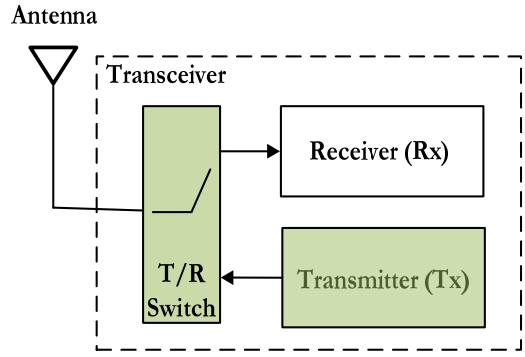

Fig. 8.24. The architecture of UWB-IR transceiver.

A T/R switch is required with low insertion loss, high isolation, large power-handling capability, and fast switching speed. Owing to the intrinsic drawbacks of standard CMOS process in RF perspectives, viz., a low quality factor, lossy substrate of passive elements, and low breakdown voltage of active devices, the design of a T/R switch in CMOS with satisfactory performance is a challenging task. Nevertheless, there have been many attempts to design T/R switches in CMOS over the last decade [22, 29-46]. A few novel design techniques such as minimizing or maximizing substrate resistance [29], stacking transistors [31], floating bodies [32, 33], and stacking transistors together with floating bodies [46] have been devised for CMOS T/R switches. Among them, the body-floating techniques that increase significantly power-handling capability of CMOS T/R switches have attracted our attention [22, 35]. Fig. 8.25 shows different schemes of the body-floating techniques. A parallel *LC* resonance network that directly floats the substrate of the nMOS transistor is illustrated in Fig. 8.25 (a). The large power-handling capability of 28 dBm is achieved for the T/R switch at 5.2 GHz with this *LC*-tuned body-floating technique [32]. In modern CMOS process, a deep n-well separates the body (p-well) of the nMOS transistor from the substrate to provide better performance of noise, isolation, bulk control, etc. Therefore, the body can be floated with a large resistance without causing latch up. The resistive body-floating technique in a triple-well CMOS is shown in Fig. 8.25 (b). The power-handling capability of 21 dBm is obtained by floating the p-wells with resistors of the same large resistance [33].

A scrutiny of the body-floating techniques reveals that the performances of CMOS T/R switches with the *LC*-tuned and resistive body-floating techniques have been investigated with different topologies and in different CMOS processes. In other words, the two body-floating techniques have not been properly evaluated. In this section, we try to fill this void. We propose an asymmetric topology and more importantly we present a comparative study of the T/R switches with the two techniques under the same conditions. Section 8.3.2 describes the CMOS T/R switch topologies. Section 8.3.3 evaluates the simulated and measured performances of the T/R switches that feature respectively the *LC*-tuned and resistive body-floating techniques. Finally, the paper is concluded in Section 8.3.4.

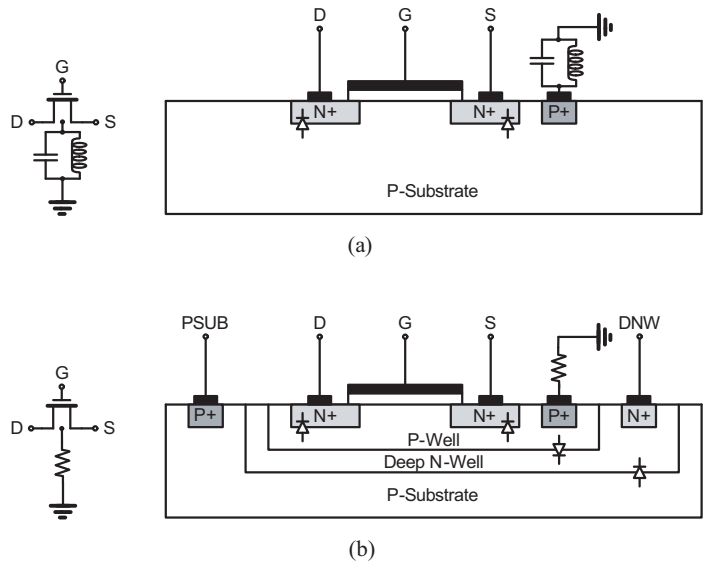

Fig. 8.25. Different schemes of the body-floating techniques: (a) The LC-tuned body-floating, and (b) The resistive body-floating.

8.3.2. Asymmetric Topology for CMOS T/R Switch

The conventional symmetric T/R switch topology is shown in Fig. 8.26 (a). The series transistors, M_1 and M_2, carry out the transmit/receive function of signals whereas the shunt transistors, M_3 and M_4, ground RF signals to enhance the isolation between the transmit (Tx) path and the receive (Rx) path. The gates of all transistors are floated by large resistances R_{G1}, R_{G2}, R_{G3}, and R_{G4} to enhance the dc-bias isolation. The bodies of all transistors are floated by high impedances Z_{B1}, Z_{B2}, Z_{B3}, and Z_{B4} to achieve low insertion loss and large power-handling capability. An on-chip inductor L_{ESD} is used for ESD protection [37].

The new asymmetric T/R switch topology is shown in Fig. 8.26 (b). It is seen that the asymmetric topology is derived from the conventional symmetric topology by omitting high impedances Z_{B2}, Z_{B3}, and Z_{B4}, which can be explained from the Tx and Rx modes. In the Tx mode, M_1 and M_4 are switched ON, while M_2 and M_3 are switched OFF. The bodies of the OFF transistors M_2 and M_3 should be RF grounded to reduce the capacitive drain-source feed-though. In the Rx mode, M_2 is turned ON to receive RF signal. The received RF signal is very weak and normally has amplitude of far less than 0.7 V, which will not turn on the parasitic junction diodes. Therefore, the body-floating techniques should not be used for M_2. Also in the Rx mode, M_3 is turned ON to ground unwanted RF signals. The body of M_3 should be directly grounded for isolation improvement. However, the omission of high impedances Z_{B2}, Z_{B3}, and Z_{B4} will cause a problem. As can be seen from Fig. 8.26, each ON transistor is connected with two OFF transistors when the T/R switch is operating. For example, in the Tx mode M_2 and M_3 are OFF whereas M_1 is ON. In this mode, supposing that OFF transistors M_2 and M_3 are body-grounded, the parasitic

to the body will not only couple extra signal to the ground to cause the insertion-loss degradation but also clip the RF signal to reduce the power-handling capability. To minimize this problem, one solution relies on the proper layout to keep the parasitic at the common nodes of Tx, ANT, and Rx as small as possible to prevent extra loss for the ON transistor. Another solution applies dc-bias on the common nodes to improve the insertion loss and power-handling capability.

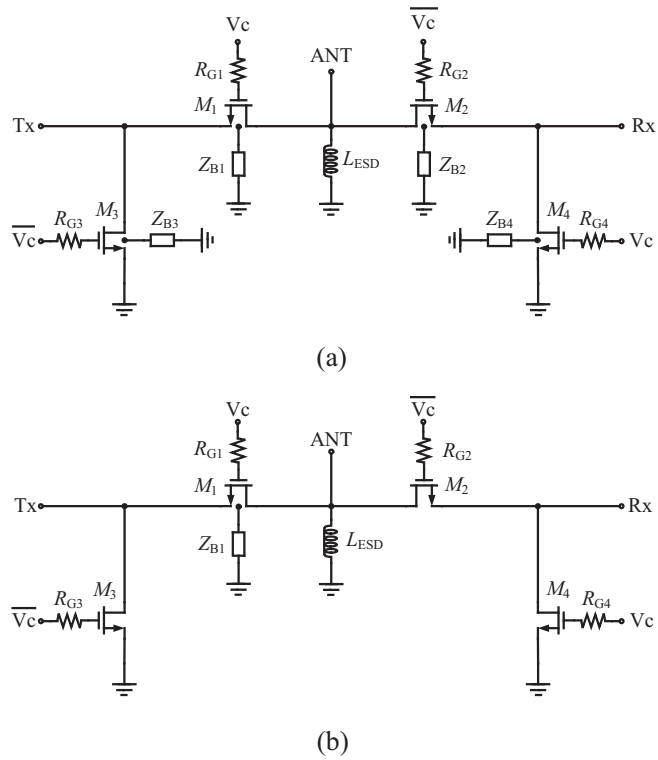

Fig. 8.26. (a) The conventional symmetric T/R switch topology (b) the new asymmetric T/R switch topology.

The simplified small-signal equivalent circuit of the asymmetric T/R switch in the Tx mode is shown in Fig. 8.27 (a). As the total impedance of parasitic capacitances is considerably larger than the on-resistance R_{on}, the ON transistor M_1 is only represented with $R_{on\ (M1)}$. The OFF transistors M_2 and M_3 are respectively represented with capacitances $C_{off\,(M2)}$ and $C_{off\,(M3)}$, where $C_{off\,(M2)}$ is connected to ground since the Rx node is pulled to ground when the transistor M_4 is turned ON. It is found from simulations that the simplified small-signal equivalent circuit can be further approximated to the circuit of Fig. 8.27 (b). Likewise, the simplified small-signal equivalent circuit of the asymmetric T/R switch in the Rx mode and its further approximation are presented in Fig. 8.27 (c) and (d), respectively.

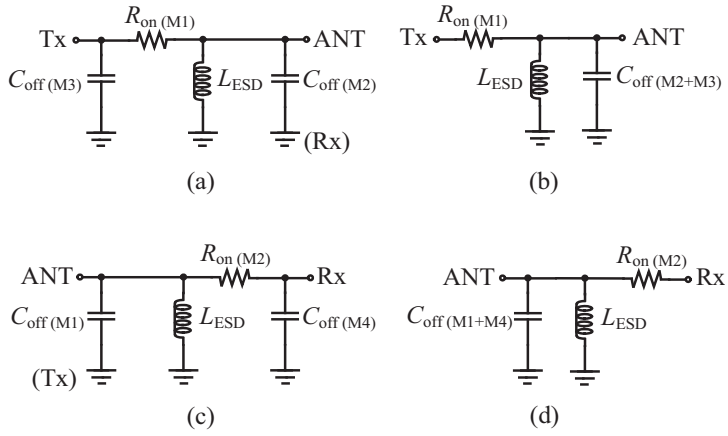

Fig. 8.27. The simplified small-signal equivalent circuit of the asymmetric T/R switch (a) In the Tx mode, and (b) Its approximate equivalent circuit; (c) In the Rx mode, and (d) Its further approximation.

Note that the simplified small-signal equivalent circuit and its corresponding approximation in the Tx mode exhibits the mirror feature with respect to those in the Rx mode. Therefore, the T/R switch can be characterized through analyzing the equivalent circuit either in the Tx mode or in the Rx mode. It is evident from Fig. 8.27 (b) that L_{ESD} and $C_{off\,(M2+M3)}$ form a parallel resonator, i.e., L_{ESD} can effectively tune out the parasitic capacitances so as to reduce the insertion loss as well as to enhance the power-handling capability. Also, in the integration of the T/R switch with other RF building blocks, $C_{off\,(M2+M3)}$ and L_{ESD} can also serve as parts of the matching network. Furthermore, the transistor's width should be increased to obtain smaller on-resistance to reduce the insertion loss and to enhance the power-handling capability. However, if the transistor's width is increased excessively, the increased parasitic capacitances significantly couple the RF signal to ground to incur extra insertion loss. Choosing smaller L_{ESD} can effectively cancel larger $C_{off\,(M2+M3)}$ to obtain wider transistor's width, however, this will degrade the ESD protection effectiveness. Hence, $R_{on(M1)}$, L_{ESD}, and $C_{off(M2+M3)}$ should be properly traded off to achieve better T/R switch performance. In order to achieve an insertion loss below 1 dB in both Tx and Rx modes at 5.2 GHz, here one set of critical model element parameters is tabulated in Table 8.7, which can be regarded as a reference for the concrete circuit design of the proposed T/R switch.

Table 8.7. Model Element Parameters.

Model Element	Element Parameters @ 5.2 GHz
$R_{on(M1)}$, $R_{on(M2)}$	12 Ω
$C_{off\,(M2+M3)}$, $C_{off\,(M1+M4)}$	310 fF
L_{ESD}	3 nH

8.3.3. Evaluation of the Body-floating Techniques

8.3.3.1. The LC-tuned Body-floating Technique

Substituting high impedances Z_{B1}–Z_{B4} in Fig. 8.26 (a) and Z_{B1} in Fig. 8.26 (b) with the corresponding *LC*-tuned networks, we get the conventional symmetric and new asymmetric T/R switches that feature the *LC*-tuned body-floating technique. As shown in Fig. 8.28 (a), the symmetric T/R switch that uses five on-chip inductors is impractical, while the asymmetric T/R switch shown in Fig. 8.28 (b) that uses only two on-chip inductors is more practical for silicon implementation. Both symmetric and asymmetric T/R switches were simulated and only the asymmetric one was fabricated using a standard 0.18-μm CMOS triple-well process. Table 8.8 lists the active device dimensions and passive element values for 5.2-GHz application. Note that a 3 nH inductance is chosen for the shunt inductor L_{ESD}, which has been verified to pass HBM ESD test of +/- 3 kV between RF pin and ground pin without obvious DC function decay.

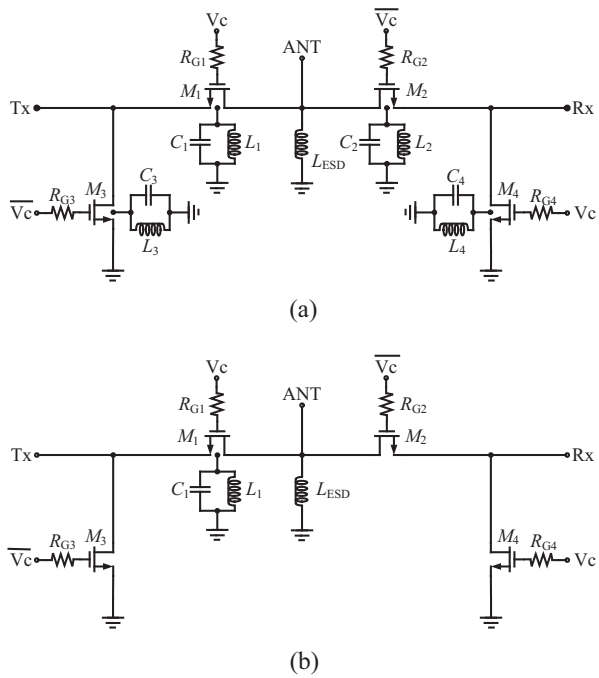

Fig. 8.28. CMOS T/R switches using the *LC*-tuned body-floating technique: (a) The conventional symmetric T/R switch, and (b) The new asymmetric T/R switch.

The die microphotograph of the asymmetric T/R switch is shown in Fig. 8.29. The whole chip area including the test pads is 1.39 mm × 1.28 mm. On-wafer measurement was performed with 100 μm GSG probes. The unused port was terminated by a 50 Ω load during measurement. The pad effect was de-embedded afterwards.

Table 8.8. Circuit Element Values.

Circuit Element	Element Value @ 5.2 GHz
M_1, M_2	180 μm/0.18 μm
M_3, M_4	80 μm/0.18 μm
R_{G1}, R_{G2}, R_{G3}, R_{G4}	10 kΩ
R_{B1}, R_{B2}, R_{B3}, R_{B4}	10 kΩ
L_1, L_2, L_3, L_4	3.6 nH
C_1, C_2, C_3, C_4	150 fF
L_{ESD}	3 nH
V_{bias} for Tx and Rx nodes	1.8 V
Vc	3.6 V (on), 0 V (off)
$\overline{Vc}$	0 V (on), 3.6 V (off)

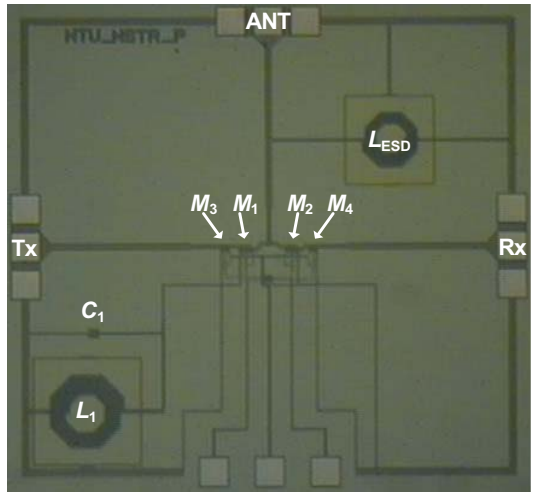

Fig. 8.29. Die microphotograph of the asymmetric T/R switch shown in Fig. 8.28(b).

Post-layout simulated insertion loss, isolation, and reflection coefficients for the symmetric (Fig. 8.28 (a)) and asymmetric (Fig. 8.28 (b)) T/R switches are plotted in Fig. 8.30. The results show that they have almost the same performance. For example, at the operating frequency of 5.2 GHz, they have 1.8 dB insertion loss, 24.7-dB isolation, and excellent matching to the 50 Ω source and load. The measured insertion loss, isolation and reflection coefficients for the asymmetric T/R switch (Fig. 8.28(b)) are also shown in Fig. 8.30. It exhibits 1.5 dB insertion loss, 23.5 dB isolation, and good matching to the 50 Ω source and load at 5.2 GHz. The simulated and measured results are in good agreement.

The power-handling capability is measured by the input 1-dB compression point (P_{1dB}) which can be expressed in dBm by

$$P_{1\text{dB}} = 10\log\left(\frac{2V_{th}^2}{Z_0}\right) + 30 \tag{8.8}$$

V_{th} is denoted as the threshold voltage of the shunt nMOS transistor M_3. The simulated power-handling capabilities for the symmetric and asymmetric T/R switches are plotted in Fig. 8.31. The results show that they have the same power-handling capability with the input P_{1dB} of 23 dBm. Hence, the body-grounding that replaces the body-floating for transistors M_2–M_4 by removing LC-tuned networks L_2-C_2, L_3-C_3, and L_4-C_4 will not impair the power-handling capability of the T/R switch. The measured power-handling capability of the asymmetric T/R switch is also shown in Fig. 8.31. The measured input P_{1dB} is 22.5 dBm, which is only 0.5 dB lower than the simulated one.

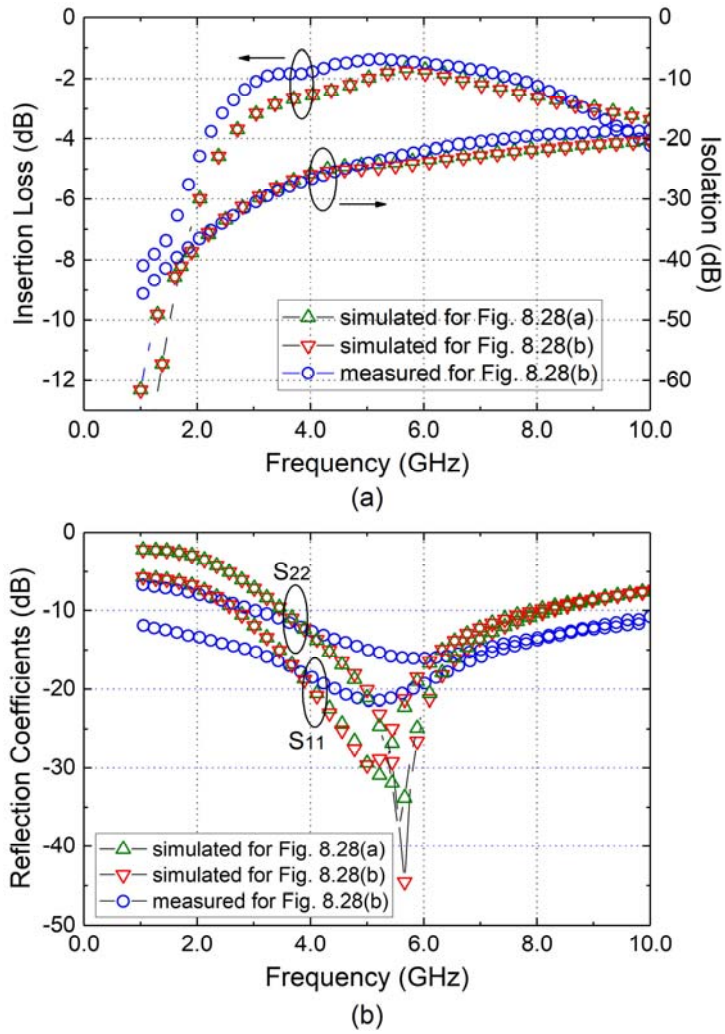

Fig. 8.30. Simulated and measured insertion loss, isolation, and reflection coefficients for the T/R switches shown in Fig. 8.28.

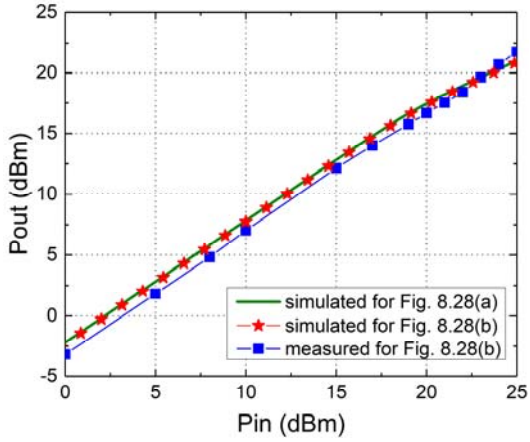

Fig. 8.31. Simulated and measured input P_{1dB} for the T/R switches shown in Fig. 8.28.

8.3.3.2. The Resistive Body-floating Technique

Substituting high impedances Z_{B1}–Z_{B4} in Fig. 8.26 (a) and Z_{B1} in Fig. 8.26 (b) with the corresponding resistances, we get the conventional symmetric (Fig. 8.32 (a)) and new asymmetric (Fig. 8.32 (b)) T/R switches that feature the resistive body-floating technique. Both symmetric and asymmetric T/R switches were simulated and only the asymmetric one was fabricated using the same 0.18-μm CMOS triple-well process. Fig. 8.33 shows the die microphotograph of the asymmetric T/R switch using the resistive body-floating technique. It occupies the same area as that using the *LC*-tuned body-floating technique. Actually, the T/R switch adopting the resistive body-floating technique consumes much less silicon area than that employing the *LC*-tuned body-floating technique. Here, the area is kept the same for comparison purpose.

Post-layout simulated insertion loss, isolation, and reflection coefficients for the symmetric (Fig. 8.32 (a)) and asymmetric (Fig. 8.32 (b)) T/R switches are plotted in Fig. 8.34. The results show that they have almost the same performance. For example, at the operating frequency of 5.2 GHz, they have 1.6 dB insertion loss, 24.6 dB isolation, and excellent matching to the 50 Ω source and load. The measured insertion loss, isolation and reflection coefficients for the asymmetric T/R switch (Fig. 8.32(b)) are also shown in Fig. 8.34. It exhibits 1.3-dB insertion loss, 24 dB isolation, and good matching to the 50 Ω source and load at 5.2 GHz. The simulated and measured results are in good agreement.

The simulated power-handling capabilities for the symmetric and asymmetric T/R switches are plotted in Fig. 8.35. The results show that they have the same power-handling capability with the input P_{1dB} of 22.8 dBm. Hence, the body-grounding that replaces the body-floating for transistors M_2–M_4 by removing resistances R_{B2}, R_{B3}, and R_{B4} will not impair the power-handling capability of the T/R switch. The measured power-handling capability of the asymmetric T/R switch is also shown in Fig. 8.35. The measured input P_{1dB} is 22.2 dBm, which is only 0.6 dB lower than the simulated one.

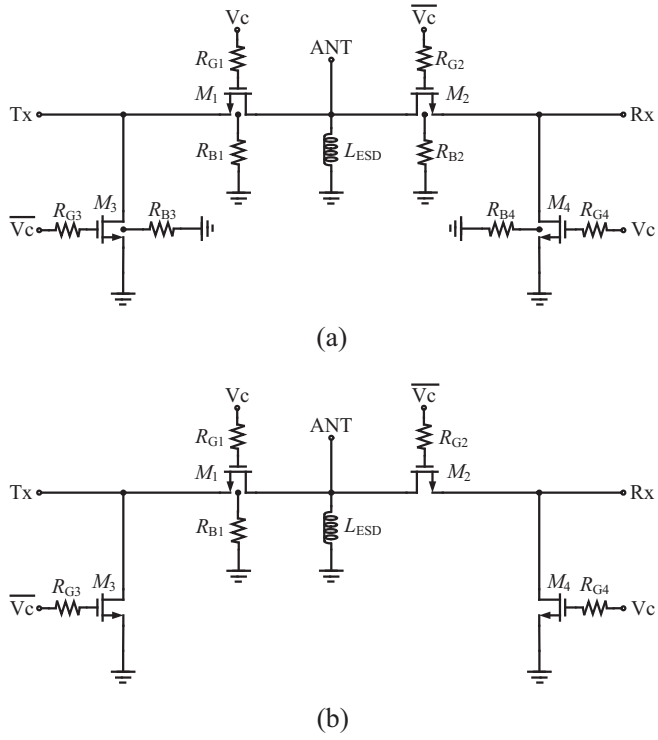

Fig. 8.32. CMOS T/R switches using the resistive body-floating technique: (a) The conventional symmetric T/R switch, and (b) The new asymmetric T/R switch.

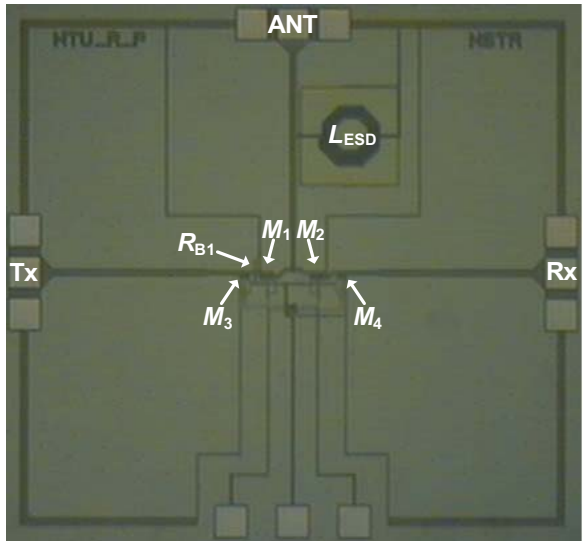

Fig. 8.33. Die microphotograph of the asymmetric T/R switch shown in Fig. 8.32 (b).

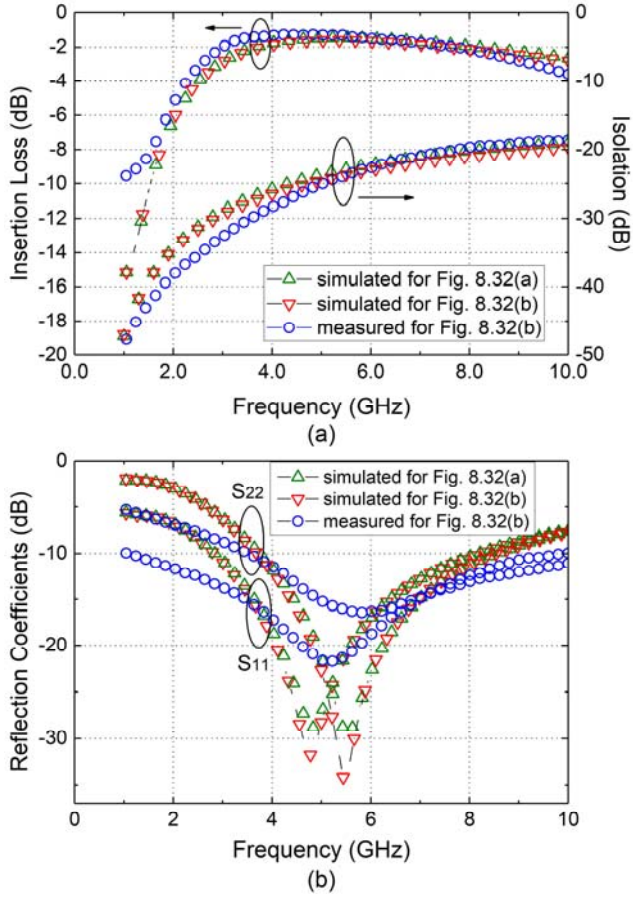

Fig. 8.34. Simulated and measured insertion loss, isolation, and reflection coefficients for the T/R switches shown in Fig. 8.32.

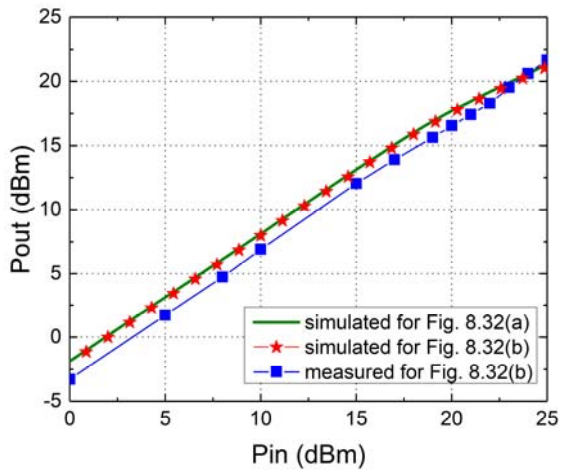

Fig. 8.35. Simulated and measured input P_{1dB} for T/R switches shown in Fig. 8.32.

8.3.3.3. Performance Comparison and Discussion

Table 8.9 lists the measured performance of our T/R switches. Note that under the same conditions, our T/R switches using either the *LC*-tuned or the resistive body-floating techniques achieve almost the same performance at the operating frequency of 5.2 GHz. However, if the shunt inductor L_{ESD} were not used the *LC*-tuned body-floating network would limit the operating bandwidth of the T/R switch owing to its narrowband nature and consumes large silicon area for the on-chip inductor whereas the resistive body-floating technique makes the T/R switch achieve wideband characteristics and consumes small silicon area.

Table 8.9. Summary of Performance and Comparison with Reported 5-6-GHz CMOS Switches.

Performance	This work		[32]	[33]
	***LC*-tuned**	**Resistive**		
CMOS	**0.18-μm**	**0.18-μm**	0.18-μm	0.18-μm
Frequency (GHz)	**5.2**	**5.2**	5.2	5.8
Return Loss: S_{11}/S_{22} (dB)	**21.4/15.3**	**21.6/15.7**	30/33 (Tx) 11/25 (Rx)	13.2/13.4
Insertion Loss (dB)	**1.5**	**1.3**	1.52 (Tx) 1.42 (Rx)	1.1
Isolation (dB)	**23.5**	**24**	30 (Tx) 15 (Rx)	27
P_{1dB} (dBm)	**22.5**	**22.2**	28 (Tx) 11.5 (Tx)	20
Control/Control/Bias (V)	**3.6/0/1.8**	**3.6/0/1.8**	1.8/0/-	1.8/-1.8/0

Table 8.9 also lists the measured performance of those T/R switches that originally employ the *LC*-tuned and the resistive body-floating techniques in the 5-GHz bands, respectively. Note that our T/R switch using the *LC*-tuned body-floating technique achieves the comparable insertion loss but poorer isolation and power-handling capability than the T/R switch that originally uses the *LC*-tuned body-floating technique. The different isolation and power-handling capability can be mainly attributed to the different topologies adopted in the two designs. Also note that our T/R switch using the resistive body-floating technique achieves slightly poorer insertion loss and isolation but better power-handling capability than the T/R switch that originally uses the resistive body-floating technique. The difference between the two designs is due to that the ESD is considered in our design.

8.3.4. Conclusion

Considering that the capacitive feed-through between the drain and source of the OFF transistor is a dominant limitation to the performance of high-frequency CMOS T/R switches, particularly at the state of body-floating, the asymmetric topology has been proposed. Furthermore, the enhancement of power-handling capability of the T/R

switches that feature the *LC*-tuned and resistive body-floating techniques has been evaluated for the first time based on the same asymmetric topology in the same standard 0.18-μm CMOS triple-well process. The simulated and measured results have shown that both techniques yield almost the same T/R switch performances at the operating frequency of 5.2 GHz. The T/R switch using the *LC*-tuned body floating exhibits measured 1.5 dB insertion loss, 23.5-dB isolation, and 22.5-dBm P_{1dB} whereas the T/R switch using the resistive body-floating techniques achieves measured 1.3 dB insertion loss, 24 dB isolation, and 22.2 dBm P_{1dB}, respectively. Therefore, we conclude that the asymmetric topology with the resistive body-floating technique is more suitable for designing UWB T/R switches for wireless local area network applications as it consumes smaller silicon area.

Acknowledgments

First and foremost, I would like to express my deepest gratitude to my supervisor, Professor Yue Ping Zhang, *IEEE Fellow*, Nanyang Technological University, Singapore, for his guidance, understanding, and patience throughout the research work. Without his persistent instruction and assistance, this work could not have been completed. His continuous encouragement along the way boosts my morale high to overcome difficulties in this work.

I would also like to thank my fellow student Shuo Li in EDA lab, Department of Microelectronics, Wuhan University. I am deeply thankful to him who had contributed towards this work with his invaluable advices, discussions, and revisions.

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Chapter 9

Printed Layers of ZnO-based Diluted Magnetic Semiconductors: Fabrication and Research

G. S. Pekar, A. F. Singaevsky, V. V. Strelchuk, O. F. Kolomys and P. M. Lytvyn

9.1. Introduction

So called diluted magnetic semiconductors (DMS) are solid solutions of the magnetic d-transition metals in diamagnetic semiconductors. In the transition metals (Mn, Ni, Co, Fe, etc.) the outer shell of the atoms is not completely filled with electrons which determines the magnetic moment of the atom. DMS are promising for use in spintronics in which, unlike conventional electronics, it is possible to use two degrees of freedom of an electron, connected with its charge and spin.

Over the past two decades, the study of DMS has become a hot topic, which is reflected in more than 2000 articles [1]. The initial impetus for such extensive research was the theoretical prediction of high-temperature ferromagnetism in wide-gap semiconductors ZnO and GaN which contain 5 at.% of Mn and have a high concentration of free carriers (about $4 \cdot 10^{20}$ cm^{-3} of holes) [2].

For a number of years this prediction was not confirmed experimentally, but recently a sufficient number of publications appeared that describe the ferromagnetic properties of DMS at temperatures above room temperature, up to 800 K [3]. It gives hope to achieve the main practical goal of these studies, namely, to create materials suitable for use in spintronics.

However, quite often the results on fabrication DMS with ferromagnetic properties are poorly reproducible and the nature of ferromagnetism, if any, remains uncertain. It means that sometimes difficult to pinpoint whether the observed ferromagnetism is an intrinsic or extrinsic phenomenon. In the latter case the ferromagnetism is due to clustering or to

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secondary phase formation and it is this mechanism that can be essential or even dominant. In the latter case, the use of such materials becomes impractical.

One of the main DMS materials supposed to be promising for spintronics purposes is zinc oxide doped with cobalt which is highly soluble in ZnO [4]. Note that ZnO:Co was indicated as a promising material still in the aforementioned prediction [2]. In 2009-2014 (and, most likely, also later) about a quarter of all publications on DMS were devoted just to ZnO:Co [5]. At the same time, DMS based on zinc oxide doped with manganese and iron are also considered promising for practical use [6, 7] and in recent years ZnO doping with Mn and Fe has been studied by many researchers. The last one is of particular interest. Firstly, the radii of both the two- and three-valent iron ions (Fe^{2+} and Fe^{3+}) are close to the radius of the Zn^{2+} ions which reduces the effect of the size of the introduced ions on the physical properties on ZnO host lattice and facilitates the interpretation of some phenomena due to doping. Secondly, doping with Fe ions makes it possible to study the possible appearance of impurity levels in the band gap of ZnO as well as some other changes in the energy band, which can be relatively dependent on valence states [8]. And, finally, it makes it possible to study the effect of doping with the same ions having a different charge on the features of the magnetic, electrical and optical properties, which are essentially determined by this impurity [9, 10].

It should be emphasized that since the beginning of the DMS research, the choice of material manufacturing technology has become perhaps the most important problem. This was due, in particular, to the facts that the dopants were found to be located at the grain boundaries and the presence of ferromagnetism was associated (as yet by not obscure way) with structural defects of the materials studied. It was established [1] that ferromagnetism appeared only in polycrystalline materials or rather in those that had a quite high density of grain boundaries. It turned out [1] that the specific area of grain boundaries per unit volume should exceed a certain threshold value. In addition, an important role is played not only by the structure of grain boundaries, but also by their orientation and disorientation. It was even suggested [1] that the role of the transition metal impurity was to shift ZnO to the ferromagnetic state, in particular, by shifting the aforementioned threshold to the larger values.

Unfortunately, it is impossible to predict the best or even the suitable technology for the production of DMS layers in advance, i.e. inexperimentally. In other words, it turned out to be impossible to predict whether the structural characteristics of the manufactured polycrystalline layers satisfy the largely undefined requirements necessary to obtain a material with the desired magnetic properties. Because of this, “the hunt for ferromagnetism” was carried out in the doped ZnO layers and films, prepared by a great variety of technological techniques including the liquid ceramics method, powder sintering, wet chemistry, chemical vapor deposition, plasma-assisted molecular-beam epitaxy, radio-frequency magnetron sputtering, ion implantation, pulsed laser deposition, etc.

In the present work we describe the successful attempts to reveal ferromagnetic properties in the Co-, Mn and Fe-doped ZnO layers prepared, apparently, for the first time, by printing. For this aim we applied the method of printing developed by us [11] which was

different from the conventional screen printing method used, in particular, to fabricate layers of another II-VI compounds such as cadmium sulfides and tellurides [12-14]. Of course, we were aware that to date the printing methods find only limited use in electronics, in particular, for printing of electrodes by means of electrically conductive inks [15] as well as for fabricating some dielectric layers and organic semiconductors. However, at present printing technologies are progressing rapidly. They are rather simple, cheap, may be easily integrated into industrial semiconductor technologies and, according to recent predictions [16], have even the prospect of replacing many methods of classic silicon electronics in the future.

9.2. Method for Sample Manufacturing

Zinc oxide, especially doped, is a material that cannot be produced easily enough in the form of both single crystals and polycrystalline layers with specified characteristics, which complicates its research and application. To solve this problem, we have developed a rather simple, accessible and reproducible method of printing which allowed the fast fabrication of the polycrystalline ZnO layers which had reproducible parameters and could be prepared with a controlled impurity composition [11].

As known, with screen printing of semiconductor layers [12-14], the paste which is made in a special way and contains the semiconductor material, is applied to the mesh stencil, then the paste is pushed through the cells of the stencil on the substrate surface, whereupon the upper part of the paste is removed from the stencil by a scraper. Finally, the wet screen-printed layer prepared must be dried and then recrystallized at high temperature.

This classical method of screen printing was widely and successfully used for decades for many applications primarily for applying various patterns, for example, on fabrics, and for this purpose rather liquid inks were usually used. However, unlike such printing, the screen printed layers of semiconductor materials turned out often be defective. This was due primarily to the fact that semiconductor pastes were more dense and inhomogeneous than ink. Because of this, the voids in the nodes, that is, in places where the wires or the fibers forming the mesh were intertwined, served as sources of air bubbles that passed to the wet paste when applied. As a result, the semiconductor layer, after its recrystallization, could contain a considerable amount of pores and other damages. In addition, when using stencils, mesh cells could be clogged with paste, and despite cleaning the cells, they could contain residues of dried paste which contaminated the prepared semiconductor layers and impaired their quality. The improved printing method developed by us [11] is free from the above disadvantages.

The first distinctive feature is that we abandoned the use of the stencils, and placed the paste directly on the surface of the substrate. The paste prepared contained ZnO powder, boric acid powder which served as a flux (catalyst) and propylene glycol which served as a binder. In addition, the cobalt, iron or manganese impurities were introduced into the paste by adding the calculated amount of the fine powder of CoO, FeO (or Fe_2O_3) and MnO_2, respectively.

The second distinctive feature of the developed method was that, before applying the paste to the surface of the (0001)-sapphire substrate, two parallel guides were fixed on the opposite edges of the substrate. These guides were thin wires, fibers or tapes with a thickness of 25 to 50 microns. After the paste was applied to the surface of the substrate, a scraper was moved along the substrate surface in a direction parallel to the guides. The scraper removed the paste layer above the guides. Then we removed the guides from the substrate, after which the printed wet layer of the paste was dried and recrystallized at a temperature 1000-1100 ºC for 90-120 min. Process of recrystallization was carried out in a quasi-closed volume which impedes the evaporation of the layer material and ensures the stability of the chemical composition of the semiconductor layer.

As a result of operations describes above, a strong, continuous and densely packed polycrystalline layer with no pores or bubbles was formed. Adhesion of the layer to the substrate surface was very good. The thickness of the layers after drying and recrystallization was slightly less than the initial thickness of the printed layer. This thickness could be changed by using the guides of various thickness. In most of our experiments, the thickness of the layers after crystallization was about 25 μm.

We could only hope that such a flexible method of obtaining polycrystalline layers would prove promising. Actually, the conditions for obtaining layers with ferromagnetic properties were shown to be quite stringent. As noted above, it was established [1] that ferromagnetism appeared only in polycrystalline samples and at a quite high density of grain boundaries. In addition, the ferromagnetic properties of ZnO depended significantly on the texture of films and the structure of amorphous intercrystallite layers, although the causes of the appearance of ferromagnetism remained largely unexplained.

9.3. Objectives of Researches

The studies of printed Co-, Fe- or Mn-doped polycrystalline ZnO layers summarized below were aimed:

- To find out the conditions for the incorporation of dopant ions into the printed ZnO layers and to establish the position of these ions in the ZnO lattice;
- To establish the effect of doping on the structural, optical and magnetic properties of printed ZnO layers;
- To find out differences in the structure, luminescence and magnetic properties of ZnO layers when they are doped with di- and trivalent ions of the same impurity (Fe^{2+} or Fe^{3+});
- To establish the conditions under which doping does not lead to the formation of the second-phase inclusions in the ZnO lattice.

The main practical goal of investigations was to obtain printed ZnO layers which are reproducibly characterized by the presence of ferromagnetism.

9.4. Methods for Layer Characterization

Before describing the properties of the printed layers, note that, as an analysis showed, the content of the dopant in the prepared layers did not exactly correspond to the dopant content in the initial powder. Probably, some part of the impurity atoms was not incorporated into the ZnO lattice in the course of crystallization. As a result, the impurity contents in the prepared layers were not necessarily expressed in round numbers.

The quality of the obtained layers was assessed using an optical microscope at 600× magnification. As a rule, no obvious defects (such as bubbles, cracks, pores, foreign inclusions, bulges) were observed. The adhesion of the layer to the substrate was assessed by scribing with a diamond tool. It turned out to be good over the entire surface of the fabricated layers.

The characterization of the prepared layers was made by several methods.

The morphology and composition of the samples were investigated by the method of scanning electron microscopy (SEM) using Tescan Mira 3 LMU SEM including Energy Dispersive X-ray (EDX) spectroscopy using Oxford Instruments X-Max 80 mm^2 SDD. Raman measurements were carried out by the T64000 micro-Raman system using the 514.5 nm line of an argon ion laser as the excitation source.

The Raman and photoluminescence measurements were carried in backscattering configuration using Horiba Jobin-Yvon T64000 equipped with Olympus BX41 microscope. Raman spectra were excited using an Ar-Kr laser (λexc = 488.0 nm). Laser beam was focused on the sample surface into the spot of about 0.5 μm in diameter. The laser power on the sample surface was always kept below 2 mW to avoid laser induced damages.

Photoluminescence spectra in the range 11-300 K have been taken using He-Cd laser as an excitation source, operating at 325 nm. Taking absorption coefficient (α) of ZnO to be 1.6×10^5 cm^{-1} at 325 nm [17], the characteristic penetration depth ($1/\alpha$) of excitation wavelength (325 nm) turned out to be about 60 nm. So, the photoluminescence emission was restricted within few tens of nanometer from the upper surface of the sample. All spectra were corrected for the system response using a calibrated neon source.

The methods of measurements by atom force microscopy (AFM) and magnetic force microscopy (MFM) as well as the apparatus used are described below in the Section 9.5.6.

9.5. Structural, Optical and Magnetic Properties of Printed ZnO:Co Layers

9.5.1. Morphology and Composition Analysis

To examine the morphology and composition of ZnO and ZnO:Co layers, SEM images and EDX spectra were recorded (Figs. 9.1 a-d). As seen, the SEM images revealed the formation of dense granular polycrystalline structure. An average grain size was equal to

500 ± 50 nm. The EDX spectra show major emission lines corresponding to the binding energy about 1 and 8.6 keV for zinc and oxygen, respectively, and about 0.52 keV for ZnO host material as well as the Co signals at about 0.8 keV.

The concentrations of Zn, O and Co and their relative proportions confirm the presence of Co atoms in the ZnO matrix. The quantitative analysis reveals a stoichiometric composition for undoped ZnO within the experimental error no more than 0.1 at.%. It is seen that the atomic percentage of zinc atom decreases for ZnO:Co layers in comparison with undoped ZnO, which could be related to substitution of Zn^{2+} ions by the Co^{2+} ions.

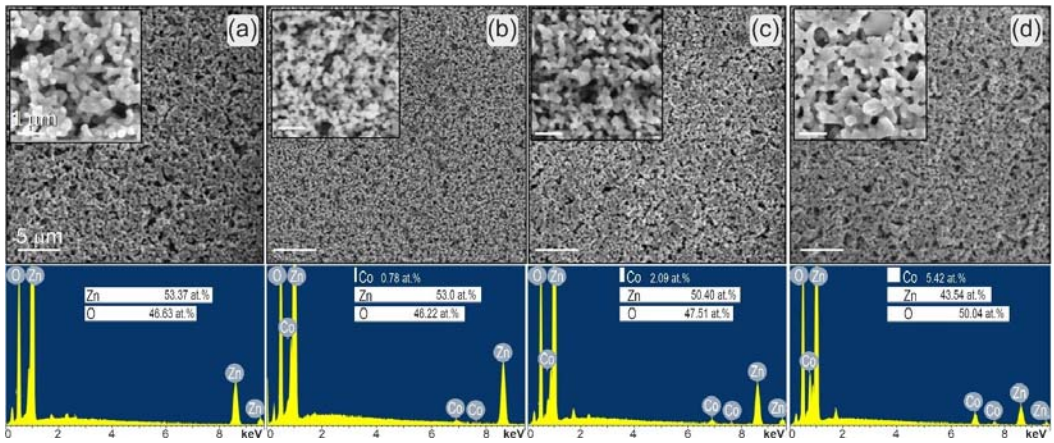

Fig. 9.1. SEM images and EDX spectra for undoped ZnO layers (a) and ZnO:Co layers (b-d). Insets show SEM images at high magnification. The average Co concentration was determined by the EDS technique.

9.5.2. X-ray Diffraction (XRD) Analysis

The XRD patterns of ZnO and ZnO:Co layers are shown in Fig. 9.2. All XRD peaks in the recorded range were identified for ZnO and it was found that a = b = 3.248 Å, c = 5.206 Å (JCPDS card No. 36-1451).The positions of the diffraction peaks and their relative intensities coincided with those reported for ZnO:Co previously [18]. It can be seen from Fig. 9.1 that all samples are polycrystalline and exhibit the single-phase ZnO hexagonal wurtzite structure. Previous investigations of Co-doped ZnO thin polycrystalline films showed [19] that the preferential orientation is caused by the minimization of the internal stress and surface energy. A strong (002) peak which dominates in the X-ray spectrum corresponds to preferential c-orientation of crystallites while domination of the (101) testifies to their mixed orientation. As to undoped and Co doped layers studied in this work, the (101) peak was the most intense, indicating a mixed orientation of crystallites along the preferred [001] direction, with the c axes tilted with respect to the substrate surface.

The XRD peak intensity decreased with increasing Co concentration without changing the crystal structure. No XRD peaks corresponding to some additional impurity phases were detected in the Co-doped layers, indicating that the layers were of single phase only.

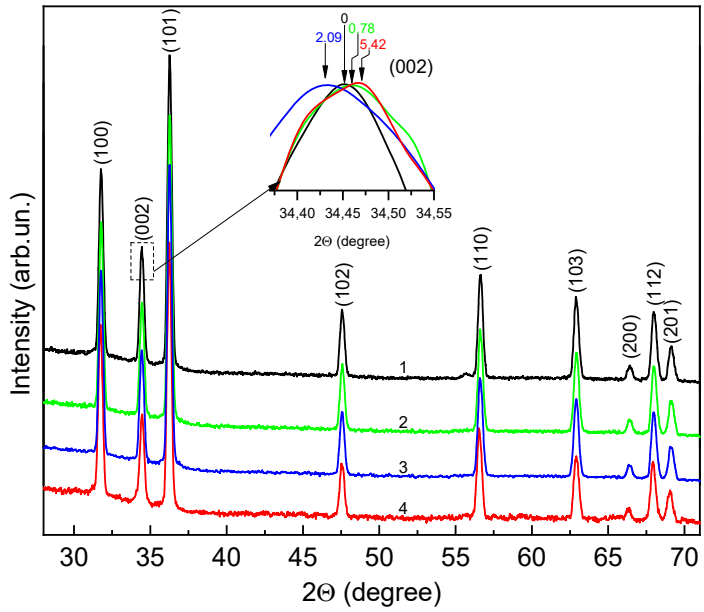

Fig. 9.2. XRD patterns of undoped ZnO layer (1) and ZnO:Co layers at Co concentrations 0.78 at.% (2), 2.09 at.% (3) and 5.42 at.% (4). The inset shows enlarged view shift of (002) XRD peak position.

It can be seen from Fig. 9.2 that doping of ZnO layers with Co result in only slight changes of the diffraction peaks position. The changes of the full width at half maximum (FWHM) values of all detected peaks are caused by a small deteriorations of the layer crystallinity. All this is indicative of the fact that Co^{2+} ions substitute Zn^{2+} ions in the crystal lattice. The intensity of all diffraction peaks decreases with increasing Co concentration. In addition, it is seen that doping with Co have a little effect on the position of the peaks: (200), (112) and (201) peaks are slightly shifted towards larger angles, whereas (002) peak is shifted to the smaller angle side. These results are due to the small ionic radius mismatch between Co^{2+} ions (0.058 nm) and Zn^{2+} ions (0.060 nm), and indicate that Co^{2+} ions substitute Zn^{2+} ions without changing the crystal structure of the layers.

As XRD studies show, lattice parameters are changed from a = 3.2497 Å, c = 5.2034 Å (c/a = 1.601) in undoped ZnO layers to a = 3.2511 Å, c = 5.2060 Å (c/a = 1.601) at 0.78 at.% of Co), a = 3.2525 Å, c = 5.2079 Å (c/a = 1.601) at 2.09 at.% and a = 3.2507 Å, c = 5.2021 Å (c/a = 1.600) at 5.42 at.% of Co) in ZnO:Co layers. Although the values of the lattice parameters are slightly changed by Co incorporation, the c/a ratio remains constant (about 1.60). Consequently, the layer doping with Co does not affect the wurtzite structure of the layers.

9.5.3. Optical Absorption Spectra

Fig. 9.3 shows the absorption spectra of the undoped and Co-doped ZnO layers in the energy range of 3.35-1.75 eV. As seen, undoped layer is highly transparent and has a sharp exciton absorption edge which is indicative of a comparatively low density of defects. Since ZnO is a direct-transition semiconductor, the optical band gap energy (E_g) of layers studied may be determined from the relationship between the absorption coefficients α and the photon energy hv by Tauc's relation: $(\alpha hv)^2 = hv\text{-}E_g$. We determined the width of the band gap by extrapolating the linear portion of the Tauc's plot to photon energy axis at $\alpha = 0$, i.e. at $(\alpha hv)^2 \rightarrow 0$. The plots of $(\alpha hv)^2$ vs. hv for undoped and Co-doped ZnO layers are shown in the insert of Fig. 9.3. Due to some changes in the in the crystal structure with doping of the ZnO layers and to the presence of tails of the density of allowed electronic states in the band gap (Urbach tails), the fundamental absorption edge is somewhat shifted towards low energies side with Co doping. The value of the optical band gap width (which is equal to Eg = 3.26 eV in undoped ZnO) is decreased to the value Eg = 2.77 in the ZnO layers at Co concentration 5.42 at.% (see the insert in Fig. 9.3). Ivill et al. [20] reported similar behaviour for Co doped ZnO thin films. A red shift of the ZnO optical band gap width at Co doping is known to be mainly due to sp-d exchange interactions between delocalized electrons of the host lattice and localized d-electrons of Co^{2+} ions substituting for Zn^{2+} ions [21] as was explained theoretically Diouri et al. [22] and Bylsma et al. [23].

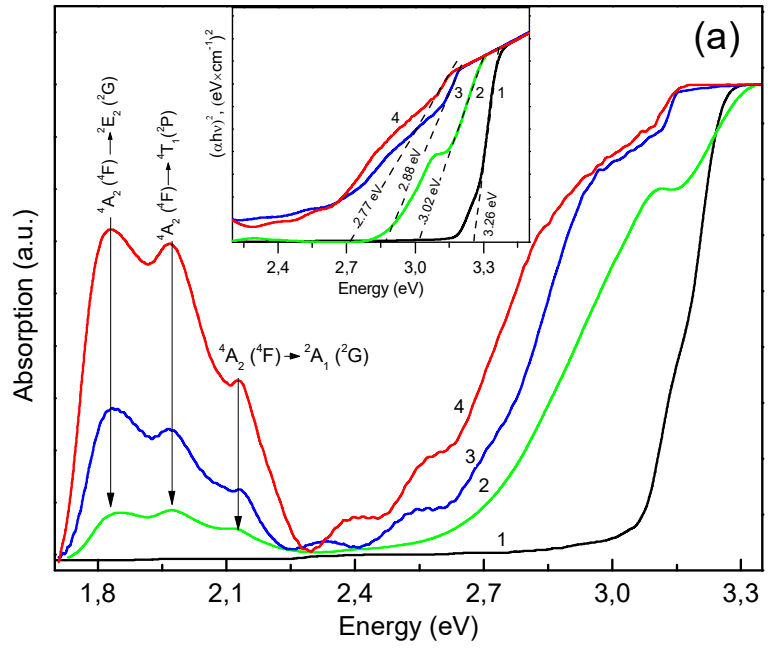

Fig. 9.3. (a) Room temperature optical absorption spectra for ZnO (1) and ZnO:Co layers with Co concentrations 0.78 at.% (2), 2.09 at.% (3) and 5.42 at.% (4). Inset to (a) shows dependence of $(\alpha hv)^2$ vs. hv. (b) The schematic energy structure of Co^{2+} intra-3D transitions in ZnO [24, 19].

In ZnO:Co layers three sharp absorption peaks are apparent in the range from 1.7 to 2.3 eV but they are absent in the undoped ZnO layers. As it was previously reported [25], these absorption peaks $^4A_2(F) \leftarrow ^2E(G)$ (1.89 eV), $^4A_2(F) \leftarrow ^4T_1(P)$ (2.03 eV), and $^4A_2(F) \leftarrow ^2A_1(G)$ (2.19 eV) are characteristic of intra-ionic *d–d* transition levels attributed to the Co^{2+} substituting for Zn^{2+} in the hexagonal lattice of ZnO crystal [19].The corresponding energy structure of cobalt ions in ZnO matrix are shown in Fig. 9.2 b. Note that the absorption peaks of d-d transitions in Co^{2+} are increased with increasing Co concentration (Fig. 9.3), whereas their spectral position is not changed. This result is an additional direct proof of the fact that the prevailing part of Co atoms was dissolved in the lattice substituting Zn in ZnO lattice [26].

9.5.4. Photoluminescence

Fig. 9.4 shows the low-temperature photoluminescence spectra of the undoped and Co-doped ZnO layers under excitation with a wavelength of 325 nm. The photoluminescence spectra can be divided into three spectral regions, those are: (1) ultraviolet region (3.236 – 3.307 eV), i.e. the intense near band edge luminescence (NBE) which has mainly the excitonic nature, and the respective phonon replica; (2) the region between 1.75 and 2.8 eV, i.e. the broad unstructured band luminescence related to deep-level emission (labeled as DLE), and (3) a structured broad band at 1.74-1.88 eV which is attributed to Co^{2+} intra-3D luminescence (see scheme shown in Fig. 9.4). Comparing the photoluminescence spectra of the samples, we found that for Co doped ZnO the NBE exciton-related emission in the range (1) decreased slightly, whereas the intensity of DLE emission in the region (2) decreases by more than 10^3 times.

The ultraviolet NBE luminescence of ZnO-based materials is due to recombination of free and bound excitons. On the other hand, the visible DLE luminescence is known to consist of several bands related to intrinsic defects: donor-type defects such as oxygen vacancy (VO), interstitial Zn (Zni), antisite (ZnO) and acceptor-type defects such as Zn vacancy (VZn), interstitial oxygen (Oi) and antisite oxygen (oxygen at zinc site, OZn) [27]. The broad green DLE band at 2.45 eV is mainly due to the existence of oxygen vacancy-related defects. The origin of the defects related to the DLE emission is the subject of the discussion thus far.

As seen from Fig. 9.4, the low-temperature NBE emission spectra of the undoped ZnO exhibit a group of narrow sharp bands in the UV region which related to the excitons bound to the neutral donor (denoted by D^0X) at 3.361 eV, ionised donor bound excitons at 3.366 eV (D^+X) [28, 29] the free excitons (FX_A) at 3.378 eV [28], the recombination of free electrons from the conduction band to the holes bound to an acceptor state (FA) at 3.314 eV [30, 31] [26, 27], followed by longitudinal optical (LO) phonon replicas with an energy separation of 72 meV (D^+X – 1LO, D^0X -1LO, FA-1LO).

As shown in previous studies [32, 33], the D^0X emission line (labeled as I4) is related to the interstitial hydrogen which is incorporated into ZnO during its synthesis and acts as a shallow donor. A conclusion was also drawn that observation of the strong D^0X bound exciton line at 3.361 eV which had a full width at half-maximum of 1.1 meV indicated

that the ZnO layers are of a good quality and could have a n-type conductivity. If it is true, the presence of similar strong emission peaks in the ZnO layers studied in this work is a sign that these layers are of a good quality as well. This conclusion is in agreement with the XRD results.

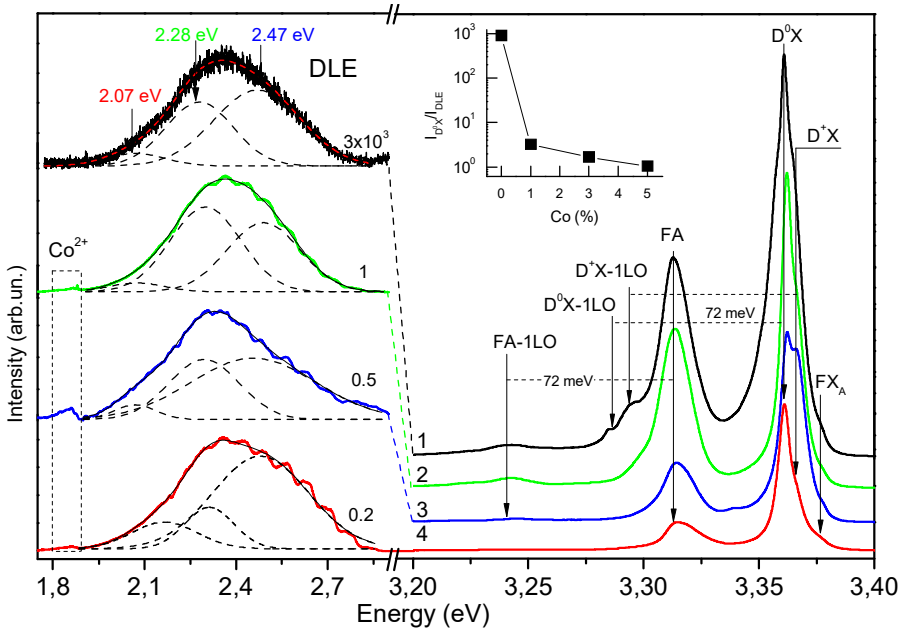

Fig. 9.4. Low-temperature photoluminescence spectra of undoped ZnO layers (1) and ZnO:Co layers with different Co content: (2) 0.78 at.%, (3) 2.09 at.%, (4) 5.42 at.%. The normalized DLE bands and their Gaussian deconvolution are shown in the region 1.75 – 2.8 eV. T = 11 K. E_{exc} = 3.81 eV (λ_{exc} = 325 nm).

It is seen from Fig. 9.4 that the intensity of exciton luminescence decreases slightly for ZnO:Co layers, confirming that Co doping induces fluorescence quenching due to a nonradiative process or charge-transfer process. Furthermore, in ZnO:Co layers the full-width of the D^0X peak is increased and the peak is shifted to a blue side by about 2.6 meV.

The intensity relation of NBE and DLE bands (INBE/IDLE) is found to depend significantly on Co content. The undoped ZnO layer shows rather low intensity of the DLE band, while the Co-doped layers show strong (by about 104 times) enhancement of DLE with increasing Co concentration (Fig. 9.4). At the same time, NBE of the highly-doped layers show a decrease by 2.5 times only as compared with undoped ZnO. The ratios INBE/IDLE shown in the inset to Fig. 9.4 enables estimating the structural perfection of ZnO films. As known, the undoped ZnO is characterized by a higher optical quality and a lower concentration of deep-level defects in comparison with highly doped material [34].

It is also known that an unstructured broad defect band in ZnO is usually a superposition of emission bands related to different structural defects [25].The broad PL band registered by us can be deconvoluted into three different component bands corresponding to different luminescence centers (Fig. 9.4). The effect of surface morphology on the green photoluminescence of ZnO was studied and the model of the transition mechanism of ZnO for the green emission was proposed [35, 36]. It is generally accepted that the radiative transition of an electron from the singly charged oxygen vacancy (V_0^+) level to the valence band is responsible for the 2.47 eV PL band. In contrast, the photoluminescence band around 2.18 eV is the contribution of the radiative recombination of a delocalized photoexcited electron close to the conduction band with a deeply electron trapped center (V_0^{++}). The weak band near 2.07 eV can be associated with deep-level transitions from the conduction band to O_i or Zn_i to O_i center [37]. The contribution of 2.47 eV green emission to observed photoluminescence spectrum was shown to be increased with increasing concentration of Co in ZnO:Co. To elucidate the origin of corresponding DLE emission in Co-doped ZnO, further investigations are required.

In addition to well-pronounced emission, we observed some features in the spectral range 1.74-1.88 eV. The emission peaks observed in ZnO:Co were previously interpreted as $^2E(G) \rightarrow {}^4T_2(F)$ (at 1.43 eV) and $^2E(G) \rightarrow {}^4A_2(F)$ (at 1.88 eV) transitions between the d-levels of cobalt ions incorporated in the ZnO host lattice (Fig. 9.5 c) [38]. Fig. 9.5 a, b shows the high resolution intra-shell luminescence of the tetrahedral Co^{2+} ions in the ZnO crystals after subtraction of the background. As seen from Fig. 9.5 b, an efficient excitation of Co ions occurs either by near resonant absorption or by energy transfer from the ZnO host lattice.

The sharp doublet lines $E_{1/2}$ (at 1.882 eV) and $E_{3/2}$ (at 1.876 eV) observed in the photoluminescence spectra can be assigned to a transition from the $^2E(G)$ doublet to the $^4A_2(F)$ ground state doublet. In fact, these two zero-phonon (ZPL) lines of spin-allowed electronic transition $^2E(G) \rightarrow {}^4A_1(^4F)$ are the main features of the emission spectrum at low temperature for all ZnO:Co samples studied (Fig. 9.5 c) [39].The energy splittings between $E_{1/2}$ and $E_{3/2}$ levels is about 0.6 meV and corresponds to the splitting of the Co^{2+} ion ground state in the ZnO lattice due to the spin-orbit interaction [37]. In addition, the spectral position and width of the intra-shell emission line is not influenced by changing the Co^{2+} concentration. With increasing Co^{2+} concentration, the ratio intensities corresponding the transitions from the $E_{1/2}$ and $E_{3/2}$ levels of the 2E(G) term to the $^4A_1(^4F)$ ground state is not changed, indicating that the populations of this levels are independent of Co concentration. The phonon side band in luminescence spectra occurs on the low energy side of the direct transition. With an increase in Co concentration, the relative increase in the phonon side band increases as compared to the intensity of the direct transition of the phonon side band, which indicates a greater imperfection of the lattice in the environment of the Co impurity and leads to a stronger phonon coupling.

The fact that the transitions from higher Co^{2+} intra-shell states than the 2E(G) components are not observed can be explained by the fact that both $^2A_1(G)$ and $^2T_2(G)$ excited states are not excited or their intensity is too low in comparison with the tail of the strong green luminescence band.

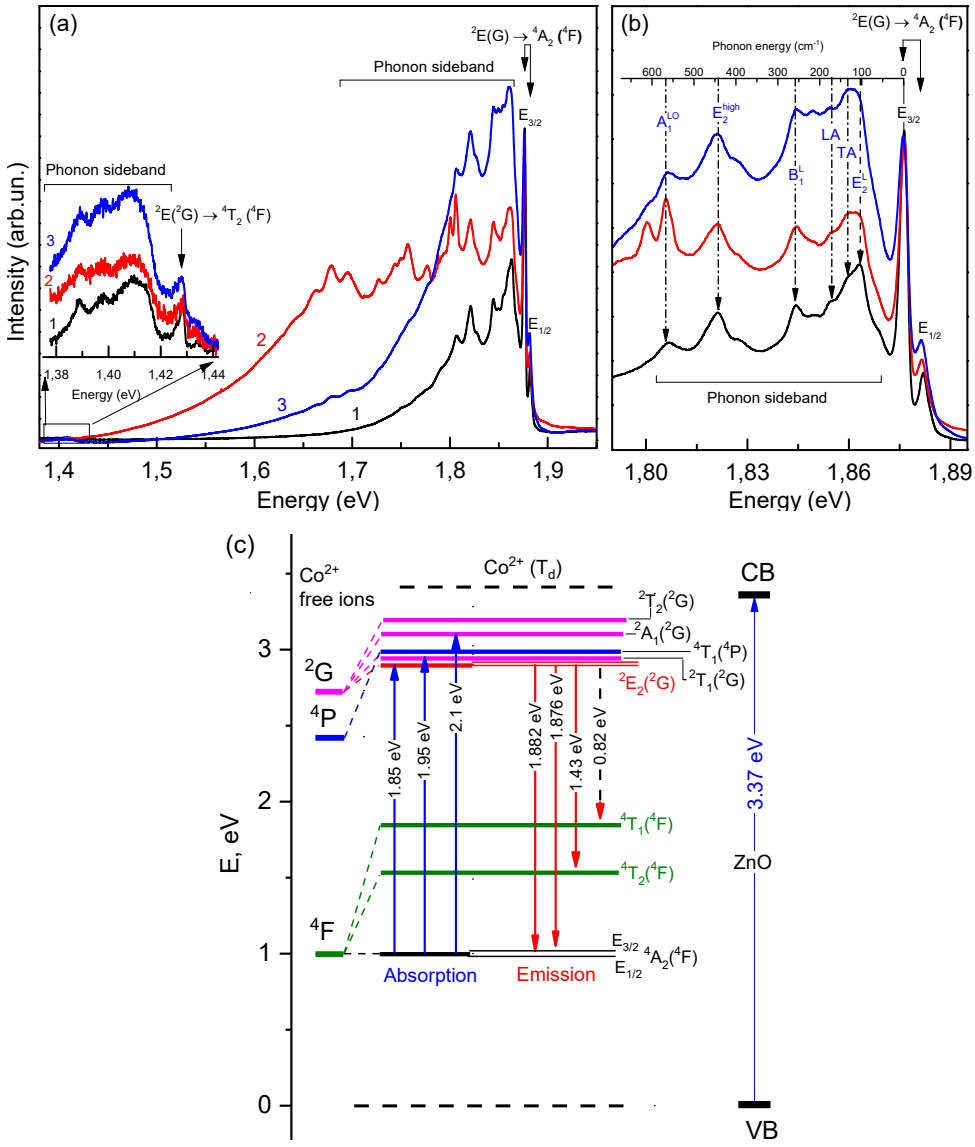

Fig. 9.5. a) The direct intra-band $^2E(G) \rightarrow {}^4A^2(4F)$ transition in Co^{2+} ions in the high resolution low-temperature PL spectra of ZnO:Co for three Co concentrations: (1) 0.78 at.%, (2) 2.09 at.%, (3) 5.42 at.%. E_{exc}=3.81 eV, T=11 K. The inset shows the region of the $^2E(G) \rightarrow {}^4T_2(^4F)$ transition with accompanied phonon sidebands in more detail; b) High-resolution spectra of the $^2E(G) \rightarrow {}^4A_2(^4F)$ transition region under sub band gap excitation E_{exc}=2.54 eV. T=11 K; c) Energy levels for absorption and emission processes in ZnO:Co.

The complex structure of the phonon side band in the emission spectra of the ZnO:Co can be interpret mainly in terms of electron-phonon coupling between the localized crystal-field Co^{2+} d-orbital states and all optical and acoustical ZnO phonons (Fig. 9.5 b) [19].

The low-temperature luminescence spectrum in Fig. 9.6 (the inset shows it in more detail) shows additional emissions in the near-infrared emission range as functions of Co concentration. The emission at 1.43 eV can be assigned to the $^2E(G) \rightarrow {}^4T_2(F)$ transition with a phonon side band which is symmetry and spin allowed [36, 37].

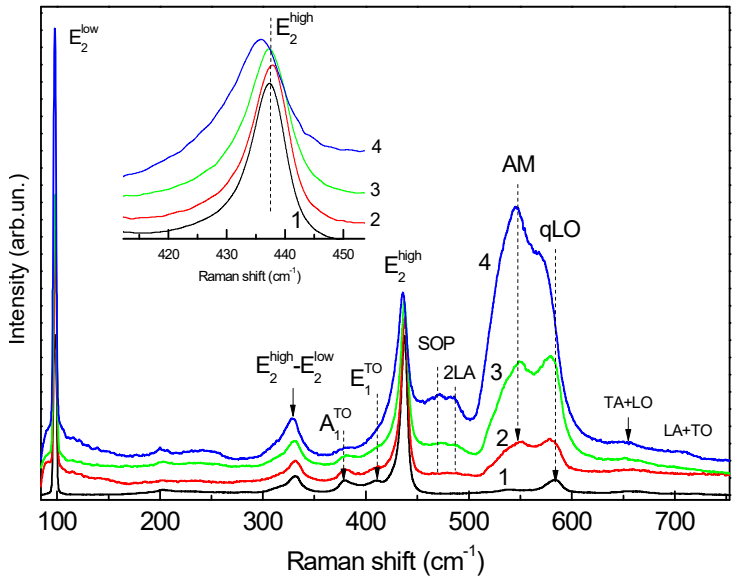

Fig. 9.6. Micro-Raman spectra of ZnO (1) and ZnO:Co layers at Co concentration 0.78 at.% (2), 2.09 at.% (3) and 5.42 at.% (4). The spectra are normalized by the intensity of the E_2^{high} mode. The low-frequency shift of E_2^{high} mode with Co doping is shown on the inset.

9.5.5. Raman Scattering

Raman scattering is known to be an effective technique to investigate the crystalline structure and defects in semiconductors. The backscattering Raman spectra for ZnO and ZnO:Co layers in the range from 90 to 800 cm^{-1} are shown in Fig. 9.4. The optical phonons at the Γ point of the Brillouin zone of wurtzite-type ZnO, which belongs to C^4_{6v} space group. According to the factor group analysis, the Raman active zone-center optical modes are $A_1 + 2B_1 + E_1 + 2E_2 + 2B_1$ [38, 39]. The polar E_1 and A_1 modes are Raman and infrared active, whereas the B_1 modes are silent. The polar A_1 and E_1 modes split into longitudinal optic (LO) and transverse optic (TO) phonon modes with different frequencies due to the macroscopic electric fields of the LO phonons. The two non-polar IR inactive E_2 modes are Raman active due to atom displacement perpendicular to the c-axis, E_2^{high} mode associated with the motion of the lighter O sublattice, and E_2^{low} mode associated with the motion of the heavy Zn sublattice.

For ZnO layer the strongest narrow peaks at 98.7 cm^{-1} (Γ = 3.86 cm^{-1}) and at 437.4 cm^{-1} (Γ = 8.8 cm^{-1}) is attributed to E_2^{low} and E_2^{high} modes, that indicate high crystal quality of the ZnO wurtzite lattice. The peak at 334 cm^{-1} is assigned to E_2^{high}–E_2^{low}which is a second-order mode caused by multi-phonon processes. The bands at 380.3 cm^{-1} and

412 cm^{-1} are attributed to A_1(TO) and E_1(TO).Weak wide bands at 475 and 482 cm^{-1} could be assigned to surface or interface phonon mode [40, 41] or multiphonon scattering in the disordered lattice due to doping [42].

Moreover, the band in the range of 574-586 cm^{-1} in the analyzed Raman spectra could be related to LO quasimode (labelled as qLO). This quasimodes are mixed symmetry LO modes in uniaxial crystals due to phonons propagating between the a- and the c-axes [43].The registration for the undoped ZnO of the quasi-LO band with a frequency close to E_1(LO) due to the fact that the c-axes of wurtzite structure are tilted with respect to the surface sample which is confirmed obtained XRD date (Fig. 9.2). As can be seen from Fig. 9.4, increases of Co concentration leads to the appearance and increase in intensity phonon band close to the position of A_1(LO), which is due to disorder of the crystal structure.

For the ZnO:Co layers, broading and decrease in intensity of the E_2^{high} mode, and its red shift up to 436.8 cm^{-1}, as shown in the inset of Fig. 9.6, indicates the introduction of Co into the ZnO lattice. It is important to note that we did not register additional Raman bands related to segregated secondary structural phases (e.g. CoO, $C_{o3}O_4$, $ZnCo_2O_4$) as it has been reported for some Co-doped ZnO samples [44-46]. These Raman results corroborate the XRD results (not shown here), as they indicate the absence of segregated secondary phase in the studied samples.

Furthermore, for the Co-doped ZnO samples appeared a strong increase in intensity of additional broad band at 500-600 cm^{-1}, which consists of several peaks with the most prominent one centered at about 547 cm^{-1} (labelled as additional mode (AM) and qLO mode). The frequency position of the qLO mode is changed from about 582 cm^{-1} to 570 cm^{-1} with increasing Co content.

The band at about 547 cm^{-1} is assigned to the Co-related additional mode (AM) associated with inelastic scattering at defect complexes containing Co^{2+} ions [36] such as the cobalt-oxygen vacancy-cobalt complexes [47]. On the other hand, ab initio calculations using the density functional theory (DFT) showed that, in hexagonal ZnO:Co, an additional band in the region about 550 cm^{-1} may appear that can be associated with the vibrational states of Co-O-Co chain complexes [36]. The observed change in the intensity of Co-related additional modes is an indication of substitutional doping of cobalt into the ZnO lattice.

9.5.6. Atom Force Microscopy and Magnetic Force Microscopy

The morphology and magnetic stray field of the layers were characterized by atomic force microscopy (AFM) and magnetic force microscopy (MFM) [48, 49] using the NanoScope IIIa Dimension 3000^{TM} scanning probe microscope with two-pass resonant technique. The two-pass technique was applied to eliminate relief influence on MFM data. The profile of the investigated sample was measured during the first run. After that the MFM tip was lifted up to 800 nm under the sample surface and was scanned along the sample repeating the surface relief (the second pass). Hard magnetic probes with a coercivity of

approximately 300 Oe (the NANOSENSORS™ PPP-MFMR probe) were used. MFM tips were magnetized before measurements along the tip axis in the magnetic field of the permanent magnet. For better identification of the surface features exhibiting magnetic properties, the surface areas were sequentially mapped with MFM probe magnetized in opposite directions (north and south poles at tip apex), and under the homogeneous external magnetic field of about 4 mT additionally applied (magnetic poles in plane of the sample). Since the investigated layers contained sometimes an electrostatic charge, all samples were discharged prior MFM measurements.

MFM data provide a direct comparison of polycrystalline grains shapes and corresponding magnetic field gradients around. Typical lateral sizes of grains in investigated samples ranged within 200-1000 nm and roughness (RMS) varied from 120 to 160 nm over uniform areas of 12×12 μm^2. The grains were found to be closely packed and have not any facets (Fig. 9.7 a). All Co-doped layers clearly showed magnetic interaction with magnetized MFM. The range of mapped MFM signal increased with Co concentration in the layers. For example, when Co concentration was increased from 0.78 to 2.09 at. %, the range of mapped MFM frequencies increased from 3 to 8 Hz. It means that magnetization of the ZnO layer became less uniform with increasing Co contamination. The MFM frequency shift became of an opposite sign if tip magnetization reversed. The mapped MFM patterns were near the same for all samples in general and could varies in features of remagnetization of individual grains under external field only. Fig. 9.7 shows some MFM data obtained for the layer with 2.09 at.% of Co. As it follows from Fig. 9.7 b-d, the magnetic stray field reviled ripple-like domains outlining grains. Grain's magnetic field oscillated with a height and small or high field value (or may be opposite poles) could be localized on a top of different grains. The 3D relief image overlapped (colored) by corresponding MFM map shown in Fig. 9.7. It visualizes localization of magnetic field on relief features. There was no dependence on the grain size.

We could suppose the complex magnetic structure of grains. It could be the set of vertical domains of opposite orientation or small domains in plane of the substrate with a vortex-like orientation within one grain. We did not simulate the fine magnetic structure since it was out of the goal of this investigation.

The self-consistent, balanced field of grains (Fig. 9.7 b) could be disturbed by external magnetic field (Fig. 9.7 c) and achieve equilibrium after demagnetization of external solenoid (after about 30 min) (Fig. 9.7 d). Magnetic field was redistributed between the grains and became of opposite contrast in some local areas. Profiles of two small grains are compared in Fig. 9.7 f for the above mentioned cases. The MFM profile was slightly modified under external field (curves 1 and 2) but there is a huge transformation after demagnetization (curve 3).

Thus, we may conclude that printed ZnO:Co layers under investigation illustrate pronounced magnetic (ferromagnetic) behavior at ambient conditions. Values of stray magnetic field detected by MFM correlate with Co content and could be effectively modified by external magnetic field of 4 mT. Fluctuations of magnetic field value over surface caused by long-range self-consistent magnetic interactions between grains but not

by a clustering of the dopant. The mapped ripple-like domain nano-magnetic structure of grains was caused by their multi-domain substructure.

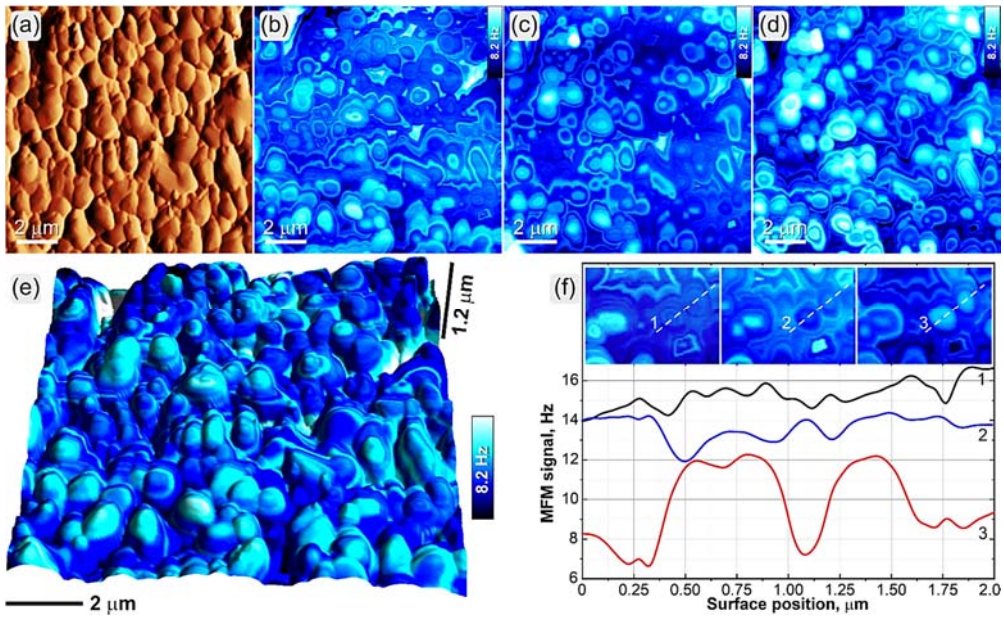

Fig. 9.7. AFM surface topography gradient image of the ZnO:Co (2.09 at.%) polycrystalline layer (a) and MFM phase images obtained over the same area prior; (b) and under (c) application of the external magnetic field of 4 mT with magnetic poles placed in plane of the sample. The MFM image captured after application of external field (d). AFM 3D topography image overlapped by the MFM map (b) is shown in (e). Evolution of MFM profile taken along dashed lines at initial state (curve 1), under external magnetic field (2) and after application of field (3). Profiles 1 and 2 are shifted up for better visualization.

9.6. Structural, Optical and Magnetic Properties of Printed ZnO:Mn Layers

9.6.1. Morphology and Composition Analysis

In order to avoid showing photographs that are practically indistinguishable from those already shown above, we will restrict ourselves to the remark that of SEM images for the ZnO:Mn layers were similar to those for ZnO:Co layers shown in Fig. 9.1. The layers had a dense granular polycrystalline structure with an average grain size 550 ± 50 nm. Fig. 9.8 shows XRD patterns of ZnO layers doped with different concentrations of MnO_2. In the undoped ZnO layers the diffraction peaks were observed at 31.88˚, 34.54˚, 36.36˚, 47.66˚, 56.7˚, 62.98˚, 66.47˚, 68.06˚ and 69.18˚, which correspond to crystallographic planes with Miller indices (100), (002), (101), (102), (110), (103), (200), (112) and (201) ZnO of the standard hexagonal structure of wurtzite (space group: P63mc (186); a = b = 0.3249 nm, c = 0.5206 nm) [50].

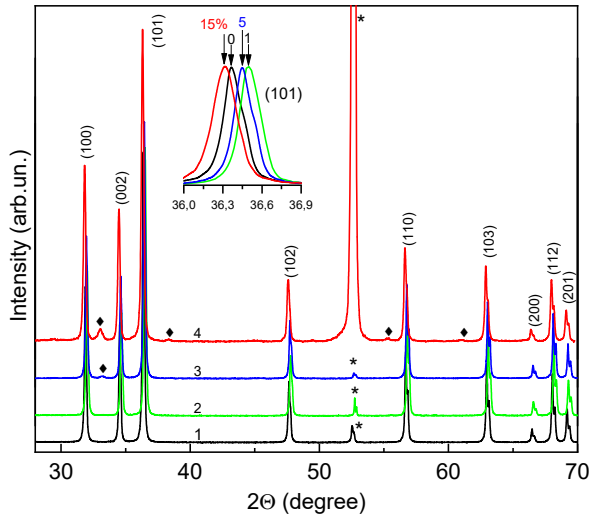

Fig. 9.8. X-ray diffraction patterns of undoped (curve 1) and Mn-doped ZnO layers with a nominal Mn concentration of 0.78 at.% (curve 2), 5.42 at.% (curve 3) and 15 at.% (curve 4) grown on a (0001)-oriented sapphire substrate The asterisk indicates the diffraction peaks of the Al_2O_3 substrate. The symbols ♦ indicate the diffraction peaks of the MnO_2 phase.

As the X-ray diffraction patterns of ZnO:Mn layers show (Fig. 9.8), the maximum intensity has a reflection peak (101) at 36.36º, which indicates a deviation of the orientation of the nanocrystallites relative to the c axis (perpendicular to the substrate plane). The small width of the diffraction peak 101) (0.16^0) is indicative of a high quality of the ZnO crystal structure. Compared with undoped layers, in the ZnO:Mn films we observe a decrease in intensity (up to 70 %) and an increase in the half-width of the XRD peaks (from 0.17 º to 19.3º). When Mn concentration was increases from 0.78 to 15 %, a shift of the 101) peak towards smaller angles (from 36.51º to 36.31º) was observed which was due to the influence of local deformations. Such deformations were caused by the substitution of Zn^{2+} ions with Mn^{2+} ions whose ionic radius (0.80 nm) is larger as compared with that of Zn^{2+} ions (0.074 nm). Wherein the parameters of the wurtzite crystal lattice a and c of ZnO:Mn determined by the ratios $a = \frac{\lambda}{\sqrt{3}\sin\Theta_{100}}$ and $c = \frac{\lambda}{\sin\Theta_{002}}$ [51], nonmonotonically decreased which point at the expansion of the crystal lattice due to the incorporation of larger manganese ions into the ZnO matrix. The results of the calculations are presented in Table 9.1.

The strain-induced broadening due to crystal imperfection and distortion was calculated using the formula $\varepsilon = \frac{\beta_{hkl}}{4\,\mathrm{tg}\,\Theta}$ [52] It is seen that the magnitude of the elastic deformations decreases, which indicates the expansion of the crystal lattice due to the incorporation of Mn2+ ions into the ZnO matrix, and hence the general relaxation of the ZnO:Mn/Al_2O_3

system. It should also be noted that the ratio c/a = 1.60 is maintained for all samples, i.e. the crystal structure is not distorted. The average size D of the crystallites was estimated by the Debye-Scherer formula $D = 0{,}89\lambda/(\Delta\cos\Theta)$, where λ is the wavelength, Θ is the diffraction angle, Δ is the line width at half height. It was found that D varies from 50 to 43 nm. These values are consistent with the data obtained by AFM.

Table 9.1. The structural parameters of printed ZnO and ZnO:Mn layers.

Doping concentration, at.%	2θ(101), deg	$I_{doped}/I_{undoped}$ (101), %	FWHM, deg.	D(101), nm	a, nm	c, nm	c/a	Strain, $\times 10^{-3}$
0	36.378	100	0.183	45	0.3240	0.5192	1.602	2.43
1	36.506	98	0.166	50	0.3228	0.5173	1.603	2.20
5	36.455	90	0.158	52	0.3233	0.5181	1.603	2.09
15	36.578	65	0.193	43	0.3247	0.5202	1.603	2.57

It should be noted that in the XRD spectra of ZnO:Mn with Mn concentration above 5 % a number of low-intensity diffraction peaks, which are absent in the XRD spectrum of undoped ZnO were recorded. Thus, the XRD peaks noted in Fig. 9.8 by a symbol ♦, (at 29.5°, 33.05°, 35.63°, 38.36°, 45.15°, 49.5° and 55.29° correspond to α-Mn_2O_3 (JCPDS No. 41-1442). Manganese oxide Mn_2O_3 is formed as a result of the reaction $4MnO_2 \rightarrow 2Mn_2O_3 + O_2$ at high temperatures (above 750 K) [53], which is less than the recrystallization temperature of ZnO:Mn layers (above1270 K). The intensity of Mn_2O_3 peak is increased with increasing concentration of the doping impurity.

9.6.2. Raman Scattering

Fig. 9.9 presents the micro-Raman spectra of ZnO:Mn layers with Mn concentrations 1, 5 and 15 at.%. Similarly to ZnO: FeO, phonon modes corresponding to the vibrations in the ZnO wurtzite structure are registered. In particular, the bands at 98.3, 437.3 and 583 cm^{-1}, which correspond to the permitted by selection rules E_2^{low}, E_2^{high} and $qA(E)_1(LO)$ phonon modes. The differential E_2^{high} – E_2^{low} and 2TA(M) ($2E_2^{low}$) two-phonon vibration modes are registered at about 333.0 and 201 cm^{-1}, respectively. Slightly pronounced phonon bands at frequencies 378 and 408 cm^{-1} correspond to the forbidden by selection rules in the backscattering geometry $A_1(TO)$ and $E_1(TO)$ phonon modes, respectively.

As known, the E_2^{low} and E_2^{high} phonons correspond to the vibrations of zinc and oxygen atoms in the cationic and anionic sublattices of wurtzite ZnO structure in the plane perpendicular to the *c* axis and, hence, are sensitive to the disorder of the ZnO crystal structure. In the Raman spectra of the layers studied, with increasing Mn concentration from 1 % to 15 %, this effect manifested itself as a decrease in intensity, an increase in half-width from 13.6 to 24 cm^{-1} and a low-frequency shift of the maximum of E_2^{high} band from 437.2 to 430.4 cm^{-1}. The increase in the half-width of the E_2^{high} and E_2^{low} bands is

due to violations of translational symmetry caused by internal defects and/or by Mn impurity and its non-uniform inclusions or non-uniform distribution. The low-frequency shift of the E_2^{high} band is indicative of the substitution of Zn^{2+} ions by Mn^{2+} ions in the ZnO crystal lattice and is due to the Mn-induced elastic tensile deformations due to the size differences between Mn^{2+} ions (0.080 nm) and Zn^{2+} ions (0.074 nm).

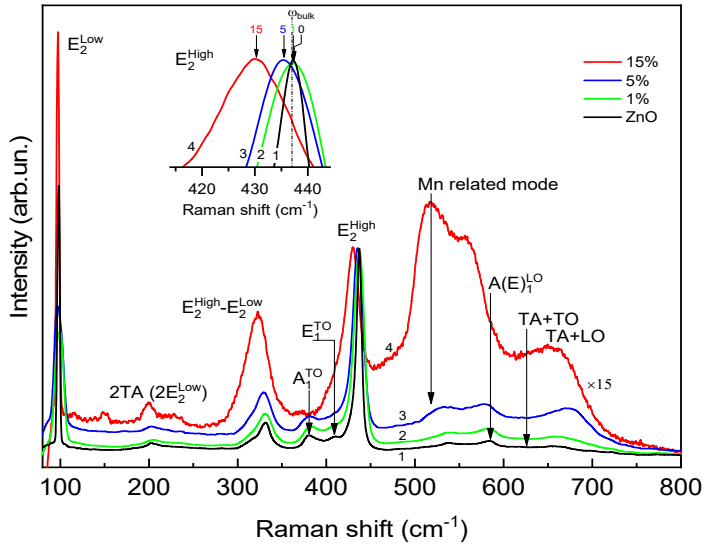

Fig. 9.9. Micro-Raman spectra of ZnO:Mn layers with nominal Mn concentrations 0, 1, 5 and 15 at.%. The insert shows the shift of the frequency position of the E_2^{high} phonon mode as a function of Mn nominal concentration in ZnO layers.

The additional complex vibrational band was also detected in ZnO:Mn spectra at about 520 cm^{-1}, which is an evidence of Mn incorporation into the ZnO lattice and the intensity of which increases with increasing Mn content [54, 55]. The nature of its origin was the subject of controversy among several research groups [56, 57]. Theoretical calculations of the phonon density of states (LPDOS) of Mn and Zn atoms in ZnO implanted with Mn+ ions have shown that the band at 527 cm^{-1} appear only in the LPDOS of the Zn atom, where Mn atoms partially replace O atoms in the ZnO crystal lattice [58].

Yadav et al. [59] considered that the band at 524 cm^{-1} in Mn-doped ZnO films may be explained as a disorder-activated $2B_1^{low}$ silent mode of ZnO. Hu et al. [60] observed a band at 528 cm^{-1} in heavily doped Mn-doped ZnO films and attributed it to the characteristic mode of Mn_2O_3. Cao et al. [61] observe a band at 523 cm^{-1} and attributed it to the local vibrations of the Mn-V_{Zn} complexes. Thus, in the Raman spectra of the samples, besides the conventional vibrations observed in undoped ZnO, there were some Mn-related Raman local vibrations. The origin of these peaks continues to be debated.

9.6.3. Photoluminescence

Fig. 9.10 shows the photoluminescence spectra of ZnO:Mn layers with a nominal Mn concentration 1, 3 and 15 at.%. As can be seen, the spectra consist of well-defined peaks at 3.369, 3.356 and 3.31 eV which correspond to the recombination of free exciton (FX), exciton bound to the neutral donor (D^0X) and exciton bound to the acceptor (FA), which are located about 13 and 59 meV below the peak FX, respectively. In addition, in the low-energy region of the spectrum, LO-phonon replicas of the FA band (F -nLO) are recorded at 3.238 eV and 3.166 eV with an energy separation of 72 meV.

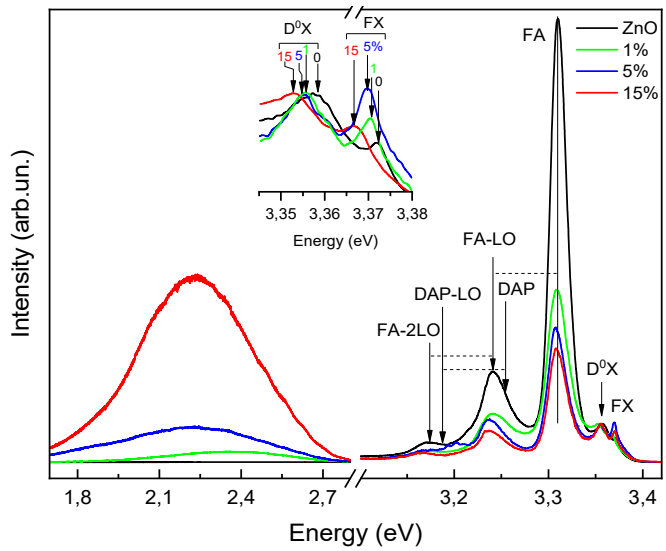

Fig. 9.10. Photoluminescence spectra of ZnO:Mn layers with nominal Mn concentrations 0, 1, 5 and 15 at.%. The corresponding phonon replica with longitudinal optical phonons (LO) are indicated. The insert shows the shift of the frequency position of exciton bands depending on the nominal Mn concentration in ZnO layers. T = 77 K, E_{exc} = 3.81 eV (λ_{exc} = 325 nm).

As the Mn concentration increased, the NBE radiation intensity decreased and its half-width increased (see Fig. 9.10, inset). At the same time, the ratio of the band intensities NBE/DLE decreased from 100 to 0.6. The attenuation of the photoluminescence edge band can be caused by the loss of photogenerated carriers due to nonradiative transitions to the energy levels of defects resulting from Mn incorporation in the ZnO crystal lattice.

With increasing manganese concentration in the ZnO layer, a low-energy shift of the FX and D^0X bands is observed to about 3.366 and 3.353 eV, respectively. This decrease of the band gap width of ZnO:Mn layers can be interpreted in terms of sp-d spin exchange interactions between the electrons in the conduction band and localized d electrons of Mn^{2+} ions [62] or by local tensile deformations due to replacement of Mn^{2+} ions with larger Zn^{2+} ions.

The luminescence band at 3.31 eV was observed in high-quality epitaxial ZnO films as well as in nanocrystalline ZnO films and ZnO nanowires [63]. As follows from the discussion below (see photoluminescence of ZnO:Fe), the emission band at 3.31 eV in undoped and Mn-doped ZnO layers may be connected with the electron transitions from the conduction band to the hole states induced by zinc vacancies V_{Zn}. The decreases in intensity of this emission band at increased Mn concentrations was observed. This behaviour can be related to the processes of replacement of Zn^{2+} ions and/or Zn vacancies with Mn^{2+} ions.

The donor-acceptor-pair (DAP) emission band positioned at 3.25 eV was observed in the photoluminescence spectra of ZnO grown by different methods. In particular, DAP emission was observed in H- and Zn-implanted ZnO single crystals [64] and in the nominally undoped ZnO films [65]. The natural of this DAP emission to associate it with radiative transitions involving acceptors and donors due to uncontrolled intrinsic structural defects that arise in the process of preparing ZnO films. The bands at 3.178 and 3.106 eV correspond to its phonon replicas DAP-LO and DAP-2LO, respectively.

In addition, in the photoluminescence spectrum of ZnO:Mn layers a wide green-yellow emission band with a peak at about 2.23 eV was observed. The origin of the deep-level emission (DLE) in ZnO is highly controversial. The DLE peak of ZnO is commonly attributed to radiative recombination with the participation of various defects such as vacancies of oxygen (V_O) and of zinc (V_{Zn}) [66] as well as interstitual oxygen atoms (O_i) [67]. With increasing Mn concentration, the intensity of the green-yellow band was increased, which was associated with an increased concentration of the singly ionized oxygen vacancy (V_O^+) in ZnO and the emission results from the radiative recombination of a photogenerated hole with an electron occupying the oxygen vacancy [68], or recombination of trapped electrons at the deep donor level of Zni with trapped holes at singly ionized zinc vacancies Zni acceptor levels [69]. Thus, the concentration of ionized oxygen vacancies (V_O^+) in Mn-doped ZnO is related to the concentration of manganese.

The presence of V_O^+ centers can lead to the appearance of bound magnetic polarons, due to the polarization of the spins of the unfilled 3D electronic shell of the magnetic impurity Mn^{2+}. As the number of V_O^+ defects increases, the volume occupied by magnetic polarons increases also, and this results in the increase of probability of formation, by Mn ions, of long-range magnetic ordering in the ZnO layers. When overlapping neighboring polarons, bipolar spins tend to be oriented in the direction of the external magnetic field [68]. These effects can lead to high-temperature ferromagnetism in polycrystalline Mn-doped layers.

9.6.4. Atom Force Microscopy and Magnetic Force Microscopy

The results of studying the morphology and magnetic topography of ZnO:Mn layers obtained by the methods of atom force microscopy and magnetic force microscopy turned out to be similar to those of ZnO:Co layers which were described above in the Section 9.5.6. It was shown also that, ZnO:Mn layers exhibit ferromagnetic properties similar to those of the ZnO:Co layers. A comparison of the magnetization of Co-, Mn- and Fe-doped layers will be carried out below in the Section 9.7.4.

9.7. Structural, Optical and Magnetic Properties of Printed ZnO:Fe Layers

9.7.1. Morphology and Composition Analysis

The composition and crystal structure of undoped ZnO and doped with FeO and Fe_2O_3 polycrystalline ZnO layers were characterized by X-ray diffractometry (Fig. 9.11).

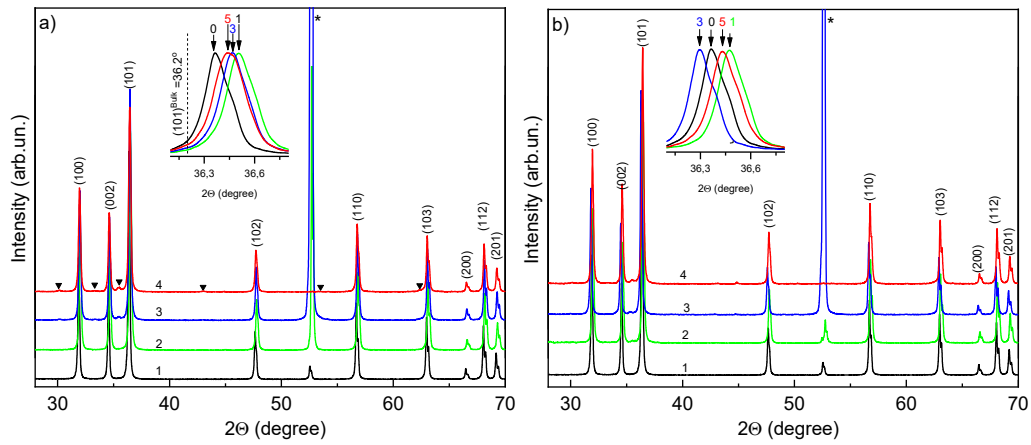

Fig. 9.11. X-ray diffraction patterns of undoped ZnO (curve 1), ZnO:FeO (a), and ZnO:Fe_2O_3 (b) layers with a nominal impurity concentration of 1 % (curve 2), 3 % (curve 3) and 5 % (curve 4). The asterisk indicates the diffraction peaks of the Al_2O_3 (sapphire) substrate. The symbols ▼ indicate the position of diffraction peaks of the secondary phase Fe_3O_4.

In the undoped ZnO layers, a number of intense and narrow diffraction peaks were observed, the angular position of which agreed well with the Joint Committee Powder Diffraction Standards (JCPDS) card for ZnO (JCPDS 036-1451) and corresponds to the monophasic polycrystalline structure of zinc oxide 636c space group [69]. Diffraction peaks of any other structural phases of ZnO as well as any metal clusters in the undoped ZnO layers were not detected.

Any amorphous phase or significant broadening of the peaks due to low-dimensional effects were not detected, so we may conclude that the prepared layers were textured and polycrystalline [70]. On the diffractograms of the ZnO layers both undoped and doped with FeO or Fe_2O_3, the reflection peak (101) at 36.37° had a maximum intensity which indicated a deviation of the orientation of the crystallites along the preferred [0001] direction, with the c axes tilted with respect to the substrate surface. The position of the peak (101) was shifted towards smaller angles compared to (101) the peak of relaxed bulk ZnO crystal (36.2 °), which was due to the mismatch of the lattice constants (about 18 %) between the ZnO layer and sapphire substrate [71]. The small width (0.18 - 0.20^0) of all diffraction peaks indicated a sufficiently high quality of the ZnO crystal structure [72]. As compared with the undoped ZnO layers, the both types of Fe doped ZnO layers showed a decrease in the intensity and an increase in the half-width of the XRD peaks. For ZnO:FeO layers with FeO concentration of 1 %, a sharp shift of the (101) peak towards larger angles

up to 36.51° was observed. At the same time an increase in the concentration of Fe_2O_3 from 1 % to 5 % leaded to a gradual shift of the peak (101) towards smaller angles (see Table 9.1). This behavior (101) of the peak can be associated with a different charge state of iron ions when they replaced Zn^{2+} ions in ZnO matrix [73].

To explain these phenomena, note that the ionic radius of Fe^{2+}, Zn^{2+} and Fe^{3+} ions are equal to 0.78 Å, 0.76 Å, and 0.64 Å, respectively [74]. Therefore, a sharp shift of the peak (101) at a Fe_2O_3 concentration of 1 % is due to significant compression deformations resulted from the substitution of Zn^{2+} ions by Fe^{3+} ions upon entering the lattice. In this case, oxygen ions O^{2-} will be directed to Fe^{3+} ions to maintain the balance of charge [75, 76]. In the case of ZnO doping with FeO, the value of the shift of the peak (101) towards small angles due to the replacement of Zn^{2+} ions by Fe^{2+} ions reflects the fact that the sizes of these two ions are close to each other [77]. In the case of ZnO doping with Fe_2O_3 the nonmonotonic shift of the diffraction peak (101) reflects the different charge state of Fe^{3+} and Zn^{2+} ions. In this case the concentration of zinc ions decreases to compensate for the charge, which inhibits the growth of ZnO crystallites and worsens their crystallinity.

To determine the effect of iron ions on the structural parameters of ZnO polycrystalline films, a number of characteristic values were determined, in particular, the size of the crystallites (D) lattice parameters (a, c, c/a), stress. The results of the calculations are presented in Table 9.2.

Table 9.2. The structural parameters of undoped, FeO-doped and Fe_2O_3-doped ZnO layers.

Dopant concentration, at.%	2θ (101), deg	$(I_{doped})/I_{undoped})$ (101), %	FWHM, deg.	D(101), nm	a, nm	c, nm	c/a	Strain, $\times 10^{-3}$
0	36.378	100	0.183	45	0.32403	0.5192	1.602	2.43
ZnO:FeO								
1	36.514	95	0.193	43	0.3227	0.5173	1.603	2.55
3	36.474	90	0.206	40	0.3231	0.5178	1.603	2.73
5	36.450	79	0.222	37	0.3233	0.5182	1.603	2.94
$ZnO:Fe_2O_3$								
1	36.483	86	0.191	43	0.3230	0.5177	1.603	2.53
3	36.307	79	0.178	46	0.3248	0.5202	1.602	2.37
5	36.442	44	0.219	38	0.3234	0.5183	1.603	2.90

It should be noted that the XRD spectra of ZnO:FeO and $ZnO:Fe_2O_3$ include also layers the low-intensity diffraction peaks that do not belong to the XRD peaks of ZnO. For example, the XRD peaks noted in Fig. 9.2a by a symbol ▼ and recorded at 30.1°, 35.5°, 43.1° and 53.5° correspond to the crystal planes (220), (311), (400), (422) and (511) of the mixed oxide $FeO+Fe_2O_3$ which has a spinel structure (according to JCPDS No. 65-3107 [78], it usually written as Fe_3O_4). It is known that Fe_3O_4 is formed by the reaction of

$3Fe + 2O_2 \rightarrow Fe_3O_4$ at a temperature of 150-600 ºC and by the reaction $3Fe_2O_3 + H_2 \rightarrow 2Fe_3O_4 + H_2O$ at 400 ºC. Since the annealing temperature of the layers was about 1000 °C, two types of iron oxide (Fe^{2+} and Fe^{3+}) coexist in them, which is manifested in the nonmonotonic shift of ZnO diffraction peaks [79]. Manifestation of Fe_3O_4 inclusions increases with increasing concentration of the dopants, which may be due to some phase segregation.

9.7.2. Micro-Raman Studies

The Raman spectra were studied to establish the structural and crystalline quality of the layers as well as to determine the location of Fe atoms in the crystal lattice of ZnO:FeO and ZnO:Fe_2O_3 layers.

Fig. 9.12 presents Raman spectra of undoped and doped with FeO (i.e. with Fe^{2+} ions) (a) and Fe_2O_3 (i.e. with Fe^{3+} ions) (b) at nominal concentration of iron 1, 3 and 5 at.%. In the Raman spectrum of undoped ZnO film there are well-known intense phonon bands at about 98 cm^{-1} ($\Gamma \sim 1.6$ cm^{-1}) and 437 cm^{-1} ($\Gamma \sim 5.0$ cm^{-1}), which correspond to E_2^{low} and E_2^{high} phonon modes ZnO, respectively. The value of the frequency E_2^{high} of the band in the ZnO layer is shifted to the high frequency side by about 0.6 cm^{-1} as compared to the bulk ZnO crystal ($\omega_{bulk} = 437.0$ cm^{-1}), which corresponds to the elastic compressive stress in the plane of the layer growth [80]. In addition, in all Raman spectra there are small bands at 378 cm^{-1} and 412 cm^{-1} that correspond to A_1(TO) and E_1(TO) phonon modes of ZnO. In the Raman spectra of all ZnO:FeO and ZnO:Fe_2O_3 layers, the bands E_2^{high} and E_2^{low} are broad due to violations of translational symmetry caused by the internal defects and/or by the Fe impurity (insert in Fig. 9.3). For ZnO:FeO layers, the position of the maximum of the band E_2^{high} (see the insert in Fig. 9.3 a) is shifted from 437.1 cm^{-1} to 435 cm^{-1}, while for ZnO:Fe_2O_3 layers a shift from 437.2 cm^{-1} to 436.4 cm^{-1} occurs (Fig. 9.3 (b)). This may be due to the change in the binding energy of Zn-O as a result of the replacement of Zn^{2+} ions by Fe^{2+} or Fe^{3+} ions and to the elastic deformations resulted from the differences in ionic radii. Substitution of Zn ions by Fe ions also affects directly the position and half-width of the E_2^{low} phonon band. In particular, with increasing concentration of the impurity, the intensity of this band is decreased and the band is shifted towards low frequencies from 98.5 to 98.2 cm^{-1} for ZnO:FeO and to 98.1 cm^{-1} for ZnO:Fe_2O_3. Since the E_2(low) phonon mode is mainly related to the vibrations of the zinc lattice and the ionic radius of iron (0.67 Å) is smaller than that of divalent zinc Zn^{2+} (0.74 Å), the displacement and broadening of this band may indicate the replacement of Zn^{2+} ions with Fe^{3+} ions in the ZnO lattice [81, 82]. The tetrahedral nodes in the wurtzite structure are occupied with Zn^{2+} ions, and at their replacement with the impurity ions Fe^{2+} or Fe^{3+} leads to formation of new defects in the crystal lattice.

In the Raman spectrum of undoped ZnO film, a wide band is also observed at 584 cm^{-1}, which corresponds to the superposition of both LO (A_1 and E_1) vibrational ZnO modes. The increase of this band, the intensity of which is usually small due to the processes of destructive interference between the mechanisms of Fröhlich interaction and the deformation potential in the scattering process on LO phonons in ZnO, is due to distortion of translational symmetry connected with the intrinsic and impurity structural defects [83].

The introduction of Fe^{2+} (Fe^{3+}) ions into the ZnO crystal lattice leads to a low-frequency shift of the $A(E)_1(LO)$ band from 585 to 578 cm^{-1} which may be due to a decrease in the misorientation of crystallites from c axis ([0001] direction.

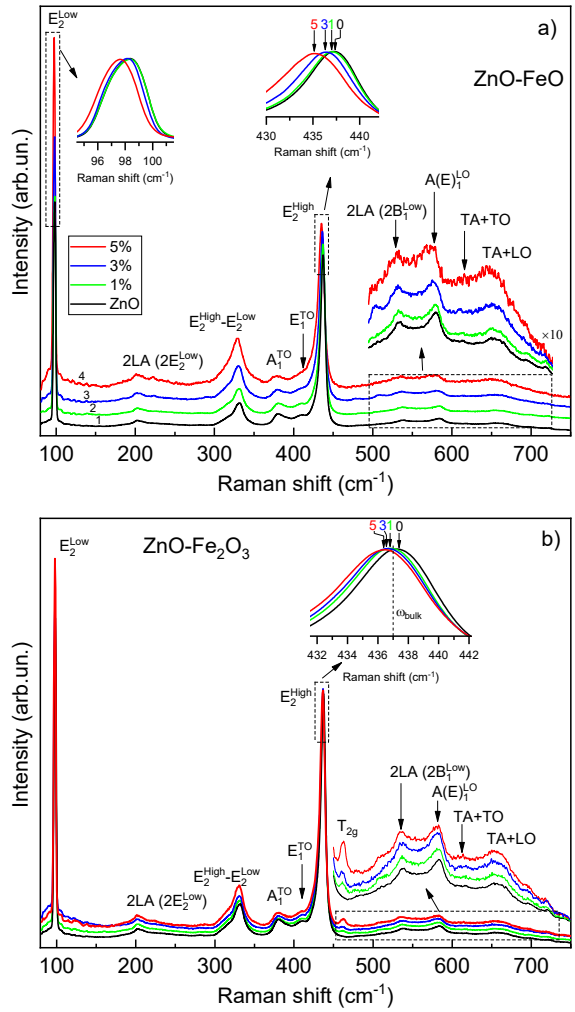

Fig. 9.12. Micro-Raman spectra of ZnO layers doped with FeO (a) and Fe_2O_3 (b) with nominal Fe concentrations 0, 1, 3 and 5 %. Inserts show the frequency position of E_2^{low} and E_2^{high} phonon modes at different concentration of Fe in ZnO layers.

It was also observed that introducing of iron ions or of new structural defects results in the increase in the intensity of the complex-shape vibrational band in the frequency range of 500-750 cm^{-1}. Structural defects of the crystal lattice introduced into the ZnO matrix during doping induce a structural disorder that disrupts the translational symmetry of the allowed phonons, which leads to a change in the shape and intensity of the bands [84]. In the Raman spectra of all samples (Fig. 9.12 a, insert), bands at 204, 331.7 and 539 cm^{-1} are also observed, which correspond to the light scattering with the participation of

second-order phonons 2TA or $2E_2^{low}$ (M,Γ), E_2^{high}- E_2^{low}(Γ) and 2LA or $2B_1^{low}$)(Γ,M), respectively [85]. The bands at 618 and 653 cm^{-1} correspond to the combination of TA+TO(H,M) and TA+LO(L,H) phonons of the second order.

It should be noted that for ZnO:Fe_2O_3 layers there is an additional new band is detected in the frequency range 455-465 cm^{-1}. The intensity of this band increases with increasing impurity concentration. This bans is usually associated with T_{2g} phonons in $ZnFe_2O_4$ [86].

Supposing that the signal at 462 cm^{-1} arises from the vibrations of the AO_4 tetrahedral groups, the increase in the intensity and high wave numbers shift is again a direct consequence of the exchange of Zn atoms by lighter Fe atoms [87]. This band is not observed for ZnO:FeO layers which is indicative of their higher structural perfection and of the absence of additional phases.

9.7.3. Photoluminescence

Fig. 9.13 presents the low-temperature photoluminescence spectra of ZnO layers doped with FeO (a) and Fe_2O_3 (b) at nominal Fe concentrations 1, 3 and 5 at. %, respectively. As seen, the spectra of both types of layers have a similar character and consist of two separate bands of radiation in the ultraviolet (NBE) and green-yellow regions 1.8 ÷ 2.7 eV of the DLE spectrum.

The spectra of NBE radiation of undoped and Fe-doped ZnO layers and doped with iron ions include a number of intense bands that belong to the free and bound excitons (FX and BX).

As known, free excitons usually appear only in high-quality structurally perfect crystals. In general, the energy of bound excitons BX is lower than that of FX, and they can also be classified as donor-bound exciton (DX) and acceptor-bound exciton (AX). For the undoped ZnO layer (see Fig. 9.13a, insert), an intense band at 3.359 eV (Γ = 24 meV) is recorded in in the high-energy region of the spectrum, which corresponds to the exciton recombination of bound excitons on shallow neutral donors (D^0X).

9.7.4. Magnetic Properties of Fe-doped ZnO Layers

The local magnetic properties of ZnO layers with different contents of magnetic impurities were studied by the method of gradient magnetic force microscopy (MFM). The result of the measurements is a map of the gradient of the magnetic field of scattering over the surface of the sample quantified by the shift of the oscillation frequency of the magnetic probe (Fig. 9.14). MSM measurements demonstrated the peculiarities of the formation of the magnetic microstructure of ZnO:FeO and ZnO:Fe_2O_3 layers with variations in the concentration of magnetic impurities in the range of 1-5 %. At room temperature, the magnetic microstructure was a characteristic superposition of the film grain field.

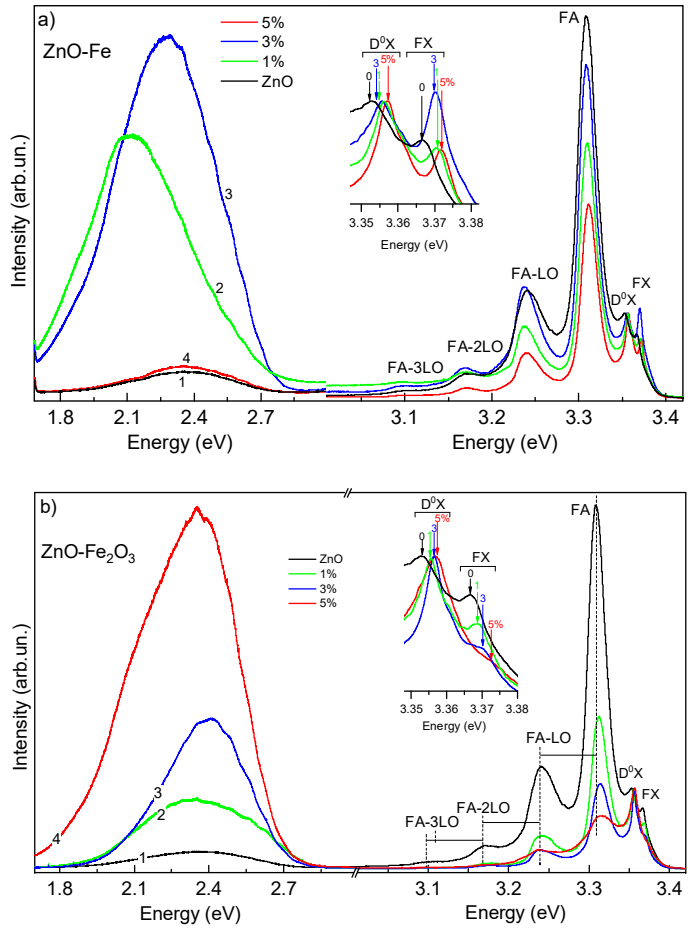

Fig. 9.13. Low-temperature photoluminescence spectra of ZnO layers doped with FeO (a) and Fe_2O_3 (b) at nominal Fe concentrations of 1, 3 and 5 at.%. T = 77 K, E_{exc} = 3.81 eV (λ_{exc} = 325 nm).

The increase in the impurity content resulted in the increase of the stationary magnetic scattering field above the surface of the sample, which was manifested in the form of lines of the light-dark contrast. Individual grains in the layer had a high level of magnetization, but it was not associated with segregation/clustering of the iron impurity. As the content of the magnetic impurity increased, there was a tendency to decrease the grain size of the layers (for ZnO:FeO from 500 nm to 280 nm).

The values of magnetization of the layers with different Fe contamination were evaluated by the macro-force magnetic interaction of the layers with the applied external magnetic field (Table 9.3). From the dependences of the strength of the magnetic interaction on the layer-magnet distance, relative values of magnetization were obtained. For convenience of comparison, the values of magnetizations were normalized to the maximum inherent in the sample ZnO:Fe_2O_3 (5 %).

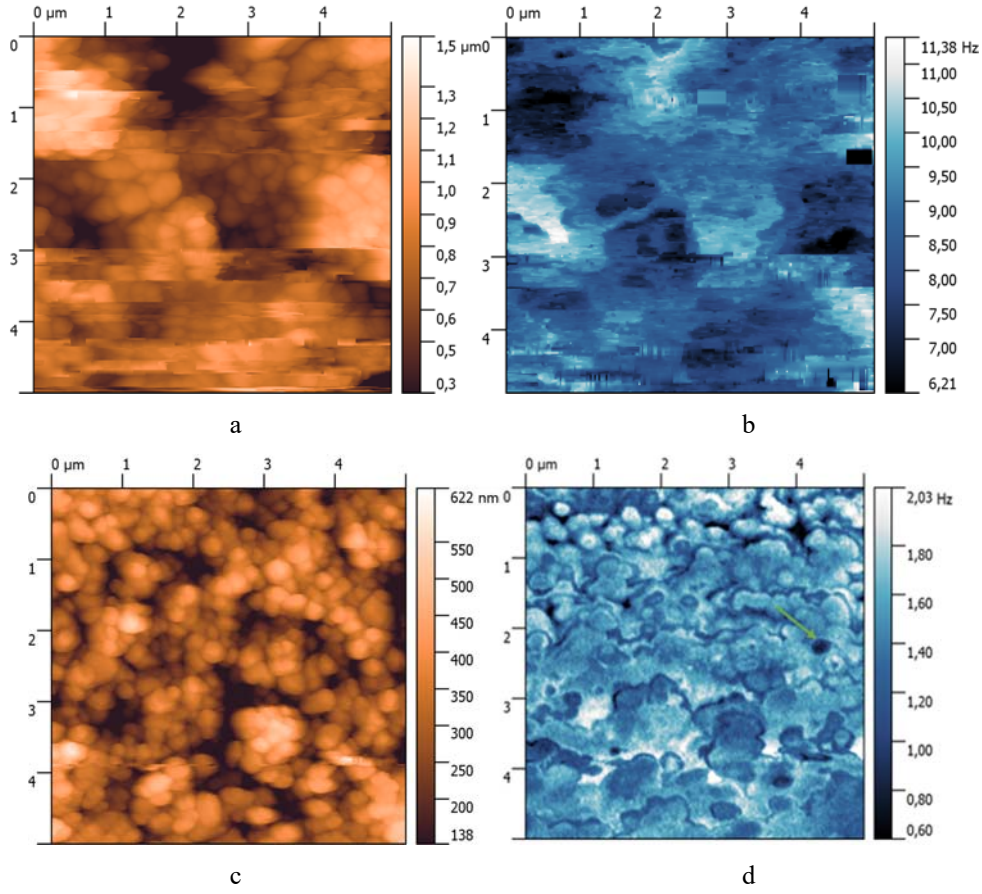

Fig. 9.14. Relief maps (left) and magnetic field scattering gradient (right) for ZnO samples with iron impurity content of 1 % (a, b) and 5 % (c, d).

Table 9.3. Relative magnetization of ZnO:FeO and ZnO:Fe_2O_3 layers.

№№	Fe content in the layers, at.%	Magnetization ZnO:Fe_2O_3, %	Magnetization ZnO:FeO, %
1	1	14.5	9.8
2	3	61.0	44.2
3	5	100.0	77.5

The fact that the magnetization of the layers increases when the layers are doped with trivalent rather than divalent ions is not unexpected. It was previously observed for ZnO films doped with Co^{2+} and Co^{3+} ions and was explained by fact that the incorporated trivalent ion may supply the third ("extra") electron of the outer shell to the conduction band of the host semiconductor. It results in the increase of conductivity of the doped layer and promotes the carrier mediated mechanism of magnetization [88, 89].

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As regards the comparison of the magnetization of ZnO layers with different dopants, it should be noted that the value of magnetization of the layers doped with Fe_2O_3 exceeded the magnetization not only of the layers doped with FeO but also of the ZnO:Co and ZnO:Mn layers studied in the present work. The magnetization of the layers ZnO:Co and ZnO:Mn was approximately the same as that of the layers doped with FeO.

We managed to prepare inclusions-free ZnO layers with Fe contamination about 12 %. Their magnetization was found to be higher than at lower iron concentrations, and these layers were even attracted to a magnet brought to their surface. This could serve as one more proof of the ferromagnetism of the layers.

9.8. Conclusions

The printed layers of diluted magnetic semiconductors (DMS) were first manufactured and researched. The ZnO layers doped with Co, Mn as well as with bivalent or trivalent Fe ions were printing by a new stencil-free technique developed by the authors. This technique makes it possible to obtain layers free of pores and other damages inherent to layers prepared by a screen printing method commonly used for printing semiconductor layers. To establish the structural, optical and magnetic properties of the layers, the methods of scanning electron microscopy, energy dispersive X-ray spectroscopy, atom force microscopy, magnetic force microscopy as well as the methods for studying the optical absorption, the low-temperature photoluminescence and Raman scattering, were jointly applied. It was shown that the prepared layers had a densely packed and rather uniform polycrystalline wurtzite structure with a typical grain size about 550 nm. The lattice parameters were slightly changed by impurity incorporation without changing the ratio of lattice parameters c/a. As investigations showed, during doping, Co^{2+}, Mn^{2+}, Fe^{2+} or Fe^{3+} ions substituted Zn^{2+} ions in the ZnO lattice and were uniformly distributed in the Zn^{2+} sites of the lattice. The latter is especially important since the uniform distribution of these impurities was not previously observed in ZnO layers obtained by other technological methods.

The use of a wide range of physical research methods made it possible to establish the effect of doping on the structural, optical, recombination, and other properties of the layers, as well as on the width of their band gap, the size of the crystal cell, etc. In carrying out the physical interpretation of the obtained experimental data, the authors used and discussed the long-term data of other authors concerning this subject, which gives the article some features of a review.

It was shown that printed ZnO layers doped with all impurities under investigation illustrate pronounced ferromagnetic behavior at ambient conditions. The magnitudes of the magnetic field correlated with the impurity content. The levels of doping with different impurities that make it possible to obtain layers free of second phase inclusions, were established. It was shown, in particular, that although the fluctuations of magnetic field value over the layer surface were observed, those fluctuations were caused by long-range self-consistent magnetic interactions between grains but not by a clustering of the dopant.

And, finally, it was shown that the magnitude of the magnetization essentially depends on the type of dopant. It turned out that the magnitude of magnetization is highest in the layers doped with Fe^{3+} ions, while in the layers doped with Co^{2+}, Mn^{2+} and Fe^{2+} ions magnetization was approximately the same for these three ions and was about two times less than in the case of doping with Fe^{3+} ions. The higher magnetization observed in ZnO layers doped with Fe^{3+} ions can be attributed to the carrier mediated mechanism of magnetization in these layers.

The fact that the ferromagnetic properties was inherent in ZnO layers doped with all magnetic impurities used and these properties were always fully reproducible showed that the method of printing developed is suitable for generating these properties. If we accept that, as it was indicated above in the Section 9.1, some peculiar features of the DMS polycrystalline structure (such as the structure of the grain boundaries, their orientation and disorientation, the specific area of grain boundaries per unit volume, etc.) does not play a minor role in the formation of ferromagnetic properties and, according to [1], even are a decisive factor for this formation, we may assume that such structural features are inherent in the printed layers studied in this work.

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Chapter 10
Time-to-digital Converters

Niansong Mei and Puqing Yang

Introduction

Time to Digital Converters (TDCs) are block circuits used to precisely quantizes the time interval between two timing events and to express the result as a digital value, which have gained more and more interest due to their increasing implementation in digital PLLs, ADCs, jitter measurements and time-of-flight (TOF) range finders. TDC have been studied since the 1970's [1], and the first integrated TDC appeared in the early nineties. The typical architecture of TDC was built based on the CMOS gate delay-line structure, this approach is quite simple but whose highest achievable resolution is limited by the intrinsic delay of a CMOS gate, the other critical issues for this structure is that resolution and dynamic range are two contractionary parameters. Some sophisticated circuit techniques to circumvent the limitation of the technology delay and enhance dynamic range will be discussed in this chapter. The main concepts are the flash TDC, the Vernier TDC, the pulse shrinking TDC, and the ADC based TDC. All concepts are explained in detail and analyzed with respect to resolution.

10.1. Flash TDC

10.1.1. Delay Line TDC

Delay line TDC uses a delay line to create uniformly distributed levels in the time domain. An implementation of the delay line TDC is shown in Fig. 10.1.

It consists of a delay-line using delay cells in the signal path and an array of flip-flops. The rising edge of the start signal is successively delayed by a series of inverter. And then each signal is connected to a D input terminal in the D flip-flop. The state of each D flip-flop is latched by the rising edge of the stop signal. A thermometer code is then generated at the D flip-flop output, which corresponds to the number of delay elements that have

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transitioned within the measurement interval [2]. The TDC output is then simply calculated as the sum of the thermometer code. The time interval t_{in} and resolution T_{LSB} can be expressed by

$$t_{in} = t_i \times \sum_{i=0}^{n=i} DU[i], \tag{10.1}$$

$$T_{LSB} = t_d, \tag{10.2}$$

where t_i is the delay time of the delay unit, t_d is the gate delay. Consequently, achieving fine resolution contradicts the goal of achieving large dynamic range, since a TDC with finer resolution would require more delay cells in order to achieve the same dynamic range. Although the flash TDC is a simple structure that can be easily integrated. However, its resolution is technology-limited by the minimum gate delay.

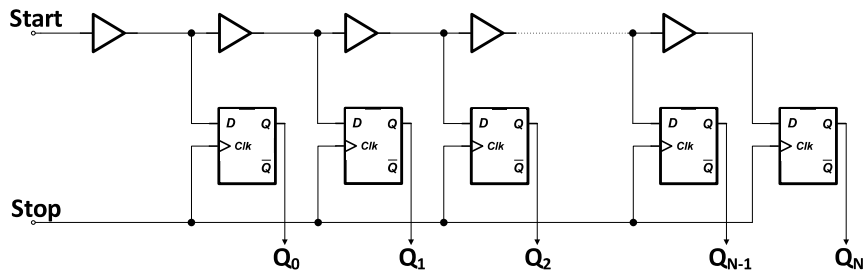

Fig. 10.1. Basic circuit diagram of flash delay line TDC.

10.1.2. Ring Delay Line TDC

The length of delay-lines (ref. Fig. 10.1) and so the area of the TDC grow with the maximum time interval to be measured. Therefore, a long-time intervals measurement means large area and high power consumption. This can be avoided by a loop configuration. Fig. 10.2 illustrates the concept of the ring delay line TDC, which connect the outputs of the last delay cells of a delay line TDC to the inputs of the first pair of delay cells. A NAND gate replaces an inverter as the first delay stage and is used to input the signals under test [2]. An odd number of delay cells is used to form the rings. The rising edge of a signal to be measured can be fed into the delay ring through one of the inputs of the NAND gate. When the start signal enters the delay-lines, the NAND gate is toggled and waits for the start event emerging at the end of the line. Therefore, the t_{in} is given by

$$\begin{aligned} t_{in} &= t_{inv}(2n \times Count) + n \times Data[n-1] + \\ &+ \sum_{i=1}^{n-1}(n-i) \times \overline{Data[\imath]\ XOR\ Data[\imath-1]}, \end{aligned} \tag{10.3}$$

Theoretically, the ring delay line TDC measurement range is only limited by the size of the output counter. However, the actual measurement range is limited by the mismatch between the transition times of the rising and the falling edges. Similar to the delay line

TDC, which highest achievable resolution is still limited by the intrinsic delay of a CMOS gate.

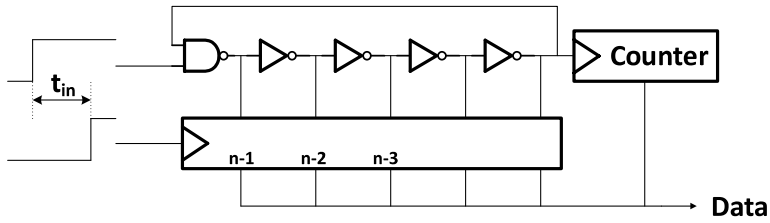

Fig. 10.2. Basic circuit diagram of ring delay line flash TDC.

10.2. Vernier TDC

10.2.1. Vernier Delay Line TDC

A Vernier TDC, shown in Fig. 10.3, overcomes the technology-limited resolution of a flash TDC, which is capable of measuring time intervals with a sub gate delay resolution [3, 4]. It employs two delay line chains with different delays: one slightly faster than the other one. The start signal propagates along the slow delay line, and fast delay line for stop signal. Thus, the stop signal chases the start signal until they become in phase. The t_{in} and T_{LSB} are defined by

$$t_{in} = \left(t_{i,slow} - t_{i,fast}\right) \times \left(\sum_{i=0}^{n=i}(n-i) \times Data[i]\ XOR\ Data[i-1]\right), \quad (10.4)$$

$$T_{LSB} = t_{i,slow} - t_{i,fast} \quad (10.5)$$

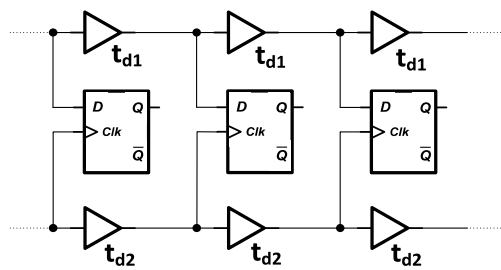

Fig. 10.3. Cut-out of Vernier delay line TDC.

The Vernier delay-line TDC's resolution does not depend on a gate delay, which only related to delay difference between the elements in the first and the second delay line. In principle this difference can be made arbitrarily small. The Vernier TDC provides a circuit technique to overcome the resolution limitations given by a certain technology. However, for an n-bit Vernier-based TDC circuit, the total number of flip-flops that are needed in

the design is (2^n-1) and the total number of required delay elements is 2(2^n-1), making it impractical in high-resolution wide-range applications. In addition, the mismatch between the delay lines severely limits the resolution in practice.

10.2.2. Vernier Ring Delay Line TDC

As discussed in Section 10.1.2, long time interval can be measured with reasonable area consumption by applying looped structures. The basic loop Vernier TDC concept is shown in Fig. 10.4. The delay-line for the start signal and the delay-line for the stop signal are both implemented in a ring delay line. A counter is applied to record the cycle times of which the start signal through the total loop until the stop signal arrives. The t_{in} can be expressed as

$$t_{in} = \left(t_{inv,slow} - t_{inv,fast}\right) \times 2n \times Count + nData[n-1] + \\ + \sum_{i=1}^{n-1}(n-i) \times Data[i] XORData[i-1], \quad (10.6)$$

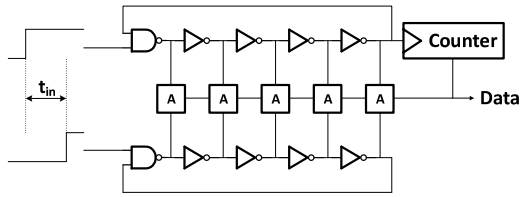

Fig. 10.4. Basic circuit diagram of loop Vernier TDC.

Just like the ring delay line TDC, the unmatched rising time and falling time leads to the duty cycle of a pulse propagating in a delay ring will either gradually increase or decrease, which eventually causes the pulse vanishing after passing a certain numbers of delay cells, limiting the achievable dynamic range of the ring TDC [5].

10.2.3. Delay-locker-loop Based TDC

In principle all concepts mentioned above can achieve an arbitrarily high resolution. In practice, however, process variations will greatly influence the performance of TDC. To overcome the process sensitive a calibration step is required before the measurement. The delay-locked-lines (DLLs) are often deployed to calibrate the process variations [6]. A DLL is adopted in a Vernier ring delay line TDC as illustrated in Fig. 10.5 [7]. The phase detector provides a signal that is proportional to the time difference between the two rising edges. As the output signal contains not only skew information but also some higher frequency components, a loop filter (low-pass filter) is required after the phase detector, and the output signal of the filter is used to control the delay of the individual delay elements. Unfortunately, this structure suffers a risk called false locking. To avoid false locking a more complex phase comparator, namely a phase-frequency detector, can be used [7]. In the Ref. [8], a 5-bit 2D Vernier TDC with delay calibration circuits was implemented, its resolution can achieve a few picoseconds.

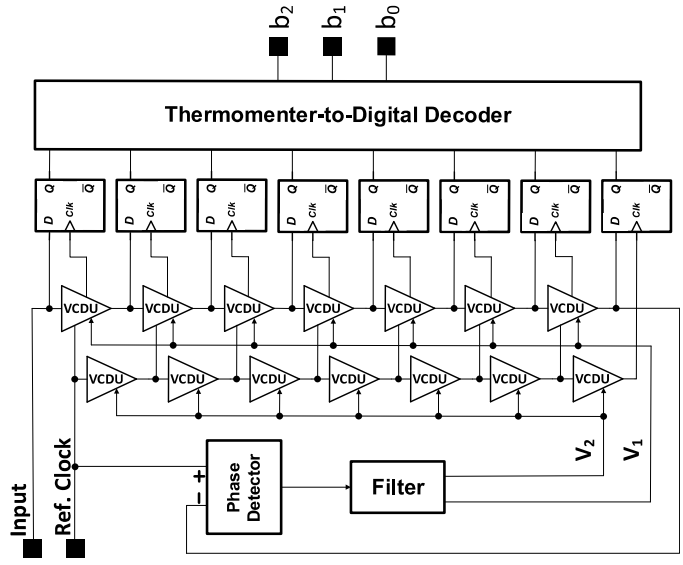

Fig. 10.5. Fine-resolution Vernier TDC adopting DLL.

10.3. Interpolation TDC

Another method to get a sub-gate delay resolution in TDC is to break an inverter delay unit into smaller units. This method also calls as time-domain interpolating [9]. For a detailed understanding the principle of time step interpolation is illustrated in Fig. 10.6.

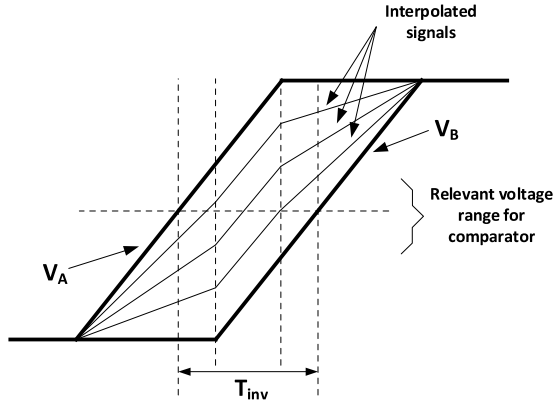

Fig. 10.6. Principle of time step interpolation.

One important precondition is that the rise time of a signal generated by a single-stage CMOS gate is in the order of the gate delay time, which ensures that the output signal is switching while the corresponding input signal has not settled yet. A new signal defined by [10]

$$V_{int,i} = V_B + \alpha_i \cdot (V_A - V_B), \tag{10.7}$$

$V_{int,i}$ lies in between the base signals, where α_i is the interpolation coefficient, which weights the two base signals and determines whether the new signal is nearer to V_A or nearer to V_B. Fig. 10.6 shows its transition in between those of the two generating signals V_A and V_B [10]. The new signal can be used to quantize the time interval between V_A and V_B.

10.3.1. Passive Interpolation TDC

Fig. 10.7 [10] shows a basic circuit diagram of a local passive interpolation TDC. The interpolation is done by resistive voltage dividers connected in between the inputs of the differential delay elements and their respective logically equivalent outputs, which goal is to create intermediate signals [11]. The results (OUT_i) can be generated by interpolator signal (R_i, F_i) connected to a dynamic comparator. For the resistance interpolation, only the ratio of two resistances is relevant, so process variations cancel out, the fine time resolution is achieved. However, the realization of high speed voltage domain comparator is a challenge. In addition, the interpolation fails when the rise-time is small than the gate delay [7].

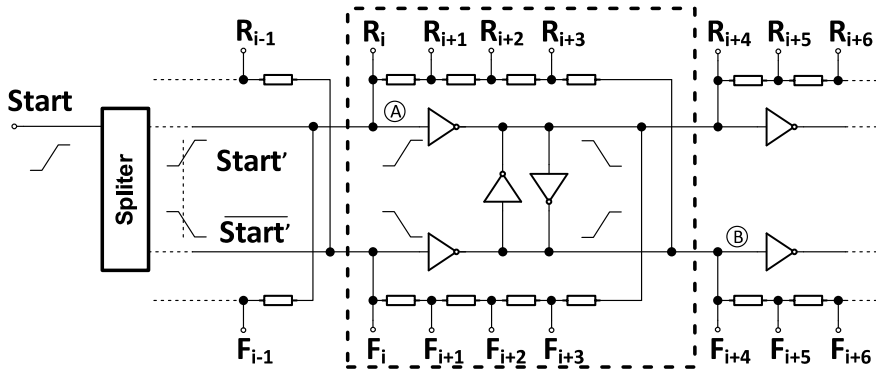

Fig. 10.7. Basic circuit diagram of local passive interpolation TDC.

10.3.2. Active Interpolation TDC

In the passive interpolating method, the voltage difference at the adjacent cell is very small, which increase the difficulty of a comparator to make a correct decision. To improve the comparison accuracy, an inverter-based interpolator [12, 13], as shown in Fig. 10.8, was proposed. The time interpolation can be realized by applying different delay of each input signal (R_i, R_{i+1}), a time comparator is applied to judge the rising edge of two interpolating signals. It is a real time-domain interpolator, compared with the resistive interpolator.

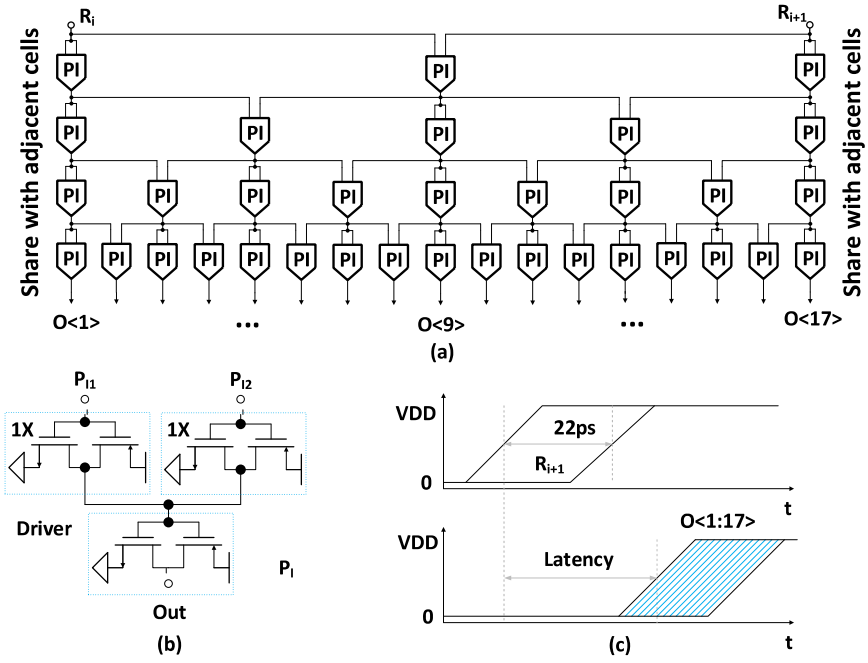

Fig. 10.8. Schematic of (a) 16× time interpolator with a four-layer architecture, and (b) unit phase interpolator cell; (c) Timing diagram of the 16× time interpolator.

10.4. Pulse-shrinking TDC

Pulse-shrinking is another relatively easy techniques to achieve sub-gate time resolution. For a detailed understanding the principle is illustrated in Fig. 10.9. When the pulse signal propagates along the delay-line it becomes smaller and smaller and vanishes completely at certain propagates point. The pulse-shrinking amount is controlled by the dimension ratio (β) between the in-homogeneity and homogeneity NOT gates. The amount of pulse width variation from stage i to stage i + 2 can be calculated according to [14]

$$\Delta W = T_{in} - T_{out} = \left(\beta - \frac{1}{\beta}\right) C_i \left(\frac{1}{k_{P_i}} - \frac{1}{k_{N_i}}\right) \times \emptyset, \tag{10.7}$$

where k_{N_i} and k_{P_i} are the transconductance parameters of the i-th NOT gate, C_i is the effective input capacitance of the i-th NOT gate, and $\phi = [(2V_{th}/((V_{DD} - V_{th})^2)) + +(1/(V_{DD} - V_{th}))ln((1.5V_{DD} - 2V_{th})/(0.5V_{DD}))]$ is a constant factor, which is not related to layout.

A basic pulse-shrinking TDC is depicted in Fig. 10.10 [15]. A register array records the rising or falling edge of each stage. The conversion result is obtained from those registers. Also, as the shrinking time is shorter, the fine time resolution can be achieved. However, the mismatch among the pulse-shrinking delay elements severely limits the TDC accuracy.

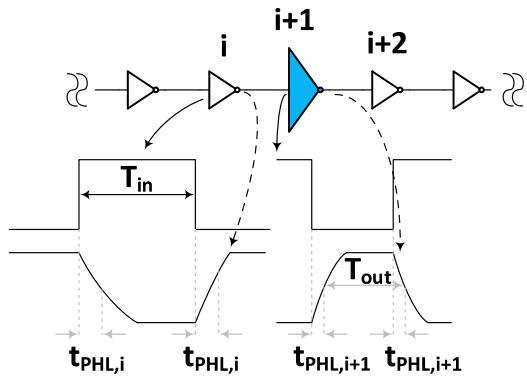

Fig. 10.9. Operating principle of the pulse-shrinking TDC.

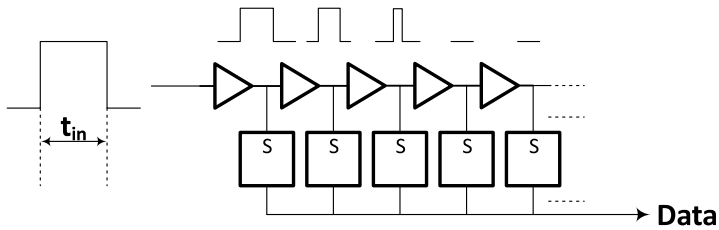

Fig. 10.10. Simplified illustration of a pulse-shrinking delay line TDC.

To reduced area consumption and better linearity the pulse-shrinking TDC also can be implemented in a ring structure as shown in Fig. 10.11 [14]. The principle is the same as for the ring delay line TDC or the Vernier ring delay line TDC. It is necessary to notice that the delay line's delay time should exceed the T_{in} when it operates properly. A critical issue for the pulse-shrinking TDC is the minimum pulse width that can be detected by the flip-flops. Before the pulse vanishes, it becomes very small and does not reach the full logic level anymore. This circuit is susceptible to PVT variations [11]. Ref. [16] propose an area-efficient CMOS TDC to achieve low thermal sensitivity by applying thermally compensated circuits. As Fig. 10.12 shows, the thermal-compensation circuit includes two current mirrors and a diode-connected transistor (M3) which can be implemented by a p-channel MOS (pMOS) or a n-channel MOS (nMOS) transistor.

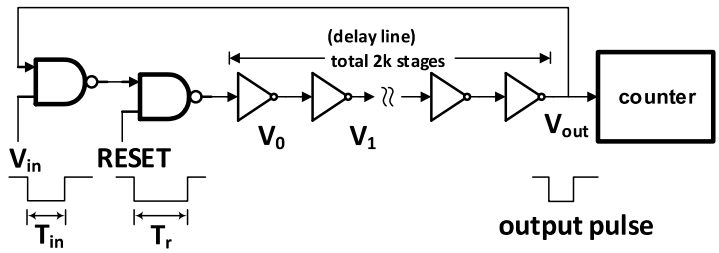

Fig. 10.11. Basic circuit diagram of pulse-shrinking TDC.

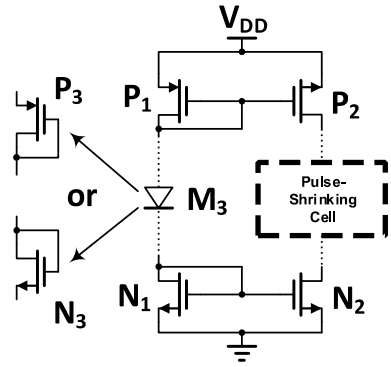

Fig. 10.12. Schematic of the thermal-compensation circuit for the pulse shrinking cell.

10.5. Pipeline TDC

Unlike all TDCs discussed so far that achieve higher resolution by creating narrower time intervals. The pipeline TDC cascade several low-resolution stages to obtain high overall resolution. Each stage performs coarse T/D conversion and computes its quantization error, or "residue". An error amplifier needs to be inserted between stages to amplify the quantization residual error of the previous stage. Fig. 10.13 shows a two-stage pipeline TDC, the coarse flash TDC acts as the first stage and generates the digital output D_{out1}. An inter-stage time interval amplifier generates residual quantization error which is then quantized by the second flash TDC to produce the fine output code D_{out2} [17]. The final TDC output is generated according to the weight of D_{out1} and D_{out2}. This method can effectively improve the resolution without increasing the number of delay elements.

A typical time interval amplifier is depicted in Fig. 10.14 [11]. It consists of a conventional NAND latch followed by an arbiter. Before taking a measurement, both input signals A and B are low. Thus, both of arbiter's output are low. On the arrival of a rising edge on, the latch locks the signal whatever switching activity occurs at the other input. The arbiter evaluates which latch output goes low (first) and sets the appropriate output to high.

However, this technique suffers from gain uncertainty due to the local PVT variations, which makes it difficult to operate linearly [11]. Therefore, calibration techniques is required to achieve higher resolution.

10.6. Successive Approximation TDC

In successive approximation ADC, the binary search and successive approximation method are applied to the converter to get the binary output quickly. The successive approximation TDC (SAR TDC) is similar to it. Theoretically, SAR TDC is more energy-saving and more resolution than flash TDC.

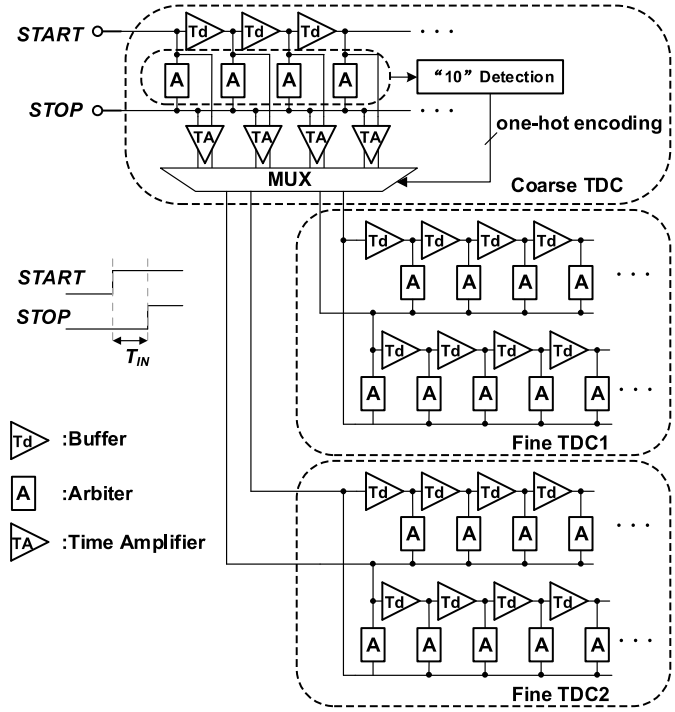

Fig. 10.13. Basic circuit diagram of pipeline TDC.

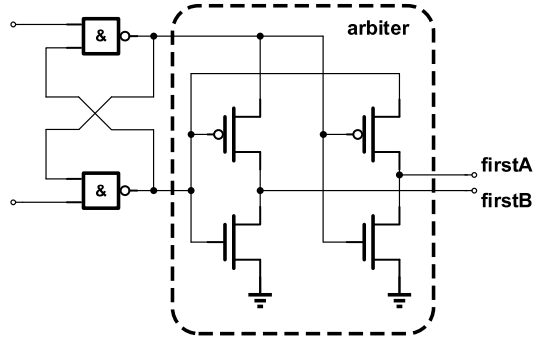

Fig. 10.14. Basic principle of time interval amplifier (TA).

10.6.1. Typical SAR TDC

Fig. 10.15 [18] shows a typical SAR TDC architecture. It consists of double digital-to-time converters (DTC), a 1-bit time-to-digital converter (TDC), a control logic, a shift register, and some multiplexes. When the start signal is applied to TDC, the start signal is added a long delay ($T_{FD}/2$), and the stop signal directed get through DTC without delay. The 1-bit TDC compares the rising edge of the delayed start signal with the stop signal. If the rising edge of the delayed start signal is ahead of the stop signal, a delay time ($T_{FD}/4$)

will be added to the delayed start signal. If not, it will be applied to the stop signal. Those process would not stop until the last bit delay ($T_{FD}/2^N$) apply to it.

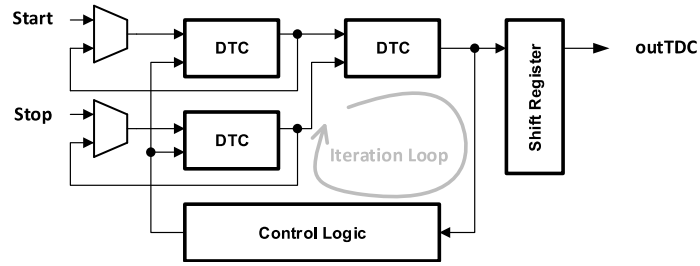

Fig. 10.15. Basic block diagram of SAR TDC.

Since the delay of DTC, control logic, and MUX cannot be negligible, inserting a programmable binary weighted delay and associated control logic to compensate the above delay is needed. As a result, the TDC conversion speed becomes slower and the energy saving effect becomes worse.

10.6.2. Decision-select Structure

Fig. 10.16 illustrates a SAR TDC based on decision-select structure [19], which can effectively reduce the delay of control logic and multiplexer. In this structure, each stage of 1-bit TDC needs to decide which one path should apply a delay (TF S/2). Because the control logic is simplified, the delay is reduced effectively. In addition, co-design of the time arbiter and control logic can significantly improve the operation speed of TDC. Its operation principle is shown in Fig. 10.17. With this property, a 6 bit 1.2 GS/s symmetric SAR TDC has been proposed [20]. It adopts a symmetrical structure and can measure the time difference between start and stop signals without distinguishing the start and stop signal.

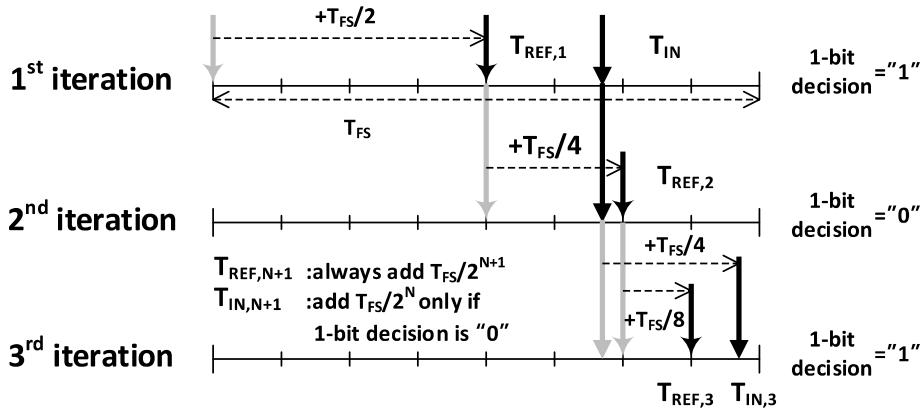

Fig. 10.16. Schematic of decision-select structure SAR TDC.

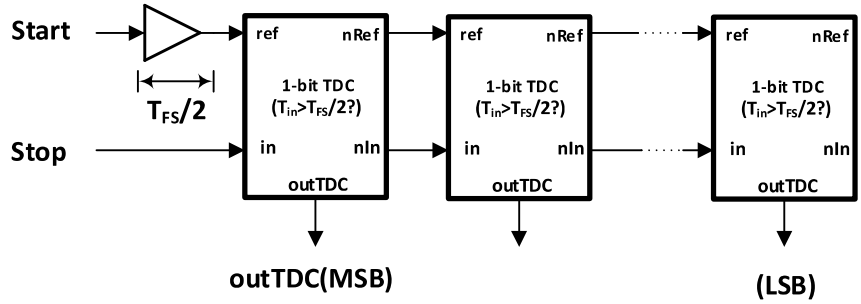

Fig. 10.17. Operational principle of decision-selected structure SA-TDC.

10.7. ΔΣ TDC

The evolution of TDCs has followed a similar path to that of ADCs. We have described several kinds of Nyquist-rate TDC in previously section, they have high speed and medium precision. To further improve the time resolution, oversampling based TDC has been proposed. The structure performs an operation analogous to ADCs by noise shaping the quantization noise of the TDC, such noise shaping yields greatly improved effective resolution of the TDC time-to-digital mapping characteristic.

Fig. 10.18 shows a basic conception of delta-sigma TDC. It consists of signal transfer path and noise transfer loop. $L_0(z)$ is applied to signal path since the input signal (*tin[n]*) is always a discrete signal. However, the feedback signal could be continuous (s) or discrete (z). Moreover, the types of feedback signals can be various, such as time, voltage, current and so on.

For a delta sigma TDC, integrator is an essential circuit unit. Three types of integrators are commonly used according to recent research: time-to-voltage integrator, time-domain integrator, and phase-domain integrator. These integrators are used in the input stage for noise shaping.

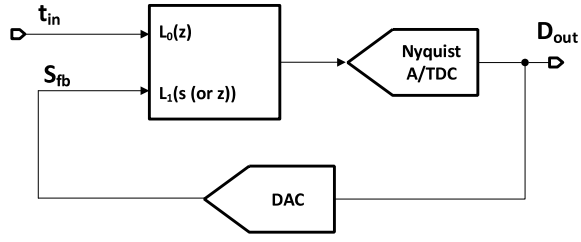

Fig. 10.18. Basic connection of ΔΣ TDC.

The feedback path is also important for a ΔΣ modulation loop. The DAC output signal is usually a voltage domain signal. Therefore, it is inevitable to design a voltage-to-time converter to give a proper feedback signal if we used a time subtractors in the input stage TDC. And, similar to the multi-bit, high-order, and MASH ΔΣ modulator, these architectures can also be applied to TDC.

10.7.1. Time-to-voltage Integrator

A time-to-voltage integrator can converter a time-domain signal into a voltage-domain signal and realize integrator in time domain. It usually can be realized by combining a switch and a capacitor [21], shown in Fig. 10.19 (a). The capacitor is charged when the switch is turned on. The output voltage V_{out} is given by

$$V_{out}[n] = V_{out}[n-1] + (V_{DD} - V_{out}[n-1])\left(1 - e^{-\frac{t_{in}[n]}{RC}}\right), \tag{10.8}$$

where V_{DD} is the supply voltage, $t_{in}[n]$ is the input time signal. Usually, $RC \gg t_{in}[n]$,

$$V_{out}[n] \simeq V_{out}[n-1] + \frac{V_{DD}}{RC}\, t_{in}[n] \tag{10.9}$$

In z-domain, formula (10.9) can be expressed as

$$V_{out}(z) = \frac{V_{DD}}{RC}\frac{1}{1-z^{-1}} T_{in}(z) \tag{10.10}$$

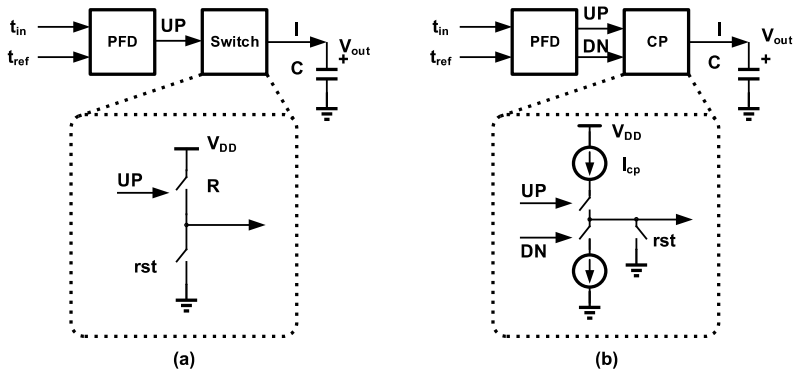

Fig. 10.19. Block diagram of (a) switch-based, and (b) CP-based time-to-voltage integrator.

When $RC \gg t_{in}[n]$, the relationship between input and output signals can be approximately linear. In the ΔΣ modulation loop, a linear system is easier to be analyzed than a nonlinear system. As Fig. 10.19(b) illustrate, a charge pump is often used as a time to voltage signal converter as well, the output voltage of the charge pump is expressed as

$$V_{out}[n] = I_{CP} \times C \times t_{in}[n] + V_{out}[n-1] \tag{10.11}$$

In z-domain, it is given by

$$V_{out}(z) = I_{CP} \times C \times \frac{1}{1-z^{-1}} T_{in}(z), \tag{10.12}$$

where I_{CP} is the bias current of charge pump.

10.7.2. Time-domain Integrator

A time-domain (TD) integrator can be realized time accumulation in time-domain. It is compromised of a TD-adder and TD-register, as shown in Fig. 10.20 [22]. The TD adder can be constructed simply by OR gate. The function of TD register is to save the time information of the last phase and output the time signal *Tout*. As the Fig. 10.20 shows, which consists of a time-to-voltage converter, a delay cell, and a voltage-to-time converter. The transfer function in Z domain of TD register is given by

$$T_{out}(z) = T_{in}(z) + T_{out}(z)^{z-1}, \tag{10.13}$$

$$T_{out}(z) = \frac{1}{1-z^{-1}} T_{in}(z) \tag{10.14}$$

A switched-RC circuit can be used to realize a TD-register, as shown in Fig. 10.21.

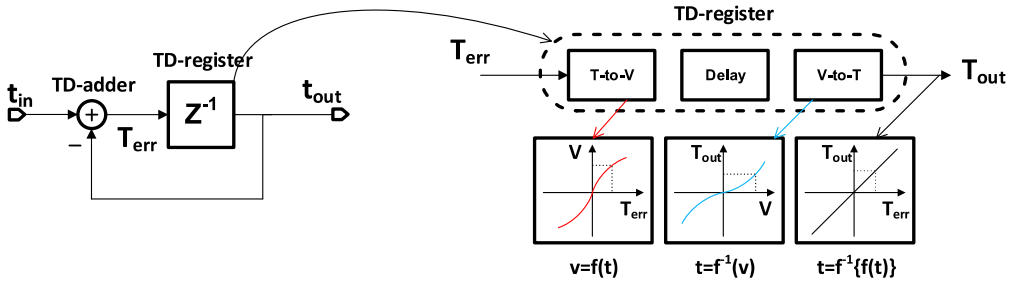

Fig. 10.20. Architecture of a TD-integrator.

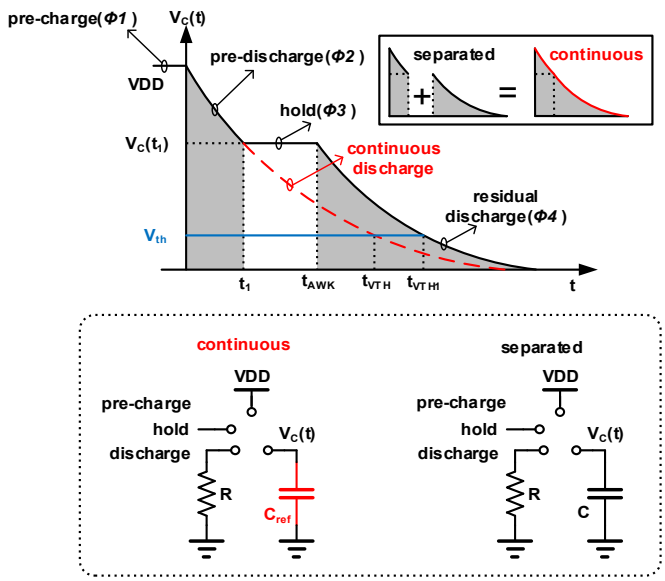

Fig. 10.21. Operation principle of a TD-register constructed by a switched-RC circuit.

The basic concept is to convert the input time signal into an intermediate voltage/charge and hold this voltage for a proper delay, then retrieve the time signal from the voltage. Fig. 10.21 illustrate the operation principle of the switched-RC circuit. In the pre-charge phase (φ_1), two identical capacitors (C_{ref}, C) are pre-charged to a fixed voltage (VDD). In the pre-discharge phase (φ_2), the capacitor connects a dis-charge path (R), and wait for input time signal. In phase (φ_3), one of capacitor (C_{ref}) hold the voltage, and the other capacitor (C) remains discharges. So far, the input time information is stored in the capacitor in the form of voltage difference. In the residual discharge phase (φ_4), two capacitors continue to discharge.

10.7.3. Phase-domain Integrator

We have known that a ring oscillator can be expressed as K_{RO}/s in the frequency domain and is often used as integrator. Similarly, a gate ring oscillator (GRO) also can be used an integrator in the TDC. To gain a better understanding of the principle of GRO-based integrator, Fig 10.22 shows a schematic of a GRO implemented with transistors. The ring oscillator is gated with an enable signal. When the switches are closed, oscillation is enabled and the circuits work as a classical ring oscillator. Conversely, when the switches are opened, the inverter is suspended, and each out node of the inverter is in a high impedance state. As a result, the status at each inverter output note is frozen and keep until the next enable signal. Thus, it allows to benefit from first-order noise shaping and to keep the residue of the last step transfer to the next one [23]. If the duration of the enabled RO is t_{in}, the radian frequency of RO is ω, and the initial phase is ψ_0, the output of phase ψ_1 can be given by

$$\psi_1 = \omega t_{in} + \psi_0 \tag{10.15}$$

After the n'th enable of the RO, the output of phase ψ[n] is given by

$$\psi[n] = \omega t_{in}[n] + \psi[n-1] \tag{10.16}$$

Therefore, we get an integrator in the discrete-time domain. Using the unilateral z-transform, we have

$$\Psi(z) = \frac{\omega}{1-z^{-1}} T_{in}(z), \tag{10.17}$$

wshere $T_{in}(z)$ is the z-transform of the input signal $t_{in}[n]$. As a result, we get a integrator in the z-domain. If a differential cell $(1-z^{-1})$ apply to the output, a GRO TDC can be achieved. The main disadvantage of GRO is that the non idealization of switches, parasitic capacitors and resistors will lead to charge leakage and charge injection in suspend state, which resulting in phase error. Fortunately, we can suppress the charge leakage effect by improving the circuit [24, 22]. Fig. 10.23 displays a conceptual implementation of a switched ring oscillator which is switched between two frequency ω_L and ω_H instead of gating the oscillator [22]. Similarly to GRO integrator, the SRO integrator transfer function in z-domain can be expressed as

$$\Psi(z) = \frac{\omega_H - \omega_L}{1-z^{-1}} T_{in}(z) \tag{10.18}$$

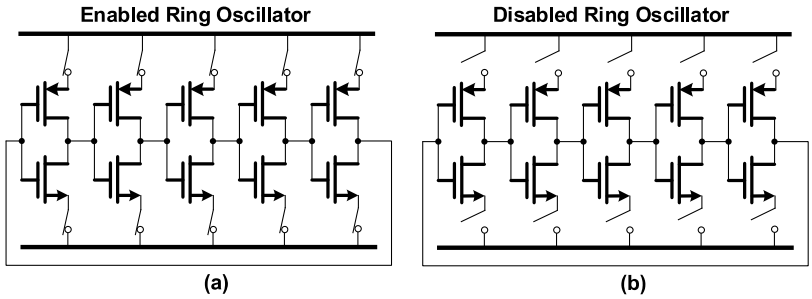

Fig. 10.22. Schematic of a GRO.

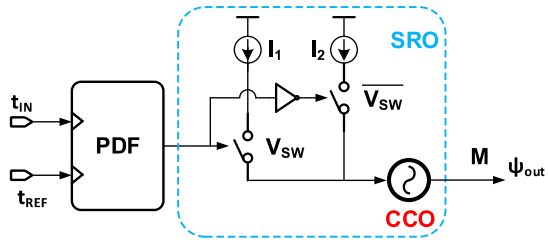

Fig. 10.23. Block diagram of a SRO.

10.7.4. Voltage-to-time Converter

Generally, a voltage-to-time converter (VTC) is a black box with an input node of voltage and an output node of time, the mathematical formula expressed as $T = f(V)$. More importantly, we need to use some specific parameters to represent the output value of time. One way is to use the edge (rising or falling) interval of two signals to represent the output time signal. In another way is to use a pulse duration or period to represent a time signal. The difference between the two methods is that one is a one-time method that requires an initial state or sampling operation, and the other is a cyclical method that the pulse duration or period varies with the voltage.

10.7.4.1. One-time Method

10.7.4.1.1. Comparator Based

If a capacitor is connected to a direct current source, the relationship among storage charge (Q), charging current (I), voltage (V), capacitor (C) and charging time (t) can be expressed by the following formula

$$Q = VC = It \Rightarrow t = \frac{VC}{I} \tag{10.19}$$

For Fig. 10.24, according formula (10.19), the time which is between the "start" and "stop" signal can be expressed as

$$t = \frac{(V_{in}-V_{cm})C}{I}, \quad (10.20)$$

where V_{cm} and V_{in} are shown in Fig. 10.24.

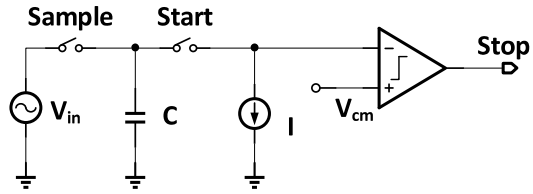

Fig. 10.24. Schematic of sampling V_{in} VTC.

By exchanging the position of V_{cm} and V_{in}, a threshold voltage controlled VTC is obtained as shown in Fig. 10.25. The input voltage is compared with a sawtooth-shaped waveform to realize time-to-digital conversion.

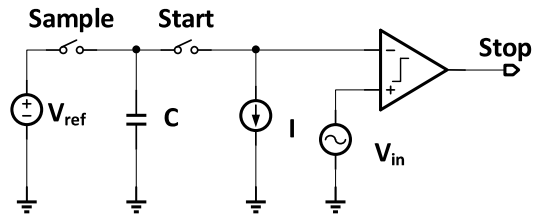

Fig. 10.25. Schematic of threshold-voltage controlled VTC.

In some cases, we want to achieve a wide measurement range by sacrificing a system's linearity. Fig. 10.26 shows a wide measurement range VTC circuit diagram, which uses voltage controlled current source to replace current source. The time which is between the "start" and "stop" signal can be expressed as can be described as

$$t = \frac{(V_{ref}-V_{cm})}{g_m V_{in}} \quad (10.21)$$

The g_m cell usually is constructed by a MOSFET or an integrator circuit.

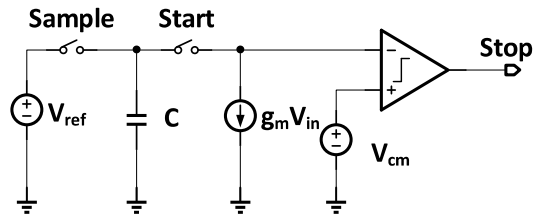

Fig. 10.26. Schematic of current controlled VTC.

10.7.4.1.2. Delay-unit Based

A simply delay-unit is comprised of an inverter and a capacitor in Fig. 10.27. The delay time is approximately

$$t = \frac{0.69}{2}\left(R_{eq,nmos} + R_{eq,pmos}\right) \cdot C, \tag{10.22}$$

$$R_{eq} = \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{7}{9}\lambda V_{DD}\right), \tag{10.23}$$

where

$$I_{DSAT} = k'\frac{W}{L}\left((V_{DD} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right) \tag{10.24}$$

Hence, we can apply the input signal to VDD or capacitor to control the delay time.

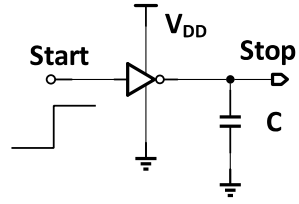

Fig. 10.27. Schematic of a simple delay-unit.

10.7.4.2. Cyclical Method

In the cyclical method, the input signal is constantly connected to the system. The frequency or pulse width of the output signal varies with the input voltage as shown in Fig. 10.28.

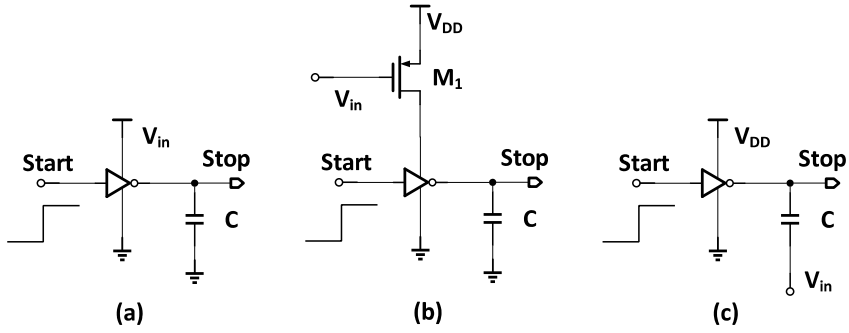

Fig. 10.28. Three control methods of delay time: (a) Voltage, (b) Current, (c) Capacitor.

10.7.4.2.1. Relaxation Oscillator Based

Fig. 10.29 shows the block diagram of relaxation oscillator. Suppose the output node *"P"* is low at the beginning of the oscillation and capacitor C is charged by the current I_2. When V_x becomes higher than the positive trip point V_{th+}, the comparator toggles and output P becomes high. Then capacitor C is discharged by the current I_1. An oscillation period is completed, while V_x becomes lower than the negative trip point V_{th-} and the output node *"P"* is low again. The output node *"P"* of comparator will generate the output voltage with desired output frequency. The period of this wave is

$$T = \frac{(V_{th+}-V_{th-})\cdot C}{g_m V_{in}} + \frac{(V_{th+}-V_{th-})\cdot C}{g_m V_{ref}} + 2t_{d,sch}, \tag{10.25}$$

$$T_{P=1} = \frac{(V_{th+}-V_{th-})\cdot C}{g_m V_{in}} + t_{d,sch} \tag{10.26}$$

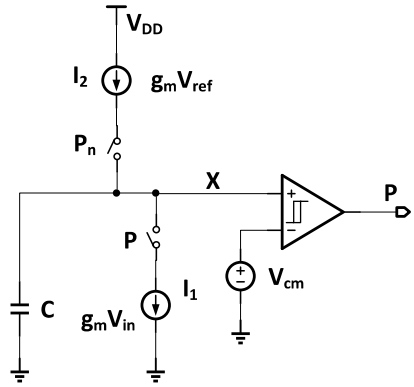

Fig. 10.29. Relaxation oscillator based VTC.

10.7.4.2.2. Ring Oscillator Based

As Fig. 10.30 shows, we can use an inverter-based voltage-controlled oscillator to converter voltage into frequency. The period of the VCO is

$$T = 10 \times t_{d,inv}, \tag{10.27}$$

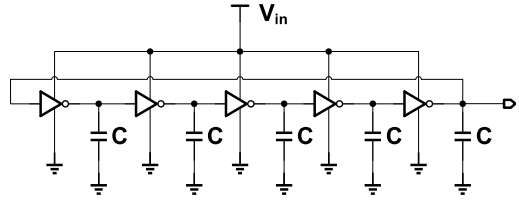

Fig. 10.30. Ring oscillator based VTC.

10.7.5. First-order ΔΣ TDC

10.7.5.1. Time-to-voltage Integrator Based

Fig. 10.31 shows a first-order single-bit ΔΣ TDC based on the time-to-voltage integrator [25]. The input signal is $t_{in}[n]$. φ_1 and φ_2 are two feedback timing signals, which is similar to V_{refn} and V_{refp} in the single-bit ΔΣ ADC. A PFD regard as a time subtractor to generate a pulse which is applied to CP to realize an integrator. The output voltage ($V_{C,TDC}$) control the delay time of the voltage-control-delay-line (VCDL). Assuming the delay time of VCDL is t_{VCDL}, the set-up time of the DFF is $t_{set-up,DFF}$, the inverter's delay is $t_{d,inv}$, and the pulse width of φ_{ref} is t_{ref}.If $t_{ref} + t_{d,inv} > t_{VCDL} + + t_{set-up,DFF}$, DFF output high level. Otherwise, DFF output low level.

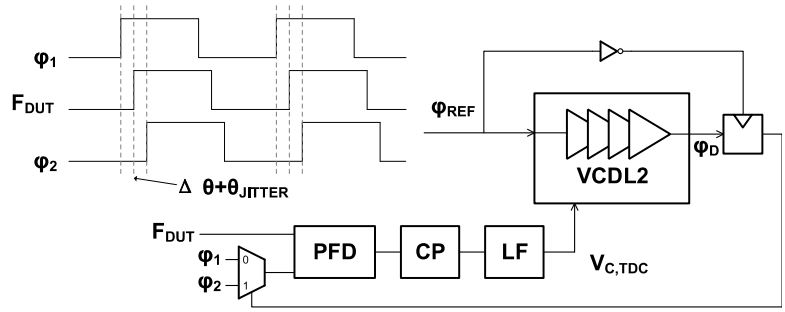

Fig. 10.31. First-order single-bit ΔΣ architecture based on the time-to-voltage integrator and timing diagram.

The φ_{ref} is the reference time signal, which can be used to generate two reference signal ($\varphi_1 = \varphi_{ref} - \Delta\theta$ and $\varphi_2 = \varphi_{ref} + \Delta\theta$), as shown in Fig. 10.32. A pseudo-DLL is designed for generating a controllable $\Delta\theta$ to extend dynamic range of TDC and get a stable reference signal (φ_1 and φ_2). During pre-charge, V_C is pre-charged by current I_{PC} for a duration time of T_{ref}. In $\Delta\theta$-discharge phase, the PFD detect the phase difference $\varphi_2 - \varphi_1 = 2\Delta\theta$ and open $I_{CPDLL} = kI_{CP}$ to discharge the voltage (V_C). Next, S/H sampling V_C and apply it to VCDL to control the phase difference. When the loop is in the stable state, the phase difference ($2\Delta\theta$) is given by

$$2\Delta\theta = \frac{1}{k} \times T_{ref} \tag{10.28}$$

10.7.5.2. Time-domain Integrator Based

Similar to first-order ΔΣ modulator, a first-order time-domain ΔΣ TDC has two feedback models: output-feedback and error-feedback, as shown in Fig. 10.33 [22]. In each model, the quantizer can be realized by a sub TDC and a digital to time converter (DTC). In this structure, signal and quantization noise transfer functions, output feedback and error

feedback functions are the same respectively. The system transfer function is expressed as

$$D_{out}(z) = T_{in}(z) \cdot z^{-1} + E(z) \cdot (1 - z^{-1}) \tag{10.29}$$

where $D_{out}(z)$ and $T_{in}(z)$ are the output and input of the ΔΣ TDC, respectively, in z-domain. $E(z)$ stands for the quantization error. Since it is easy to implement a DTC with time domain subtraction function at the circuit level, the error feedback TDC is preferred. As Fig. 10.34 shows [22], the digitalized output can be got from the sub-TDC which is constructed by two DFF and two t_d delay cell, and the error-feedback signal is generated by the sub-DTC circuit, in which two $2t_d$-cell and MUX realize a subtractor. If $\Delta T > t_d$, the output are D0 = 0 and D1 = 1. Next, the digital signal would apply to sub-DTC, and the error feedback signal is $Q_{err} = \Delta T - 2t_d$. The input signal is limited within $[-2t_d, 2t_d]$. The state function is given by

$$E[n] = Y[n] \cdot 2t_d - \Delta T[n], \tag{10.30}$$

$$\Delta T[n] = t_{in}[n-1] - E[n-1], \tag{10.31}$$

and $Y[n]$ is given by

$$Y[n]\begin{cases} -1 \ \Delta T \in [-3t_d, -t_d) \\ 0 \ \Delta T \in [-t_d, t_d) \\ 1 \ \Delta T \in [t_d, 3t_d) \end{cases}, \tag{10.32}$$

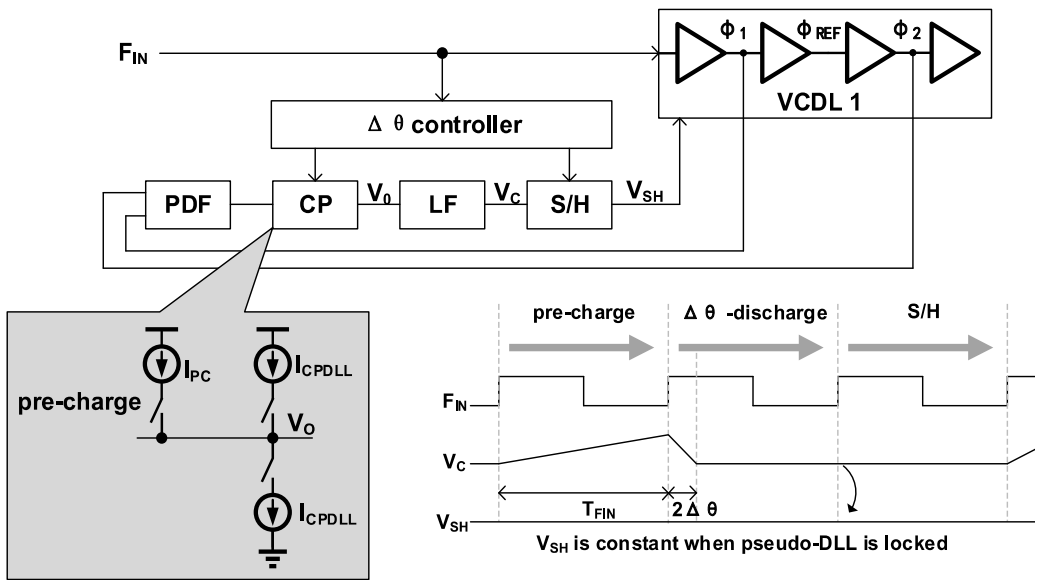

Fig. 10.32. ϕ_1 and ϕ_2 generation schematic and timing diagram.

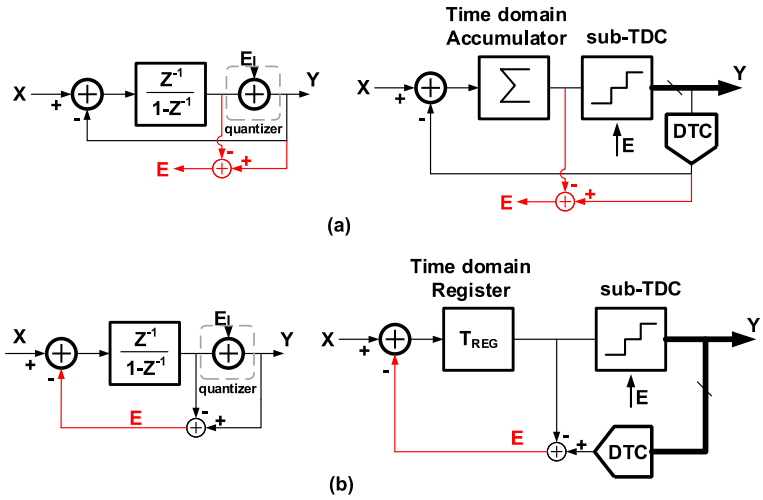

Fig. 10.33. Model of (a) output-feedback, (b) error-feedback TDC.

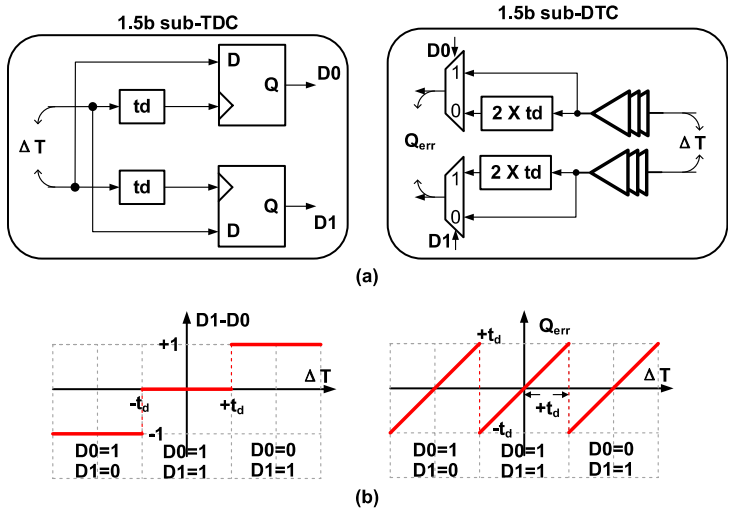

Fig. 10.34. (a) Architecture of 1.5-bit sub-TDC and sub-DTC. (b) Transfer function of 1.5-bit sub-TDC and sub-DTC.

10.7.5.3. Phase-domain Integrator Based

Fig. 10.35 shows a SRO-TDC, it is comprised of a phase domain integrator, a quantizer and a differential unit $(1-z^{-1})$ which is constructed by two groups of DFF and a group of XOR gate. From Eq. (10.18), the system state function is expressed as

$$D_{out}[n] = \alpha(\theta[n] - \theta[n-1]), \tag{10.33}$$

$$\theta[n] = \psi[n] + E[n], \tag{10.34}$$

The first-order noise shaping operation property is given by

$$D_{out}[n] = \alpha \cdot \left((\omega_H - \omega_L) \cdot t_{in}[n] + \underbrace{E[n] - E[n-1]}_{first-order\ noise-shaping} \right), \tag{10.35}$$

where $E_{[n]}$ is the quantization noise, and α is the correlation coefficient between the digital output and the phase oscillator.

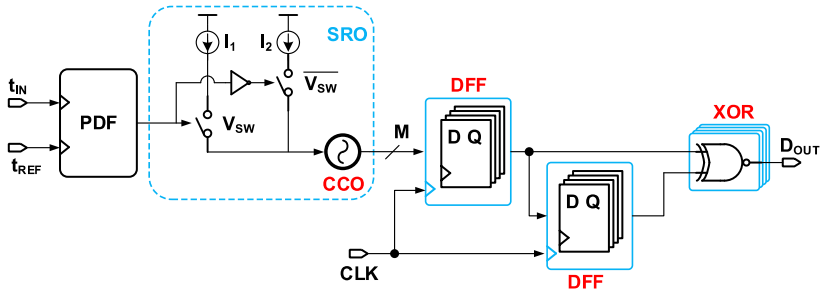

Fig. 10.35. Schematic of a SRO-based TDC.

10.7.6. High Order ΔΣ TDC

Similar to design of ADCs, the noise-shaping concept can also be extended to higher orders. For modulators, there are two ways to realize high-order noise-shaping: single-loop and MASH. Compared with the time-domain TDC, it is easier to realize the high order modulator in voltage domain. Fig. 10.36 shows a second order TDC with sub-ps resolution [26]. The architecture is composed of a time-to-voltage converter and an integrator in the voltage-domain to realize second order filter in the loop. The feedback digital signal with a multiplexer is to select a signal with different delay which would input to phase detector to realize "Δ" operation.

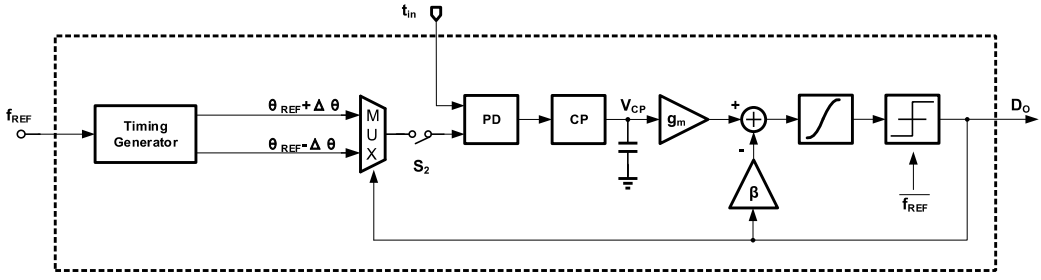

Fig. 10.36. Block diagram of ΔΣ TDC.

Also, we can apply phase-domain integrator and time-domain integrator to a third-order ΔΣ TDC in Fig. 10.37 [27]. It consists of a OR-gate based adder, a GRO, a counter to

quantize output phase, a differentiator to realize first order noise shaping, a QEGen to generate quantization error, and a time-domain error filter to realize second-order noise shaping. As shown in Fig. 10.38, the signal transfer function (STF) is given by

$$STF = \frac{\omega}{1-z^{-1}} \times \alpha(1-z^{-1}) = \omega\alpha \tag{10.36}$$

where ω is the operation radian frequency of the GRO, α is the quantization coefficient of the counter. Similarly, the noise transfer function (NTF) is given by

$$NTF = \left(Q(z) - Q(z)z^{-1} \times H_{EF}(z) \times \frac{\omega}{1-z^{-1}}\right) \times \alpha(1-z^{-1}), \tag{10.37}$$

where *Q(z)* the quantization phase error, H_{EF} *(z)* is the transfer function of the time-domain EF filter in z-domain. The third-order noise-shaping NTF have a form of $(1\ z-1)^3$. If ω = 1, the transfer function of the EF filter is

$$H_{EF}(z) = (1-z^{-1}) \times (2-z^{-1}) \tag{10.38}$$

As shown in Fig. 10.39, the time-domain EF filter can be constructed by time-domain register (TR), time-domain amplifier (TA), and logic gates.

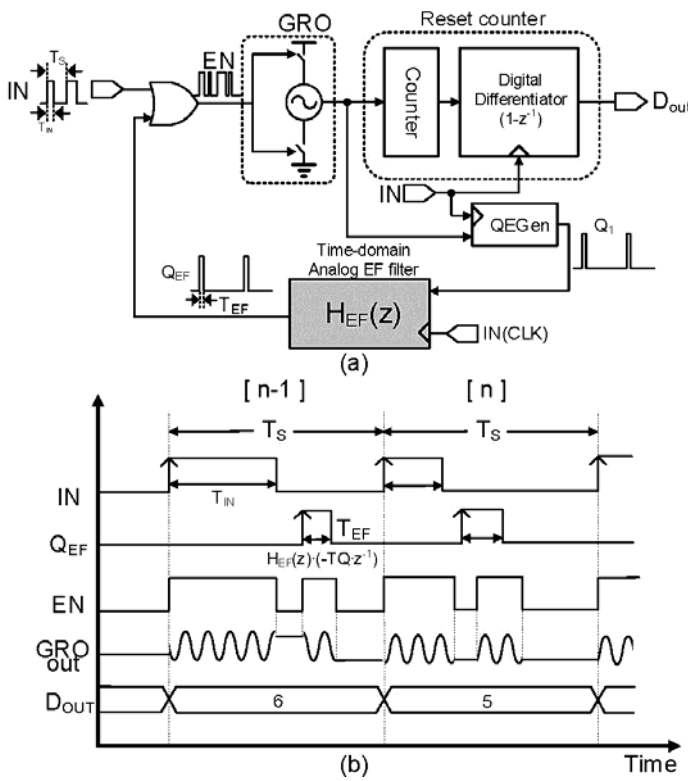

Fig. 10.37. (a) Block and (b) Timing diagram of the third-order ΔΣ TDC.

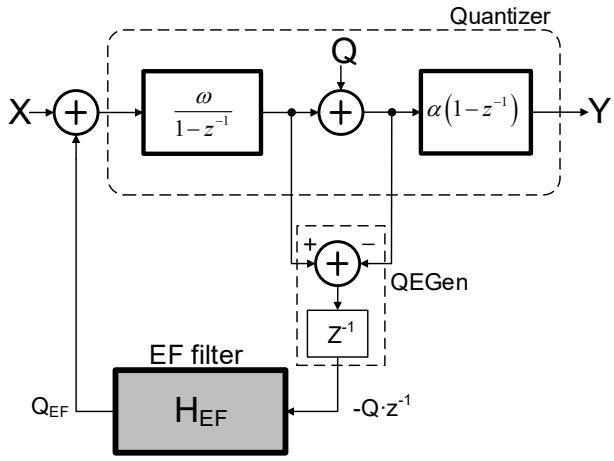

Fig. 10.38. Block diagram of the third-order ΔΣ TDC architecture.

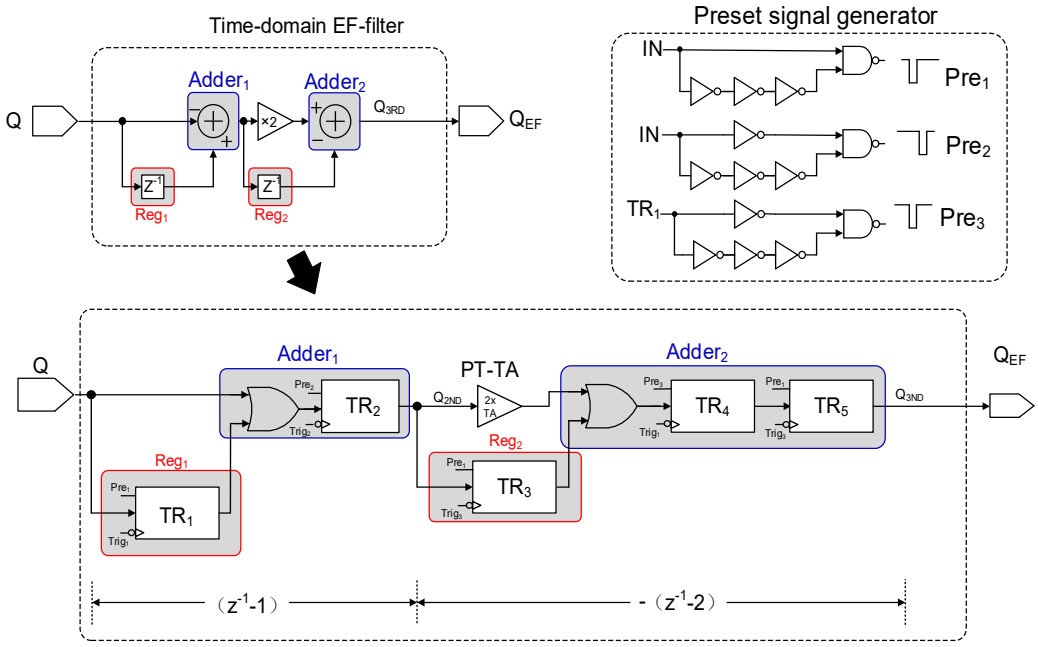

Fig. 10.39. Block diagram of the EF-filter.

10.8. Conclusions

TDCs is an attractive technology in precise time-interval measurement system. This chapter provides a review and explore of the mainly used fully digital TDC architectures including state-of-art TDC architecture. In addition, the key technologies of TDC are classified in order to compare and study the TDCs. Flash TDCs provide a high speed and poor resolution. In contract, ΔΣ TDC offers a fine resolution, but its speed is relatively

slow. The research of ΔΣ TDC is becoming a hotspot, especially the STRO-based structure. In summary, the appropriate TDC architecture can be adopted according to the actual application requirements.

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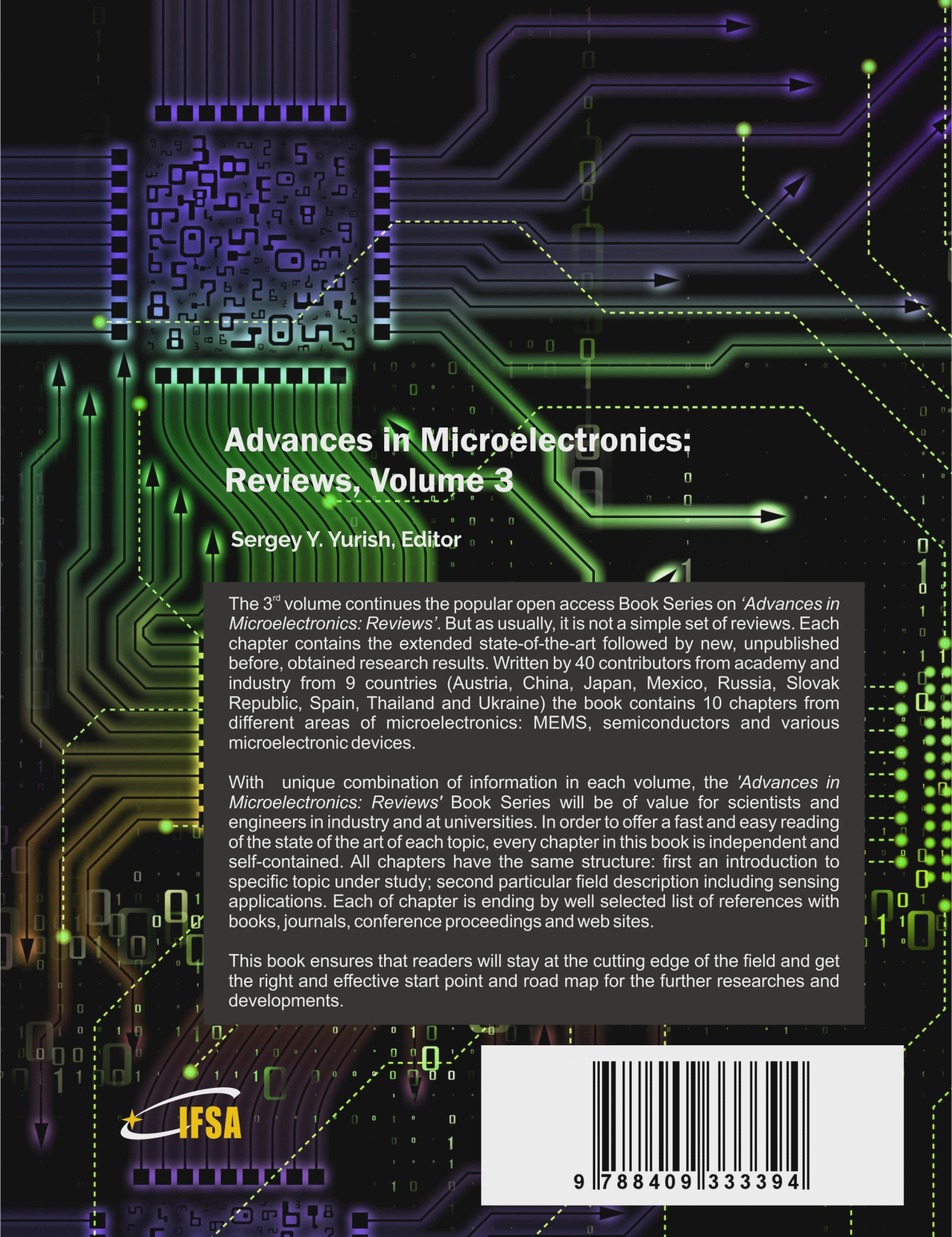

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