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Fault-Tolerant Algorithm Based on Decoupled Space-Vector for Dual Three-Level Inverter-Fed Induction Motor Drive

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Abstract: The dual inverter topology has the advantages of higher output voltage; more output levels and well tolerance performance. In this paper, a five-level SVPWM method with fault-tolerant control was proposed for dual three-level Inverter-fed Induction motor drive. In order to meets system requirement, decoupling space-vector ideological is used. A simplified algorithm is suggested to calculate the corresponding switching times, which only use the three-phase voltages and switching period. Also this scheme does not employ any look-up table, thus obviating the need for the sector identification. In order to improve the harmonic characteristics of output voltage and current, the balance control factor was regulated properly. The simulation and experimental results show that by using the proposed method, the fault-tolerant requirement can be met, running time of program reduced and the harmonics performance of output voltage and current improved effectively. *Copyright © 2013 IFSA.*

Keywords: Open-end winding induction motor, Dual inverter-fed topology, Fault-tolerant algorithm, Simplified algorithm, Quasi circular locus.

1. Introduction

High-voltage power inverter with its excellent performance and good energy saving effect, which has been rapidly promoted and applied in the fans, pumps and other industrial fields. In recent years, the development of high-voltage frequency conversion technology is seriously restricted by the withstanding voltage rating of switching device [1, 2]. For getting higher output voltage at the existing withstanding voltage rating basis of switching device, some scholars have proposed a dual inverter topology based on open winding motor. The topology open the motor stator winding asynchronously, winding at both ends is supplied by two sets of inverter power simultaneously [1-4].

Compared with single-ended power supply system, dual inverter power supply system output higher voltage, can provide more numbers of phase voltage levels, and can be made proportional to the switching frequency of the switching losses reduced significantly, and there is no voltage-sharing problem of traditional switch devices in series way [4-11]. With double three-level inverter speed control system as an example, the system can use the inverter switching devices of 4.5 kV withstanding voltage rating to achieve the rated 6 kV output voltage, output can maximize 17 level, compared with single-

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inverter systems up to the motor winding is equivalent to switching frequency is doubled; DC bus voltage ±2.5 kV, amplitude voltage jumps Udc/2 ≤ 2.5 kV, identical with 3 kV voltage three-level inverter. At present, foreign scholars have topology structure of dual inverter power supply in-depth study, and the domestic research is less.

Dual inverter topology, the motor terminal voltage is equivalent to two inverter voltage synthesis results respectively, while motor stator winding opens, motor midpoint no longer exists in the traditional sense, the definition of common-mode voltage has changed, need to be mathematical analysis. According to different bus structure, the Dual inverter-fed topology can be divided into two forms as total bus structure and independent bus structure [4], as shown in Fig. 1. Compared with common bus structure, a set of multi-bus equipment is less than independent bus structure, the higher the cost, control is more complex, but due to its rectifier parts isolated from each other, can effectively solve the circulation problems caused by the common mode voltage (4, 8-11), and has good fault tolerance features. When the system in which one of the inverter or rectifier failure occurs, the part can be quickly removed from the system, then the system into a single-ended power supply form, depending on the load conditions can still be full or half-speed heavy load, especially suitable for the coal mine blower, hoist and other high-power high-reliability applications.

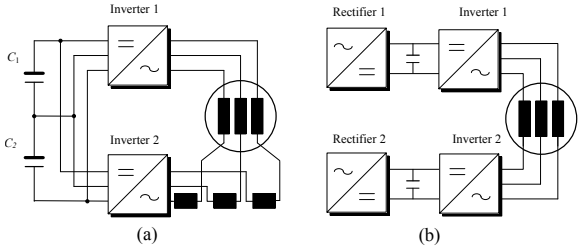


Fig. 1. Schematic of the open-end winding induction motor drive system fed by two inverters: (a) two identical inverters with common DC link, (b) two identical inverters isolated DC link.

Algorithm for fault-tolerant control requires applying to both dual inverter power supply state and single inverter power supply state condition. Dual Inverter SVPWM modulation algorithm is more to use integral control. These methods based on space voltage vector after synthesis of motor end as an object modulating, since the first vector and its redundant vector corresponding to two inverter output voltage vector may not be symmetric positive and negative small vector, so if the both ends using NPC three-level inverter will be very difficult to achieve the midpoint potential balance control, and the single inverter cannot be used when working state. At present, there are few literatures on fault-tolerant algorithm of topology for research.

In this paper, the Dual inverter-fed topology is analyzed, based on the idea that refer to voltage vector decoupled, proposed a kind of five level fault-tolerant algorithm that aimed at independent bus double NPC three-level inverter topology; set up a double three-level inverter speed control system experimental platform for validation, simulation and experimental results prove the effectiveness of the fault-tolerant algorithm.

2. The Dual Inverter-Fed Topology Analysis

2.1. Open-End Winding Three-Phase Asynchronous Induction Motor Mathematical Model Analysis

Open-end winding asynchronous motor without special manufacture, simply need to split stator winding that conventional asynchronous motor star connected into three-phase independent windings, and leads six end lines.

Compared with the traditional three-phase asynchronous motor, open-end winding induction motor is the same on the main structure, the difference is that the stator three phase current no longer meets the constraint conditions of Kirchhoff's current law $i_a + i_b + i_c = 0$, drive system circuit need special circuit design, when the motor running the stator voltage is equal to the power supply voltage synthesis results on both ends. Because the whole structure has not changed, open-end winding induction motor is consistent with traditional induction motor on the mathematical model, so the drive system can use the same control strategy.

2.2. Dual Inverter-Fed Topology Mathematical Model

The power supply device at both ends of topological winding of dual inverter can be a two-level inverter; can also be a multi-level inverter [4-8], the circuit model of topology is shown in Fig. 2.

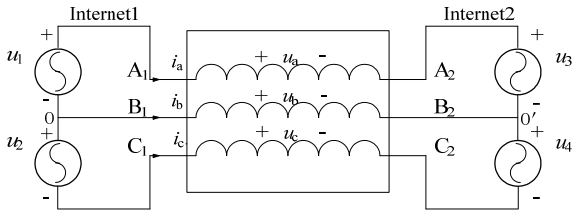


Fig. 2. Circuit model of the open-end winding induction motor drive system fed by two inverters.

Because the motor stator winding is open, the traditional definition of common-mode voltage is no

longer applicable, dual inverter topology common mode voltage is defined as the midpoint between two voltage inverters. Open-end winding induction motor phase voltage is

$$u_{a,b,c} = u_{A1,B1,C1} - u_{A2,B2,C2} - u_{00'}, \quad (1)$$

where uA1, B1, C1, uA2, B2, C2, respectively, the inverter 1, three-phase voltage inverter 2 output; u00 ' as a common-mode voltage.

According to Fig. 2, can be obtained circuit node current and mesh voltage equation from the Kirchhoff's law.

$$\begin{cases} u_1 + u_b = u_3 + u_a \\ u_2 + u_c = u_4 + u_b \\ i_a + i_b + i_c = 0 \end{cases} \quad (2)$$

For induction motors, the winding phase voltage

$$u_x = i_x R + L\frac{di_x}{dt}, x \in \{a, b, c\} \quad (3)$$

Standard three-phase asynchronous motor winding resistance R and L are equal, and that when the motor running, three-phase voltage initial value are zero, that is

$$u_a + u_b + u_c = 0 \quad (4)$$

By the formula (1) and formula (4) to derive the common mode voltage u00 ′ expression is

$$u_{00'} = (u_{A1} + u_{B1} + u_{C1} - u_{A2} - u_{B2} - u_{C2})/3 \quad (5)$$

If power supply device at the ends of the winding uses three-level inverter, the dc side voltage are Vdc, a phase, for example, the output voltage of the inverter1, uA1 can be output 0, + Vdc / 2, three kinds of voltage, uA2 also have 0, + Vdc / 2 of the three conditions. According to the type (1), when the common-mode voltage u00 ' is zero, the phase voltage Ua can be output 0, + Vdc / 2, ±5 five kinds of voltage. The space voltage vector diagram of topology of is the same as the conventional five-level topology, the simulation waveform of the common-mode voltage and phase voltage in Fig. 7(a), Fig. 7 (b), as shown in the load is resistive load. It can be seen that the common-mode voltage level number is 7, the number of phase voltage level number is 17, and the phase voltage waveform of conventional three-level topology circuit output as shown in Fig. 7(c), the voltage level number maximizes 9.

From the above analysis we can see that dual three-level inverter topology is equivalent to a five-level topology, compared with single-ended power supply topology, when using the switching devices that withstand same voltage level, can obtain higher output voltage, resulting in more space voltage vector and more voltage level number, DC-side voltage utilization rate is higher.

2. Dual Five-Level Inverter Topology SVPWM Fault-Tolerant Algorithm

2.1. Space Voltage Vector Decoupling

This paper selects the midpoint of double diode clamped (NPC) three-level inverter topology studies shown in Fig. 3, from the above, it is equivalent to a five-level converter. According to the requirements of fault-tolerant control, the algorithm needs to apply to both dual and single inverter power inverter power status, this paper, the space vector decoupling [12] the idea of the equivalent reference voltage vector is decomposed into two equivalent vector, respectively, by the inverter 1 and the inverter 2 generated separately.

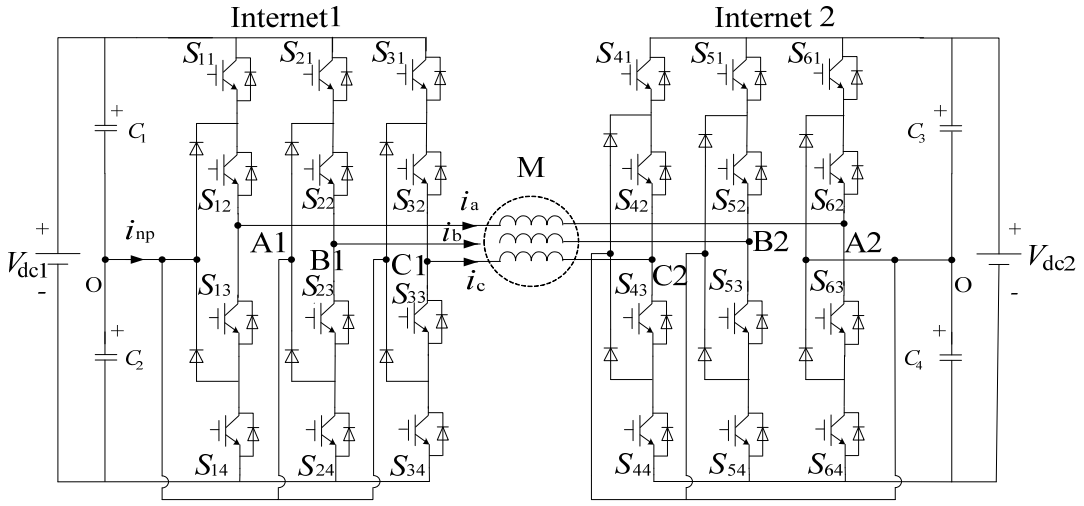


Fig. 3. Schematic of the open-end winding induction motor drive system fed with two NPC three-level inverters.

As shown in Fig. 4, V_{ref} is the Dual inverter-fed topology for reference voltage vector on the motor end, be decomposed into the same size and opposite direction of two equivalent voltage vector Vref1 and V_{ref2}, including V_{ref} = V_{ref1} - V_{ref2}, V_{ref1} and V_{ref2} respectively generated by inverter 1 and 2 inverter separately.

The advantage of space vector decoupling method is that when the system switch to a single of inverter power supply state, originally five-level SVPWM algorithm automatically degrades for three-level, just depends on the electrical motor load conditions change the given value, can maintain the system run full load or half load operation. For the convenience of digital implementation, shorten the operation time, a simplified three-level SVPWM algorithm is proposed.

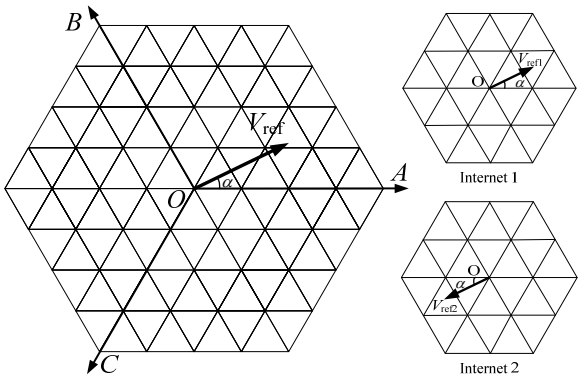


Fig. 4. The decoupled PWM strategy.

2.2. Simplified Three-Level SVPWM Algorithm

SVPWM modulation algorithm eventually need to be a switching time of the each vector of switching cycle (the opening of the switch compared with the turn-off time in each switch tube), thus to obtain the trigger pulse signal of each power devices. If according to the relationship between each variable, the corresponding formula is deduced, fully use of three-phase voltage Va, Vb, Vc, the dc side voltage Vdc, switch cycle Ts is to represent each switching cycle, compared the moment the opening of the switch tube to shut off, can according to the three-phase voltage, directly calculate the corresponding comparative moment.

As shown in Fig. 5, ti1 (I = a, b, c) is to control the switching time that phase bridge arm's first switching tube opening and turn-off, ti2 (I = a, b, c) is to control the switching time that phase bridge arm's second switching tube opening and turn-off. Each of the third, fourth switching tube of phase bridge arm, respectively, with the first and second switching tube opening and turn-off complementary, so there is no need to control the on-off alone, only will be make the first and second switch tube of a given trigger pulse then respectively control the third and fourth switch tube.

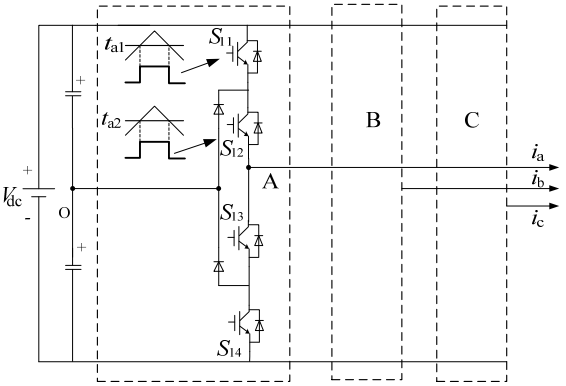


Fig. 5. Schematic diagram of switch-on and switch-off control for switches.

According to deduction, switching moment ti1 and ti2 general formula is:

$$t_{i1}=\begin{cases}\mathrm{T_s}/4, & (V_i<0,\ i=\mathrm{a,b,c})\\ \mathrm{T_s}(\frac{1}{8}-\frac{x_{i1}}{2V_{\mathrm{dc}}}+\frac{y_{i1}}{4V_{\mathrm{dc}}}), & (V_i\geq 0,\ i=\mathrm{a,b,c})\end{cases} \tag{6}$$

$$t_{i2}=\begin{cases}0, & (V_i>0,\ i=\mathrm{a,b,c})\\ \mathrm{T_s}(\frac{1}{8}-\frac{x_{i2}}{2V_{\mathrm{dc}}}+\frac{y_{i2}}{4V_{\mathrm{dc}}}), & (V_i\leq 0,\ i=\mathrm{a,b,c})\end{cases} \tag{7}$$

Among them, xi1, xi2, yi1 yi2, respectively, as follows:

$$x_{i1}=\begin{cases}V_i-\frac{1}{2}, & (V_i=V_{\max},\ |V_i|=V_{|\max|})\\ V_i, & (else)\end{cases} \tag{8}$$

$$x_{i2}=\begin{cases}V_i+\frac{1}{2}, & (V_i=-V_{\max},\ |V_i|=V_{|\max|})\\ V_i, & (else)\end{cases} \tag{9}$$

$$y_{i1}=y_{i2}=\begin{cases}V_{\mathrm{a}}+V_{\mathrm{c}}+Z_1, (V_{\mathrm{b}}^{'}=V_{\mathrm{mid}}^{'})\\ V_{\mathrm{b}}+V_{\mathrm{c}}+Z_2, (V_{\mathrm{a}}^{'}=V_{\mathrm{mid}}^{'})\\ V_{\mathrm{a}}+V_{\mathrm{b}}+Z_3, (V_{\mathrm{c}}^{'}=V_{\mathrm{mid}}^{'})\end{cases} \tag{10}$$

In the Formula, Va, Vb and Vc are respectively three-phase given voltage, Va ', Vb', and Vc 'as Va, Vb and Vc obtained the new three-phase voltage after through the reference voltage decomposition method [13], Vmid' is Va ', Vb', and Vc are 'intermediate value, Ts is the switching cycle, Vdc is DC voltage, Vmax is the maximum value in the Va, Vb and Vc, V | max | is maximumvaule that after Va, Vb and Vc taking the absolute value. Among them, Z1, Z2 and Z3 can be obtained by the following formula:

$$\begin{cases} Z_1=-\frac{1}{2},\ Z_2=0,\ Z_3=-\frac{1}{2}, & (V_a>-V_b, V_a\ge -V_c) \\ Z_1=\frac{1}{2},\ Z_2=\frac{1}{2},\ Z_3=0, & (-V_c>V_a, -V_c\ge V_b) \\ Z_1=0,\ Z_2=-\frac{1}{2},\ Z_3=-\frac{1}{2}, & (V_b>-V_c, V_b\ge -V_a) \\ Z_1=\frac{1}{2},\ Z_2=0,\ Z_3=\frac{1}{2}, & (-V_a>V_b, -V_a\ge V_c) \\ Z_1=-\frac{1}{2},\ Z_2=-\frac{1}{2},\ Z_3=0, & (V_c>-V_a, V_c\ge -V_b) \\ Z_1=0,\ Z_2=\frac{1}{2},\ Z_3=\frac{1}{2}, & (-V_b>V_c, -V_b\ge V_a) \end{cases} \quad (11)$$

The advantage of the algorithm is that only need three-phase given voltage signal to be able to quickly calculate the switching time of every switch's opening and turn-off, the moment you can get all the switches' trigger pulse signal. Compared with triangular carrier.

2.3. Neutral Voltage Balance and the Optimum Position of Space Vector

Neutral voltage balance using literature [14] proposed control method based on the balance control factor, the method is based on a switching cycle and point charge conservation principle to calculate the respective action time that small positive and negative vector participate in, make each switching cycle's neutral voltage fluctuation is zero. In fact this balance method when the load current passing zero or near zero, balance control factor f value is very big, beyond the constraints and forced to 1 or-1, this seven-segment SVPWM output will degenerate into six stages or five stages, make the harmonic characteristics of output waveform deteriorate, so need to be further optimized. According to the optimal space vector position theory in this paper, we can adjust the balance control factor in order to obtain the optimum harmonic performance.

Fig. 6 (a) shows the converter output voltage time integral (flux) track. The ideal trajectory of sinusoidal output voltage is a circle, but the switching converter work feature makes real trajectory is a substantially circular locus is shown in Fig. 6. Fig. 6 (b) shows flux trajectory in the switch cycle, Δθ as a switching cycle corresponds to the point of view, the area between space vector flux trajectory and the ideal flux trajectory to be minimized, the smaller the area of the region, then the quasi circular flux trajectory is closer to the ideal flux locus.

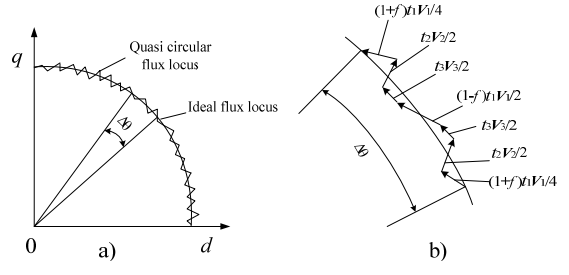


Fig. 6. The curve of flux locus.

Set switch sequence using the space vector V1, V2 and V3, the corresponding action time are t1, t2 and t3 respectively; the redundant switching state action time of space vector of is given by the following equation.

$$T_{V_1(1)}=\frac{1+f}{2}t_1 \qquad T_{V_1(2)}=\frac{1-f}{2}t_1$$
$$T_{V_2(1)}=T_{V_2(2)}=\frac{t_2}{2} \qquad T_{V_3(1)}=T_{V_3(2)}=\frac{t_3}{2} \quad (12)$$

In the formula, f is for balance control factor, two redundant switching states of V1 respectively occupy first, seventh segment and the fourth section of switch sequence.

The deviation between the quasi-circular trajectory and ideal trajectory of each switching cycle provides a means of measuring harmonic distortion, the deviation can calculate each switching cycle between two tracks area by integrating, so optimization problem is to identify a way to find the f value, make the smallest in order to achieve the best modulation strategy.

According to literature [15], the optimal values of fluctuates near zero, therefore, in the case of neutral voltage balance, as much as possible to reduce the f value for better performance of harmonic. By constantly adjusting the f value, resulting in reducing the total harmonic content of output current, f value is selected as shown in Table 1.

Table 1. Selection of the value for f.

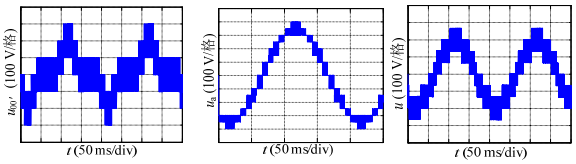
Condition	Selection of the value for *f*
$f\ge 0.2$	0.2
$0.1<f<0.2$	0.1
$-0.1\le f\le 0.1$	*f*
$-0.2<f<-0.1$	−0.1
$f\le -0.2$	−0.2

3. Simulation and Experiments

To verify the correctness and effectiveness of five-level SVPWM fault-tolerant algorithm proposed with simulation and experimental verification. Experimental parameters for: dc side voltage is 400 V, dc side capacitor C1 = C2 = 2200 μF, winding induction motor rated power is 5 kW, rated speed is 1420 RPM, a logarithmic np=2, stator resistance Rs=1.91 Ω, rotor resistance Rr = 1.45 Ω, stator self-inductance Ls=0.24939 H, rotor self-induction Lr=0.24939 H, the mutual inductance between the stator and rotor Lm=0.23507 H, load torque TL=7.5 N, m, to simulate the load in dc motor, the output voltage frequency is 50 Hz, the sampling frequency is 5 kHz, adopts TMS320F2812 DSP of TI company as the core of control circuit, MOSFET models is IRFP450. Open-end winding induction motor adopts

the vector control method. The simulation model is consistent with the experimental parameters.

Fig. 7 (a) and Fig. 7 (b) respectively is the common mode voltage and phase voltage waveform that dual three-level inverter power supply circuit with resistive inductive load, Fig. 7 (c) as the output phase voltage waveform that the NPC three-level topology circuit with resistive inductive load , the inverter dc side voltage is 400 V, the modulation ratio is 0.9. Contrast figure 7 (b) and (c) shows that compared with the single power supply topology, Dual inverter-fed topology output voltage level is more, can obtain higher output voltage.



(a) (b) (c)

Fig. 7. The voltage waveforms with series RL load: (a) common mode voltage, (b) phase voltage, (c) output phase-voltage of three level topology.

Fig. 8 (a) and Fig. 8 (b) respectively is rotational speed and torque waveform, to test and verify the fault-tolerant control of the system, at t = 1 s time will be one of the inverter is removed from the system. At about t = 0.8 s time motor speed is stable, to achieve a given rotational speed n = 1420 RPM, at this time the motor electromagnetic torque is equal to the load torque. At t = 1 s moment, by the characteristics of fault tolerant modulation algorithm, this time the given speed is half of the given original, due to the jump speed can't instantaneously change, so the actual speed is greater than the given speed, motor is in the power generation state, change the mechanical energy into electrical energy, reduce speed to follow a given speed, from Fig. 8(c) and Fig. 8(d) can be found, inverter removal time, motor stator current occurs reverse jump and voltage is not, show that the power transmission direction change. At about t = 2 s moment, electromagnetic torque is equal to the load torque, motor speed achieve stable, for half a given original,, that is, n = 710 RPM.

Fig. 8 (e) and Fig. 8 (f) respectively for waveform that two inverter DC side capacitor voltage difference between the upper and lower, can be found that the capacitor voltage difference of transient process (neutral voltage fluctuations can be said) is greater than the steady state process, the whole process of neutral voltage fluctuations within ± 2 v, satisfies the requirement of neutral voltage balance. Fig. 8 (f) for the removal of inverter voltage waveform of the difference between the two capacitors in dc side, at t = 1 s, when the moment the inverter cut off, then the inverter dc side neutral without current inflow and outflow, neutral voltage will not fluctuate.

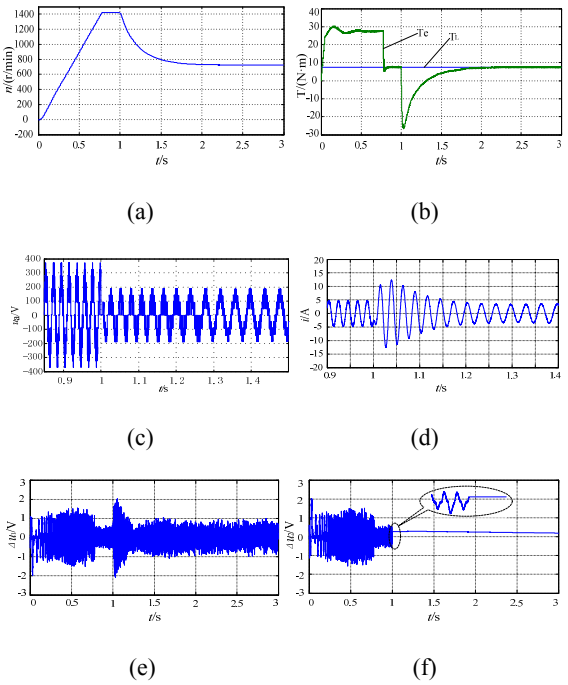


Fig. 8. The simulation waveforms of dual three-level inverter-fed induction motor drive system:(a) waveform of rotational speed, (b) waveform of torque, (c) waveform of the phase voltage for motor, (d) waveform of the phase current for motor, (e) waveform of the two capacitor-voltage difference in DC link, (f) waveform of the two capacitor-voltage difference in DC link for the removed inverter.

4. Conclusion

Dual inverter-fed topology output voltage is high, the level number is much, its independent bus structure has a good fault tolerant performance. For its fault-tolerant features, this article proposed algorithm has the following advantages:

The space voltage vector decoupling method is adopted, the motor end reference voltage vector is decomposed into two independent voltage vector, respectively produced by two inverters alone. Thus the system does not need to switch alternate algorithm in fault state, the original modulation algorithm for five-level is automatically degenerated from three-level, satisfying the system requirements.

On the basis of space voltage vector decoupling, by using the proposed simplified algorithm of the three-level, directly through three-phase given voltage after decoupling and switch cycle is to calculate each inverter corresponding switching moment, omit sector judgment and table lookup process, reduce the amount of code, shorten the program running time.

Using the optimal space vector position theory to adjust balance control factors, optimizing the output waveform, and reduced system requirements for sampling current signal accuracy

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