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Challenge of the Process Variation on Designing the On-Chip EMI Sensor Array

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Abstract: This paper presents our first design of the on-chip EMI sensor array. The feedback signal from the sensor array helps to determine the location of the failed circuit on the chip of an integrated circuit (IC) when external electromagnetic interference (EMI) is applied to the IC. The array structure, the feedback signal and the corresponding circuit of the sensor cell is developed. The design is implemented with a FPGA. The functionality of the design is checked through measuring the generated feedback signal of the FPGA. The feedback signal suffers instability problems due to the on-chip process variation. A set of equations are developed to describe the performance limitation that current IC technology put on the sensor array. The trade-off between the timing and the spatial resolutions of the array is analyzed. The conclusion of the paper shows the necessary conditions to make the measurement method practical. *Copyright © 2014 IFSA Publishing, S. L.*

Keywords: IC, EMI, Sensor, FPGA, Process Variation.

1. Introduction

When EMI is applied on an IC, the EMI signal is spread in the on-chip power distribution network (PDN). Some locations of the chip will be hot-spots [1]. At those hot-spots, the transistor circuits suffer great disturbance and even fail. To optimize the immunity of the IC, it is important to find the distribution of the hotspots. Therefore, it is interesting to measure the two-dimension (2D) EMI distribution in the PDN.

The most popular method to study EMI of ICs in a laboratory environment is the direct power injection method [2], which is sketched in Fig. 1. Under that environment, the on-chip EMI distribution has several important properties:

- The EMI signal comes from external sources.
- Monitoring locations are spread on the chip.
- The response of the IC to EMI is in real time.
- The IC is forced to fail in the immunity test.

The 2D EMI measurement method should match the aforementioned properties of EMI. Moreover the measurement itself should bring modification on the PDN as less as possible.

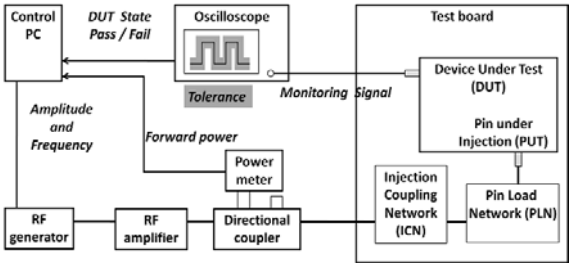

Fig. 1. Immunity Measurement Setup.

Measuring signals in PDN is difficult because the PDN is embedded on the chip inside the package. Several on-chip probing systems have been reported since 1990s [3-21]. However, when applying those systems to measure the 2D on-chip EMI in immunity test environment, following problems appear:

- The measured signals have to be stored first and then read out afterwards [3-8]. They are not suitable for real-time monitoring.
- There are control, switching, storage, buffering and other associative circuits [5-6, 9-19]. If those circuits fail due to their local EMI, the measured signals at target location cannot be properly read out. The location of the EMI hotspot cannot be determined.
- The target signal has to be internally generated in a repeated way [5-8]. They are not suitable to measure external signal with unpredicted waveform.
- Additional PDNs are inserted for probing circuits [8, 10-11, 20-21]. The measure fixture may modify the host PDN considerably.
- Multiple pins are required to measure and read the target signal of single location [8]. Appling that probing circuit in a massive way required too many pins and is thereby impractical.

The solution we propose in this paper is an on-chip EMI sensor array (EMISA). The array contains sensor cells distributed uniformly on the chip. The cells can send feedback signals indicating the cells' status. Sensor cells generate their feedback signals independently from each other. During the operation, the cells sense their local supply voltage. If the EMI shifts the local supply voltage by a certain threshold, the corresponding cell on that location fails and can no longer generate the correct feedback signal. By reading the feedback signals of the cell array, the failed cells can be identified. The location of the failed cells corresponds to the location in the PDN where severe EMI are presented. The EMISA performs the following operation mechanism:

- An EMISA has multiple sensor cells distributed on the chip.
- The operation status of cell is determined by only its local supply voltage.
- The cell status is presented by the feedback signal generated from the cell.
- The feedback signal of a cell can be accessed in real time.
- The propagation of the feedback signal from the target cell to off-chip circuit does not rely on circuit at any other location.
- The combination of the feedback signals of whole array form a feedback pattern.
- Sensor cells at the EMI hotspots fail during the immunity test.
- The feedback pattern implies locations of the failed cells.
- The locations of the failed cell show the distribution of the on-chip EMI hotpots.

Obviously, the EMISA has no storage circuits, no center control circuits, and no switch circuits. Watching the EMI at one location does not rely on the operation of any circuits at other locations. It is suitable to measure the on-chip EMI distribution in the immunity test environment.

This paper is organized as the following. The second section introduces the circuit structure and the operational mechanism of the proposed EMISA. The third section implements the sensor array with a FPGA. The feedback signals generated by the FPGA are presented. Based on the obtained pattern of feedback signals, problems of EMISA are pointed out. The fourth section discusses the origins of the problem. The limitation factors on the performance of EMISA are analyzed. The final section is the conclusion.

2. Principle and Design

The EMISA presented in this paper is called TSCI EMISA for the following reasons: the feedback signals are designed and analyzed in Time domain; the feedback signals from cells are assembled in Series and share a common output channel; the feedback signals are connected to the detector in a Conducted way; and the feedback signals from all cells have the Identical waveform.

2.1. Feedback Signal

The structure of the TSCI EMISA is shown in Fig. 2. The parameters of the array are given in Table 1. Each row (column) has a signal propagation path and a port. A signal propagation path starts with the port and ends at the last cell on the other side of a row (column). Outputs of sensor cells of the same row (column) are directly connected to the same signal propagation path. A signal propagation path for a row of cells is a row path. Its port is a row port. The signal propagation path for a column of cells is a column path. Its port is a column port.

A sensor cell contains a pulse generator and two delayers. All sensor cells have the same pulse generator. However, their delayers are different from each other. The generator produces periodical pulses. The pulse to the row path is delayed by a time proportional to the column index of the cell. The pulse to the column path is delayed by a time proportional to the row index of the cell.

Pulses of different cells on a row (column) arrive at the port at different time. Their arrivals are uniformly spaced in time domain. A pulse sequence thereby appears on the port. The signal seen on a port is called monitoring signals (MS). The expected regular pattern of MS in the normal operation is sketched in Fig. 2c. The pattern is repeated for every T_{CLK}.

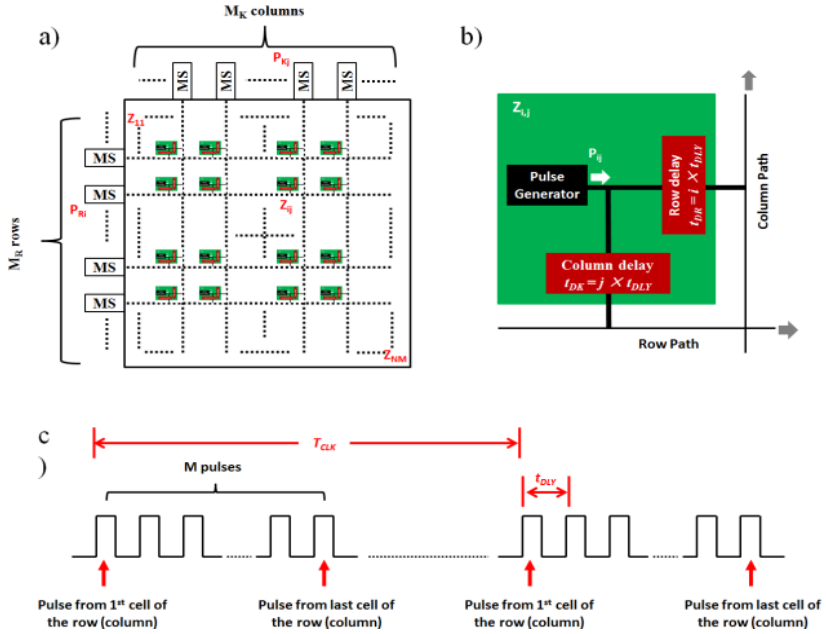

Fig. 2. The TSCI OCEMISA: a) array organization; b) Feedback signal generation; c) Expected feedback pattern.

Table 1. Parameters of the TSCI EMISA.

Parameters	Meaning
M_R	Number of the rows
M_K	Number of the columns
Z_{ij}	Sensor cell at (i, j)
P_{ij}	Pulse generated by Z_{ij}
t_{DLY}	Unit delay
T_{CLK}	Period of the cell pulse
t_{DK_ij}	Column delay time of Z_{ij}, $t_{DK\_ij} = j \times t_{DLY}$
t_{DR_ij}	Row delay time of Z_{ij}, $t_{DR\_ij} = i \times t_{DLY}$

The location of the failed cells is determined by the following mechanism: If cell Z_{ij} fails, the shape or the arrival time of its pulse will be modified. Consequently, waveforms of the monitoring signals on ports of the i^{th} row and the j^{th} column will be irregular. A port where the MS is irregular is called an error port. With the indices of the error ports, the location of the failed cells, which is at the i^{th} row and the j^{th} column, can be identified. The indices of the error ports form a vector called EPIV (error port index vector). For cases of single-cell failures, the EPIV uniquely determines the location of the failed cell.

2.2. Circuit of the Sensor Cell

The function of a sensor cell is to generate an output signal which is dependent on its supply voltage. A simple solution for the sensor circuit is shown in Fig. 3. The cell contains a ring oscillator and a counter with parameters defined in Table 2. The ring oscillator generates a clock whose period (T_{CLK_ij} for Z_{ij}) depends on the supply voltage. The clock is fed to a counter and produces a pulse, which is P_{ij}. By setting the parameter of the counter, the duration and the position of the pulse can be controlled in such a way that pulses of cells from a row (a column) form a required pattern like the one in Fig. 2c. The supply voltage at Z_{ij} is denoted with V_{ij}. When V_{ij} is changed by the EMI, T_{CLK_ij} will change, and the waveform of P_{ij} will change accordingly. Thus monitoring signals at the i^{th} row and the j^{th} column will be irregular. From the EPIV, the location of the corresponding V_{ij} is determined. In the circuit shown in Fig. 3, each cell has its own ring oscillator and counter, therefore cell signals are generated independently, and P_{ij} responds only to V_{ij}.

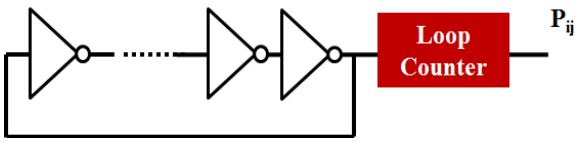

Fig. 3. Circuit of a sensor cell.

Table 2. Parameters of the Sensor Cell.

Parameters	Meaning
N_{RN}	Number of the cascaded NOT gates in the ring oscillator
N_{DIV}	Modulus of the counter

There are various methods to build the ring oscillator using CMOS logic gates. In this paper, the ring oscillator is composed of a chain of NOT gates of an odd number N_R. The period of an N_{RN} stage ring oscillator is $2N_{RN}$ times as long as the delay time of a NOT gate: $T_{RN} = 2N_{RN} \times t_{NOT}$. The t_{INV} stands for the delay time of NOT gate, which is affected by the local supply voltage.

The frequency divider module is designed as a loop counter. A N_{DIV}-modulus counter can divide the frequency of clock signal by $2N_{DIV}$. A pulse is generated for every $2N_{DIV} \times T_{RN}$. By increasing or reducing the modulus of the loop counter, we can adjust the pulse period. Also we can adjust the pulse width of the feedback signals. In this test design, N_{DIV} equals 64 and the pulse width is one T_{RN}. The pulse width is smaller than t_{DLY}. And t_{DLY} is much smaller than t_{CLK}.

3. FPGA Implementation of the TSCI EMISA

The Field Programmable Gate Array (FPGA) contains basic logic gates that can form NOT gate, counter, and delayer. The interconnections between gates are programmed. Moreover, the locations of the routed gates are selectable. The sensor cells can be easily implemented and positioned in a FPGA. The FPGA, when programmed as an EMISA, is called a FPGA EMISA. The FPGA EMISA can be applied to perform the initial function verification on the sensor circuit designed in the section 3. After the FPGA verification, a customized IC design procedure will be conducted to put the sensor design into an ASIC (application specified IC) chip in future. In this paper, a FPGA from [22] is utilized to implement the EMISA.

As the first step, a single cell is built in the FPGA to check the response of the cell to the EMI. In the original design, see Fig. 2, the cell drives the monitoring port directly. However, that is not possible in FPGA. Therefore the output of the sensor cell is connected to an input/output cell (I/O) of the FPGA. The monitoring port is driven by the I/O cell. The signal generated by the single cell is shown in Fig. 4. The cell generates pulses with period T_{CLK} as expected.

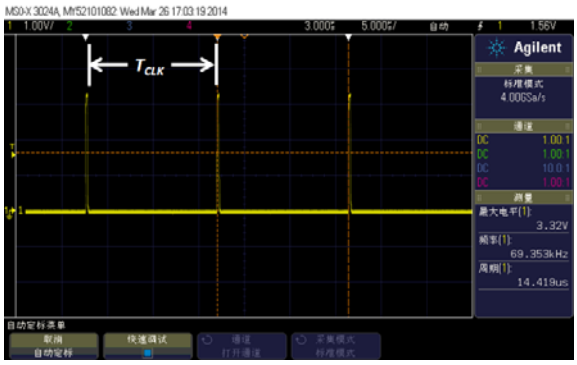

Fig. 4. Pulses generated by a single cell without EMI.

A radio frequency signal generator, as the EMI source, is connected to the supply pin of the FPGA. The frequency of EMI is set to be 940 MHz, which is much higher than the frequency of the ring oscillator. Refer to Fig. 5, applying EMI cause the duration of the pulse to be wider than the normal case. An increase in T_{CLK} is observed. The relationship between ΔT_{CLK} and V_{EMI} is relatively linear. Here V_{EMI} is the amplitude of the EMI at the source. The sensor do reacts with the EMI. Therefore, it can be utilized to detect the EMI.

After verifying the functionality of a single sensor cell, an 8-row and 8-column sensor array is implemented. The locations of cells and their indices are shown in Fig. 6. A necessary modification should be made here. In the original design, outputs of cells of the same row (or column) are connected to the same signal propagation path. That is not realizable with FPGA. Therefore, the feedback signals from the cells of the same row (or column) are connected to an OR gate. Noting that delayers of different lengths are inserted between the output of the counters and the inputs of the OR gate.

The MS are displayed with an oscilloscope. Snapshots of two typical waveforms of the MS at a row port are shown in Fig. 7. We do observe repeated eight-pulse sequences on the oscilloscope, as expected. However there are two negative behaviors on the MS waveform.

The first negative behavior is the phase difference. In Fig. 7a or Fig. 7b, each snapshot contains two cycles and each cycle has a sequence of eight pulses. The spaces between two neighboring pulses are not uniform. The cause of the problem is the phase difference between the ring oscillators and delayers of the different cells. The problem makes it difficult to recognize the pulse from the first cell of a row (or column).

The second negative behavior is the frequency difference. Comparing the sequence waveforms in Fig. 7a or Fig. 7b, we can find that the spaces of pulses in a sequence are changing with time. The cause of the problem is the frequency difference between the ring oscillators of different cells. If the oscillators of cells operate with different frequencies, then the pulse pattern on the MS will not be a fixed pattern. Without a fixed regular pattern, it is very difficult to judge the operation status of a MS. Moreover, it is impossible to recognize the location of the corresponding cell for a specific pulse.

The phase difference problem is bad but still solvable. Due to the phase problem, the exact position of pulse of a cell in the feedback pattern is unknown. However, a cell is monitored with a column port and a row port. If a cell fails, a distorted pulse appears on both the column port and the row port of the cell. Recoding the EPIV gives the location of the failed cell.

The frequency difference problem is fatal. The origin of the problem is the process variation on a chip. The geometry and chemical components of a circuit element like transistors vary with location on a chip. Consequently, the electrical properties of the circuits of the same type but at different locations are different.

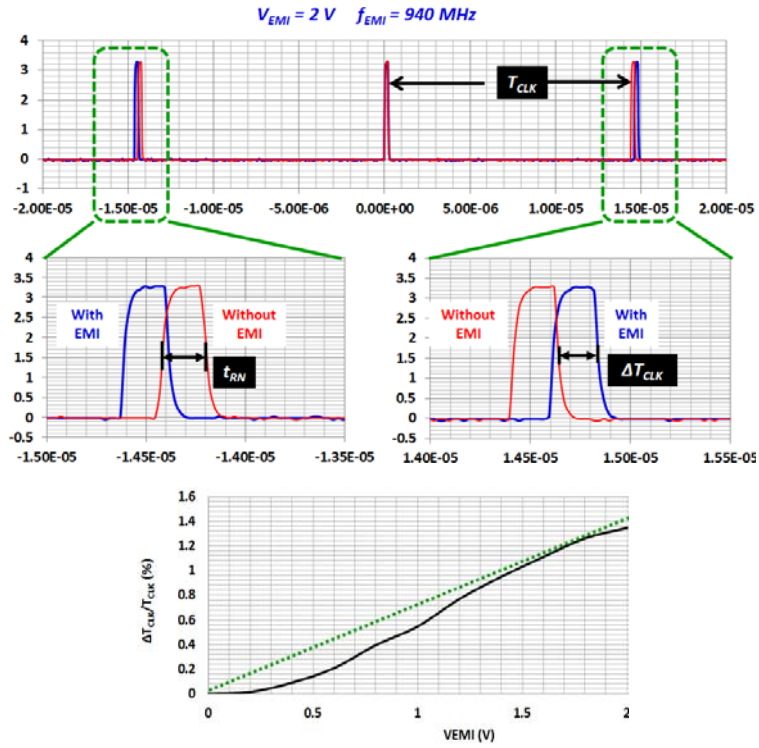

Fig. 5. Response of a single cell to EMI.

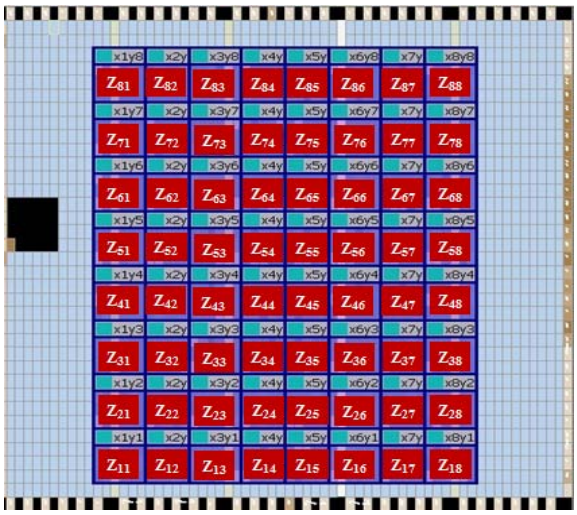

Fig. 6. Distribution of the sensor cell in FPGA.

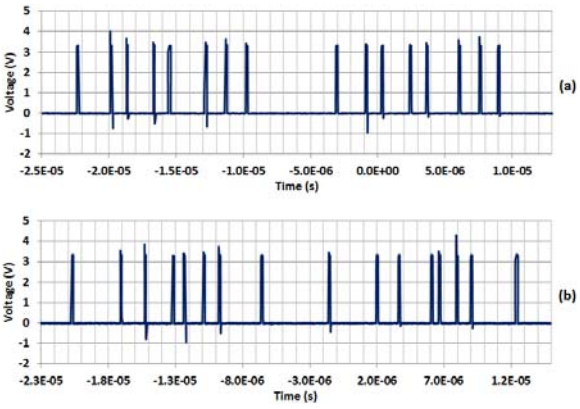

Fig. 7. Measured monitoring signals.

The process variation in FPGA will also happen in ASIC. The phase and frequency variation problems will appear when the sensor array is implemented with ASIC.

4. Discussion

The above experiment shows the difficulty in implementing the TSCI EMISA. It is a problem due to the process technology. It is interesting to see whether we can overcome the difficulty and apply the TSCI EMISA for voltage distribution measurement or not. The question is addressed through three aspects:

1) What is the up limit of the stability performance?

2) How to optimize the sensor circuits?

3) How to adapt the voltage distribution measurement procedure?

4.1. Arrival Jittering (Δt_{ij})

With the parameters defined in Table 3, the arrival time of the $(N_{CLK}+1)^{th}$ pulse generated by cell at (i,j) at the row port is rewritten as (1). The second term of the right side is the accumulation of the clock periods; the third term is the delayer's delays. By inserting the expression of T_{CLK} (2), (1) can be converted into (3).

Table 3. Parameters of the cell pulse.

Parameters	Meaning
t_s	Occurrence time of the first pulse of a cell
t_{DIV}	Delay of the counter
N_{CLK}	Number of the past clock cycles
t_{ij}	Actual arrival time of a pulse from Z_{ij}
t_{ij0}	Average arrival time of a pulse from Z_{ij}
Δt_{ij}	Arrival jittering, $\Delta t_{ij} = t_{ij} - t_{ij0}$

$$t_{ij} = t_{s\_ij} + \sum_{k=0}^{N_{CLK}} T_{CLK\_ij} + it_{DLY}\,, \quad (1)$$

$$T_{CLK\_ij} = (2N_{RN})t_{NOT\_ij}(2N_{DIV}) + t_{DVI\_ij}\,, \quad (2)$$

$$t_{ij} = t_{S\_ij} + 4N_{RN}N_{DIV}\sum_{k=0}^{N_{CLK}} t_{NOT\_ij} + \sum_{k=0}^{N_{CLK}} t_{DIV\_ij} + it_{DLY\_ij} \quad (3)$$

(3) shows that the actual pulse arrival time is determined by t_S, t_{NOT}, t_{DIV}, t_{DLY}. Variations of those parameters with time cause the pattern instability problem. Variations of those parameters with location cause the phase difference problem.

Table 4 defines a few processing parameters. With those parameters a few equations can be established as (4) – (7). With the definition of the ideal arrival time (8), the shift of the arrival time can be calculated with (9). For simplicity in writing, the shift of the arrival time is called the arrival jittering. Fig. 8 depicts the timing parameters on the waveform of the feedback signal.

Table 4. Process Parameters of FPGA.

Parameters	Meaning
t_{S0}	Average starting time of first pulse of a cell
t_{DLY0}	Average propagation delay of a delayer
t_{NOT0}	Average propagation delay of a NOT gate
t_{DIV0}	Average delay of a counter
β	Spatial variation of (t_S, t_{DLY}, t_{NOT}, t_{DIV})
$\Delta\beta$	Range of the spatial Variation in the temporal evolution of (t_S, t_{DLY}, t_{NOT}, t_{DIV})
γ	Temporal variation of (t_S, t_{DLY}, t_{NOT}, t_{DIV}), $\gamma = \gamma_{AVE} + \gamma_{VAR}$
$\Delta\gamma$	Range of the temporal variation in the temporal evolution of (t_S, t_{DLY}, t_{NOT}, t_{DIV})

$$t_{S\_ij} = t_{S0}[1 + \beta_S(i,j)]\,, \quad (4)$$

$$t_{DLY\_ij} = t_{DLY0}[1 + \beta_{DLY}(i,j) + \gamma_{DLY}(t,i,j)]\,, \quad (5)$$

$$t_{N0T\_ij} = t_{N0T0}[1 + \beta_{N0T}(i,j) + \gamma_{N0T}(t,i,j)]\,, \quad (6)$$

$$t_{DIV\_ij} = t_{DIV0}[1 + \beta_{DIV}(i,j) + \gamma_{DIV}(t,i,j)]\,, \quad (7)$$

$$t_{ij0} = t_{S0} + 4N_{RN}N_{DIV}\sum_{k=0}^{N_{CLK}} t_{NOT0} + \sum_{k=0}^{N_{CLK}} t_{DIV0} + it_{DLY0}\,, \quad (8)$$

$$\Delta t_{ij} = \Delta t_{S0} + 4N_{RN}N_{DIV0}\sum_{k=0}^{N_{CLK}} \Delta t_{N0Tij} + \sum_{k=0}^{N_{CLK}} \Delta t_{DIV\_ij} + i\Delta t_{DLY\_ij}\,, \quad (9)$$

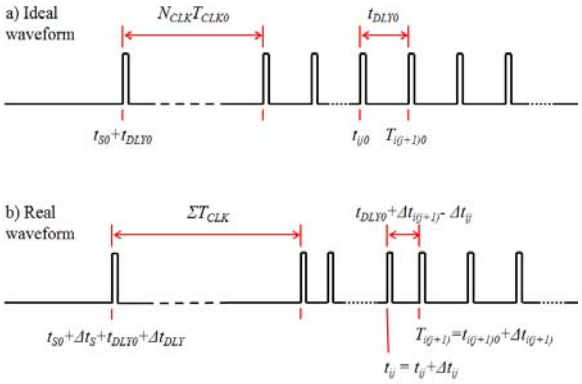

Fig. 8. Waveform parameters.

4.2. Spatial Variation in the Arrival Jittering Due to β

The arrival jittering due to the spatial variation of the process parameters alone is given in (10).

$$\Delta_S(t_{ij}) = t_{S0}\beta_S(i,j) + 4N_{RN}N_{DIV}N_{CLK}t_{N0T0}\beta_{NOT}(i,j) + t_{DIV0}N_{CLK}\beta_{DIV}(i,j) + t_{DLY0}i\beta_{DIV}(k,j) \quad (10)$$

The second and third terms of the right side in (10) shows that $\Delta S(t_{ij})$ changes with time (N_{CLK}). Because β varies with the cell location, the change in $\Delta S(t_{ij\_L})$ is not uniform. That means the space of the pulses from different cells change with time. Consequently, the pulse pattern is broken. The difference in the shifts of the two neighbor pulses is called the relative shift. Suppose the maximal difference of β is Δβ, the worst-case relative shift is estimated with (11).

$$\delta_S(t_{ZP}) = 4N_{RN}N_{DIV}t_{N0T0}N_{CLK}\Delta\beta_{NOT} + t_{DIV0}N_{CLK}\Delta\beta_{DIV} \quad (11)$$

Fig. 9 shows a pattern mask on the oscilloscope, with which the feedback signal can be checked. If the feedback signal does not fit the mask, the circuit is considered to be wrong. If the relative shift exceeds t_{DLY0}, the feedback pattern will not fit the mask. The circuit will be considered wrong even in absence of the external EMI. Therefore, to measure the voltage distribution on the chip, (12) must be satisfied for the entire duration of the measurement

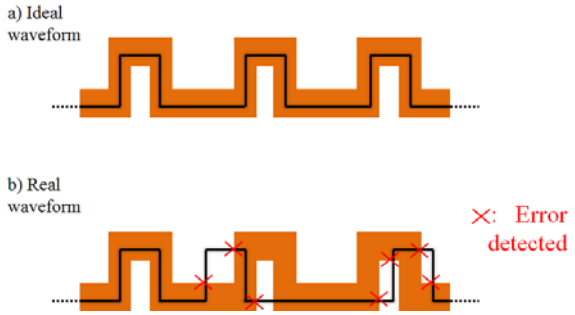

Fig. 9. Criterion for detecting the intolerable EMI.

$$\delta_S(t_{ZP}) < t_{DLY0} \tag{12}$$

If the spatial variation alone is considered, we can use (11) and (12) to calculate the maximal number of clock periods in the measurement duration, as shown in (13). t_{DVI0} is roughly the order of $N_{DIV}t_{NOT0}$. For large N_{RN}, the denominator of the second term in the right side of (13) is neglectful. The expression of the maximal number clock period can be simplified as (14). The corresponding measurement time is given in (15).

$$N_{CLK} < \frac{t_{DLY0}}{T_{CLK0}\Delta\beta_{NOT}} \frac{1}{1+\frac{1}{4N_{RN}N_{DIV}}\frac{t_{DIV0}}{t_{NOTO}}\frac{\Delta\beta_{DIV}}{\Delta\beta_{NOT}}}, \tag{13}$$

$$N_{CLK\_\max\_S} = \frac{t_{DLY0}}{T_{CLK0}\Delta\beta_{NOT}}, \tag{14}$$

$$t_{MT\_S} = N_{CLK\_\max} T_{CLK0} = \frac{t_{DLY0}}{\Delta\beta_{NOT}} \tag{15}$$

4.3. Spatial Variation in the Arrival Jittering Due to γ

Same analysis can be made on the effect of γ. The arrival jittering due to the temporal variation of the process parameters alone is given in (16).

$$\Delta_T(t_{ij}) = 4N_{RN}N_{DIV}t_{NOT0}\sum_{k=0}^{N_{CLK}}\gamma_{NOT} + t_{DIV0}\sum_{k=0}^{N_{CLK}}\gamma_{DIV} + it_{DLY0}\gamma_{DIV} \tag{16}$$

The worst-case relative shift can be estimated with (17).

$$\delta_T(t_{ZP}) = 4N_{RN}N_{DIV}t_{NOT0}N_{CLK}\Delta\gamma_{NOT} + t_{DIV0}N_{CLK}\Delta\gamma_{DIV} + t_{DLY0}\Delta\gamma_{DIV} \tag{17}$$

If the temporal variation alone is considered, we can use (17) and (18) to calculate the maximal number of clock cycles in the measurement duration. The formula is given in (19) and simplified as (20). The corresponding measurement duration in time scale is given in (21).

$$\delta_T(t_{ZP}) < t_{DLY0}, \tag{18}$$

$$N_{CLK} < \frac{t_{DLY0}(1-\Delta\gamma_{DIV})}{T_{CLK0}\Delta\gamma_{NOT}} \frac{1}{1+\frac{1}{4N_{RN}N_{DIV}t_{NOT0}}\frac{t_{DIV0}\Delta\gamma_{DIV}}{\Delta\gamma_{NOT}}} \tag{19}$$

$$N_{CLK\_\max\_T} = \frac{t_{DLY0}(1-\Delta\gamma_{DIV})}{T_{CLK0}\Delta\gamma_{NOT}}, \tag{20}$$

$$t_{MT\_T} = N_{CLK}T_{CLK0} = \frac{t_{DLY0}(1-\Delta\gamma_{DIV})}{\Delta\gamma_{NOT}} \tag{21}$$

4.4. Overall Spatial Variation in the Arrival Jittering

The total amount of the relative shift is the sum of effects due to β and γ, see (22). If ΔγDIV is sufficient small, the maximal duration allowed to complete an immunity measurement is given in (23) and (24). The duration is inversely proportional to the process variation parameters.

$$\delta(t_{ZP}) = \delta_S(t_{ZP}) + \delta_T(t_{ZP}), \tag{22}$$

$$N_{CLK\_\max} = \frac{t_{DLY0}}{T_{CLK0}(\Delta\beta_{NOT}+\Delta\gamma_{NOT})}, \tag{23}$$

$$t_{MT} = \frac{t_{DLY0}}{\Delta\beta_{NOT}+\Delta\gamma_{NOT}} \tag{24}$$

To observe how serious the process variation is, a special experiment is done: the repetition rate of the pulses of 64 cells are measured and compared. The pulse rate of a cell is averaged by 10000 times. The measurement results are presented in a frequency distribution map in Fig. 10. The map is draw with 8 by 8 mono-color gray blocks. Each block corresponds to a sensor cell in Fig. 6. The gray scale

of block gives the pulse rate. The right bar in the figure gives the scale of the frequency.

In Fig. 10, the pulse rate ranges from 67.2 kHz to 69.0 kHz. The frequency distribution map gives a variation in the pulse frequency of 2.7 %. That is the rough value of $\Delta\beta_{NOT} + \Delta\gamma_{NOT}$. In Fig. 7, t_{DLY0} is 2 μs and T_{CLK0} is 20 μs. According to (24), N_{CLK_max} is 3.7. That means a feedback pattern can be hold only for 4 cycles and the measurement should be completed within 74 μs. It is impractical.

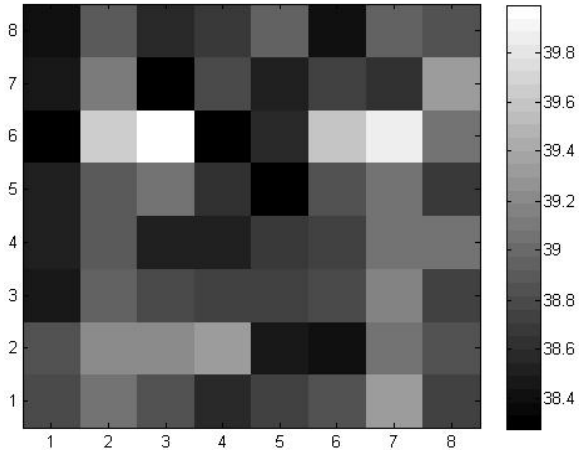

Fig. 10. Pulse rate (in kHz) of cells at different location.

4.5. Array Optimization

The instability limit causes the tradeoff between the timing and the spatial resolution of the measurement. t_{DLY0} and T_{CLK0} are not completely independent. All pulses of cells from the same row (or column) should appear within one clock cycle. Relationship (25) must be hold. Inserting (26) into (24), we obtain (26).

$$M_{R,K} t_{DLY0} = \alpha T_{CLK0} \qquad 0 < \alpha < 1, \tag{25}$$

$$N_{CLK\_\max} M_{R,K} = \frac{\alpha}{\Delta\beta_{NOT} + \Delta\gamma_{NOT}} \tag{26}$$

N_{CLK_max} corresponds to the timing resolution of the measurement. $M_{R,K}$ corresponds to spatial resolution of the measurement. (26) shows that for a given process, the product of those two resolutions is a constant. Fig. 11 shows the up-limit of the timing and spatial resolutions for various process uniformity.

If 100 T_{CLK0} measurement time is desired on a 10 * 10 array, the spatial process variation should be less than 0.1 %. The requirement is far beyond what can be offered in the current state of art [23].

As the IC technology approaches nano-meter scale, the process variation increases. Under that technology, it is almost impossible to get a stable pattern of pulses from independent cells. The time-domain feedback scheme does not work. Another approach should be developed so that independent feedback signals form a stable pattern under the current process variation. A possible solution is to set T_{CLK} of the cells different from each other and monitor the MS in frequency domain. In frequency domain, the spectrums of the cell pulse are stable and are separated from each other. The process variation may broaden of the spectrum of the cell pulses thus cause overlap between the signals of two cells. However, the problem can be solved by selecting proper value of the difference in T_{CLK}.

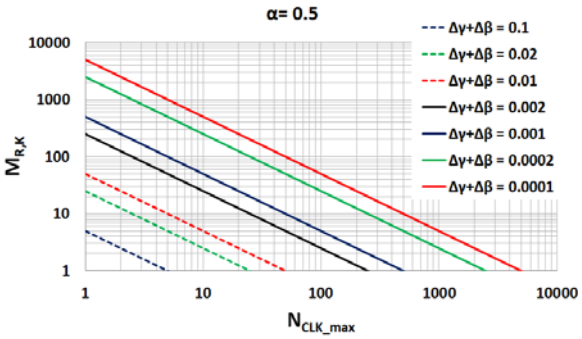

Fig. 11. Tradeoff between spatial and timing resolutions.

5. Conclusions

It is interesting to see a two-dimension distribution of the EMI voltage in the power distribution network on an IC chip. There is a wide range of possible schemes of OCEMISA for measuring the distribution. The TSCI is an intuitively simple approach to perform the measurement. The process variation causes instability problem on the feedback signals and thereby limits the application of the feedback pattern to monitor the EMI voltage. The limitation is expressed in an analytical way by relating the process variation parameter to the spatial and the timing resolutions of the measurement. Under current processing technology, the TSCI scheme cannot measure two-dimension distribution of the EMI voltage with reasonable spatial and timing resolution. Looking for a solution in frequency domain might be the right direction to realize EMISA.

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