

## Comparative Analysis of Shift Registers in Different Nanometer Technologies

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**Abstract:** In this paper, power and speed efficient registers have been designed using different nanometer technologies. Serial in Serial out (SISO) and Serial in Parallel out (SIPO) shift registers are designed using 180 nm and 90 nm technologies. Both the design are analyzed and compared based on power, delay and power-delay-product (PDP). Present portable real time system demands high performance in terms of speed along with low power consumption. The concept of technology scale down has been used to optimize power and delay in booth designs. The schematic of SISO and SIPO has been developed using Cadence Virtuoso software and analysis has been performed using Analog Design Environment. It has been observed from simulation analysis that 90 nm based SISO design shows an improvement of 68.61 % in power and 54.92 % in delay as compared to 180 nm technology. Likewise SIPO design has shown an improvement of 67.75 % in power and 53.32 % in delay as compared to 180 nm technology.

**Keywords:** CMOS, Flip Flop, Shift register, SISO, SIPO, VLSI.

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### 1. Introduction

The new era of technology had a great impact on the field of Very Large Scale Integration (VLSI), which is constantly under examination by many researchers throughout the world. It involves mainly reduction of delay and power consumption [1]. Due to high demand for portable electronics devices, the major concentration is on the low power systems. The amount of components on a chip are continuously increasing, thus resulting in a need of higher packing density. So with there exists another problem of rising power consumption. Thus in order to enhance the amount of battery life in portable devices and avoid overheating problem, it is very much important to reduce the total consumption of power. Therefore, it has become an eminent task for the designers to acknowledge the power consumption in complex Integrated Circuits (ICs) along with the delay parameter as well as energy. Further, power has turned

into a crucial parameter which needs the concern and understanding of developer while designing any circuit in modern VLSI applications, notably for those designs utilizing small scaled Complementary Metal Oxide Semiconductor (CMOS) technologies [2]. Most vital component of the ICs for temporary storage of data is a Flip Flop. It stores a logical condition of one or more input signals using external clock [3]. Flip-flops are used in majority of computational circuits to store the data and provide adequate processing time to different circuits inside a system. In CMOS circuits,

D Flip Flop (DFF) is essential building block and is responsible for the delay and total power dissipation calculations of any electronic system. Shift registers, which are created with the help of D flip-flops, have their intensive applications in various VLSI fields. The design of a shift register includes an N-bit shift register, made out of N number of Flip Flops [4]. While working with digital circuits, it is required to remember that register based execution has high speed

processing. The power and speed of the processor is determined with the help of number of register that processor has and the size of each register [5].

A register is a circuit with two or more D Flip Flops connected together such that they all work exactly in the same way and a single clock synchronizes all the flip flops [6]. Each of these flip-flops has the ability of storing a single logic i.e., 0 or 1. There are limited compositions of 0 and 1 that can be stored into a register. These combinations are called the state of the register. Flip-Flops can store data in multiple sizes like 4, 8, 16, 32 or even 64 bits. Thus, several Flip Flops are combined to store whole data which form register [7]. So, a shift register is actually a collection of flip-flops. Utmost essential utilization in shifting and storage of data in computers, calculators and other electronics systems such as two binary numbers before they are added together or to shift the data from either a serial to parallel or parallel to serial form [8]. Serial data across small distances of tens of centimeters, utilize shift register to obtain data into and out of microprocessors. Various factors, along with analog to digital converter, digital to analog converters, memory (digital storage), and display drivers, utilize shift registers to lower the amount of wiring in the circuit board [9]. Some counter circuits literally utilize shift register to develop repeating waveforms. Large shift registers usually act as the support of feedback generators for long time, so that they might look like pseudo-noise, random noise. The particular data latch that produce up a single shift register are all directed by a same clock (CLK) signal from them synchronous devices. Shift register IC's are usually given with a clear or reset connection so that they can be "SET" or "RESET" as appropriate. Fully custom 4-bit CMOS shift register consumes less power and less area as compare to semi-custom and auto generated designs [10].

## 2. Shift Register

All flip-flop is a binary cell which is able to storing one bit of information. A Register is built up by a group of flip-flop. A register made up of  $n$  flip-flop is an  $n$ -bit register. Fundamental function of a register to store the information sequence in digital system so that during any computing process logic element access it easily. As long as there is finite number of flip-flop in a register and every register is able to store a single 0 or 1 bit, so that a register can store finite number of 0-1 combinations. All of those combinations is known as state or content of that register. By using flip-flop data can be store bitwise but generally data does not carry out as single bits. Rather it is familiar to store data words of  $n$  bit in register with general word lengths of 4, 8, 16, 32 or even 64 bits. Hence, to store whole data words a register is made up using several number of flip-flops [11].

In registers single clock line is used to control all flip-flops that's why it is a synchronous circuits. The shift register is particular sequential logic circuits that

is utilize to store or transfer sequence of bits (data) in binary form and after that "shifts" the bits out once at each clock pulse. It mainly compose of certain single bit "D-Type Data Latches", for every bit (0 or 1) joined proper in a serial or daisy-chain layout so that output come out from one latch turn into the input of the next latch and go on. The data bits (0 or 1) can supply in or out of register serial manner, i.e. one follow the other from either the direction right or left, or in parallel, i.e. all composed [12].

### 2.1. Serial-in to Serial-out (SISO)

The number of bits to be stored in single shift register state the need for number of individual data latch used in that register. In serial shift register data is inserted serial form and read directly in a serial form from the output  $Q_D$ . In the circuit shown in Fig. 1, data are approved to progress over the register and out of the other end. Because there is only one output, the data go through the shift register one bit at a time in a serial pattern, accordingly the name Serial-in to Serial-Out Shift Register or SISO. The SISO structure is one of the easy configuration of the shift registers in that it has only three contact, the serial input (SI) which settle what enters the left hand flip-flop, the serial output (SO) which is caught from the output of the right hand flip-flop and the sequencing clock signal (Clk). Fig. 1 shows a generalized 4 bit serial-in serial-out shift register [13].

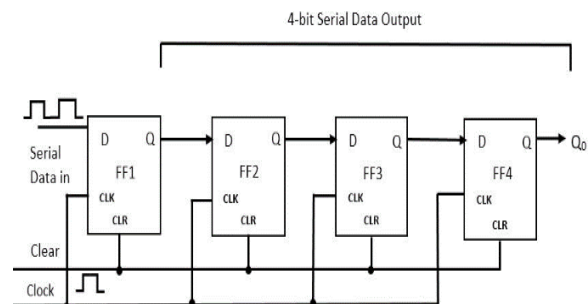


Fig. 1. Serial-In Serial-Out 4-bit Shift Register.

Assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) in Fig. 1 and that the output at logic level "0" i.e., no parallel data output. If a logic "1" is connected to the DATA input pin of FFA then on the first clock pulse the output is remain "0". The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at QA. After the fourth clock "1" at the output will appear. Table 1 show propagation of logic "1".

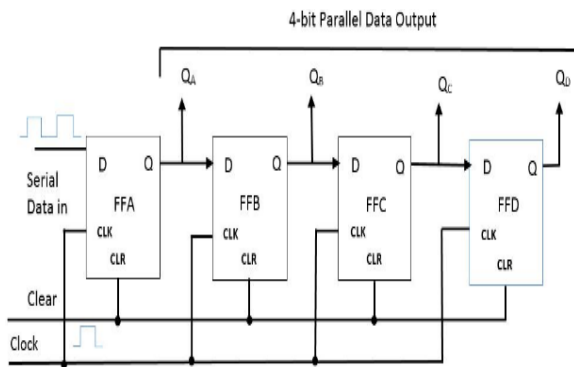
SISO is the type of Shift Register that work as a temporary storage device or as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register, 4, 8, 16 etc. or by varying the application of the clock pulses [14].

**Table 1.** Movement of data through SISO shift register.

| Clock Pulse No. | QA | QB | QC | QD |
|-----------------|----|----|----|----|
| 0               | 0  | 0  | 0  | 0  |
| 1               | 1  | 0  | 0  | 0  |
| 2               | 0  | 1  | 0  | 0  |
| 3               | 0  | 0  | 1  | 0  |
| 4               | 0  | 0  | 0  | 1  |
| 5               | 0  | 0  | 0  | 0  |

## 2.2. Serial-in to Parallel-out (SIPO)

Fig. 2 shows a 4-bit Serial-in to Parallel-out Shift Register. Initially RESET (CLEAR input) have been given to all flip-flops and then get logic level "0" at all the outputs  $Q_A$  to  $Q_D$  i.e., no parallel data output. If DATA input pin of FFA is connected to logic "1" then output of FFA is generated on first clock pulse and hence the output  $Q_A$  will be logic "1" set to HIGH along with the all other outputs still being at LOW logic "0". Now suppose that the DATA input pin of FFA has restored LOW anew to logic "0" providing us one pulse or 0-1-0.

**Fig. 2.** Serial-In to Parallel-Out 4-bit Shift Register.

At second clock pulse output of FFA will change to logic "0" and the output of FFB i.e.  $Q_B$  HIGH to logic "1" as its input D has the logic "1" level on it from  $Q_A$ . Now the logic "1" has been "shifted" or moved one step in register to the right as it is now at  $Q_A$ . Whenever the third clock pulse came this logic "1" value shifted to the output of FFC ( $Q_C$ ) and it goes on unless the fifth clock pulse arrive that set back again all the outputs  $Q_A$  to  $Q_D$  to logic level "0" as the input to FFA is maintained at logic level "0" [15].

The arrive of every clock pulse is to shift the data bits of each point one step to the right, and this is presented in below table unless the entire data sequence of 0-1-0-1 is saved in the register. Now, this data sequence can be get directly from  $Q_A$  to  $Q_B$

outputs. Hence data has been transformed from a serial data input to parallel data output. The truth table, shown in Table 2, shows the going on of the logics through the register from left to right with clock pulses. It is observe that after the fourth clock pulse, the 4-bits of data (0-1-0-1) are save in the register and will preserve rather providing clock of register has been stopped.

**Table 2.** Movement of data through SIPO shift register.

| Clock Pulse No. | QA | QB | QC | QD |
|-----------------|----|----|----|----|
| 0               | 0  | 0  | 0  | 0  |
| 1               | 1  | 0  | 0  | 0  |
| 2               | 0  | 1  | 0  | 0  |
| 3               | 1  | 0  | 1  | 0  |
| 4               | 0  | 1  | 0  | 1  |
| 5               | 0  | 0  | 0  | 0  |

In practice the input data to the register may consist of various combinations of logic "1" and "0". The practical application of the serial-in/parallel-out shift register is to convert data from serial format on a single wire to parallel format on multiple wires for example to illuminate LEDs (Light Emitting Diodes) [16].

## 3. Schematic Design Simulation

Due to technology scaling the circuit of serial shift register is designed for different technology nodes in the Nano scale regime. The design also requires the use of different operating voltages for different technologies, like 1.8 V for 180 nm and 1.2 V for 90 nm technologies. Fig. 3 shows that these registers are constructed with the help of D flip flops, which again comprises of NAND gates.

D flip flops are connected serially so as to form the serial shift register, in which the input as well as output proceeds in a serial fashion. 4-bit SISO shift register schematic design is shown in Fig. 4 for all the technology nodes.

Analog simulation of designed SISO shift register has been performed for logic verification. The transient responses of proposed register, along with their power variations are shown in Fig. 5 and Fig. 6 for different nodes.

Fig. 7 and Fig. 8 show the DC response of SISO shift register for 90 nm and 180 nm technology nodes.

To improve the speed factor SIPO shift register schematic is designed as shown in Fig. 9. In this speed is more as the data is sent in a serial manner, while the output is taken out simultaneously, in a parallel fashion.

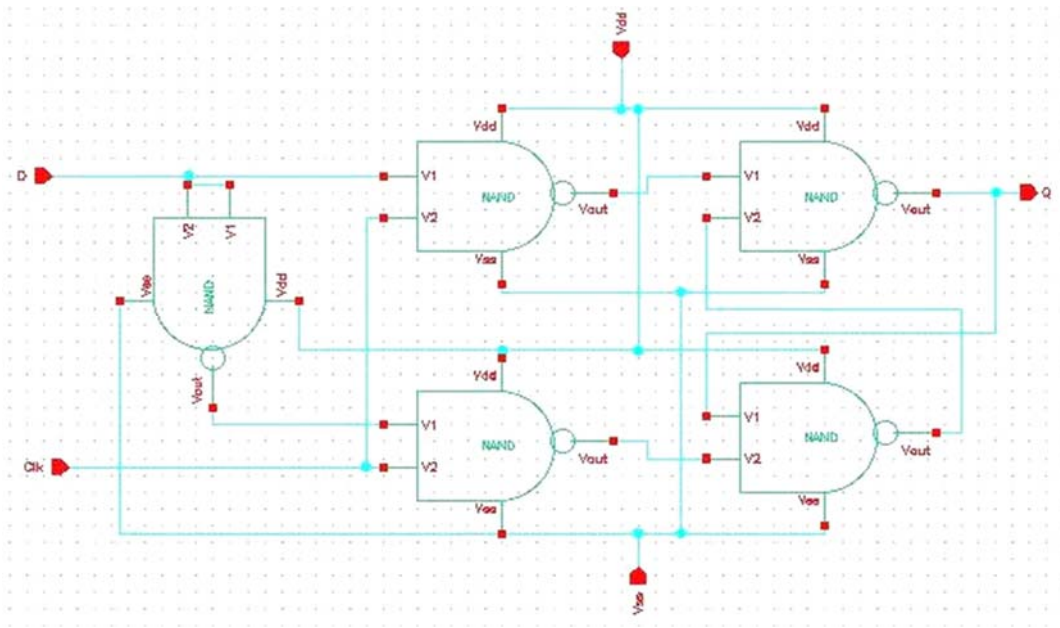


Fig. 3. Schematic Design of D Flip-Flop.

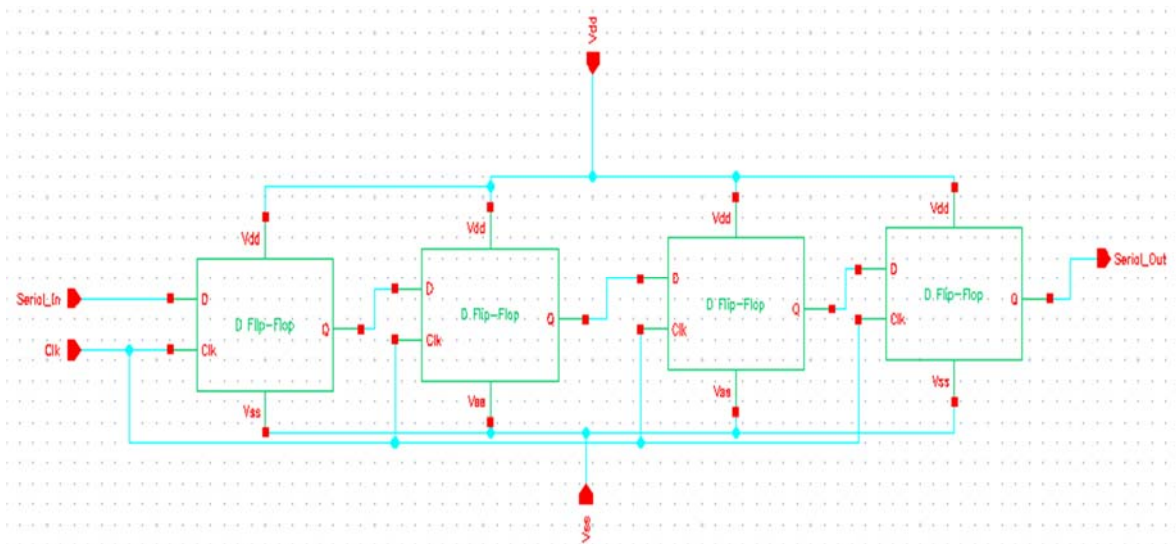


Fig. 4. Schematic of 4-bit SISO Shift Register.

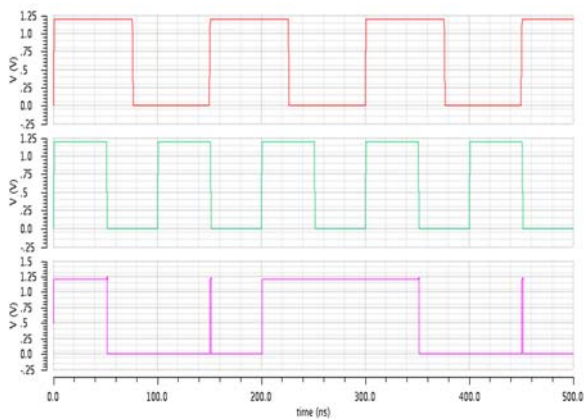


Fig. 5. Transient Response of SISO Shift Register in 90 nm Technology.

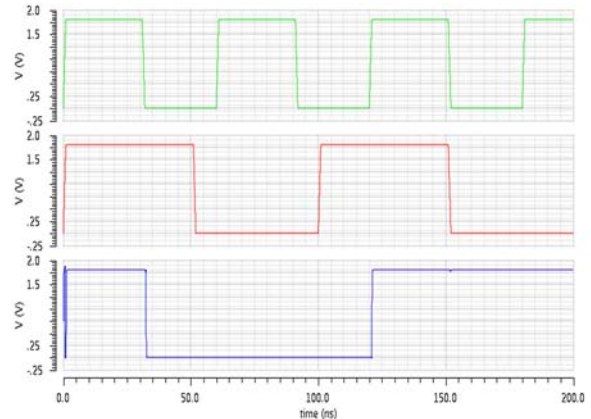


Fig. 6. Transient Response of Shift Register in 180 nm Technology.

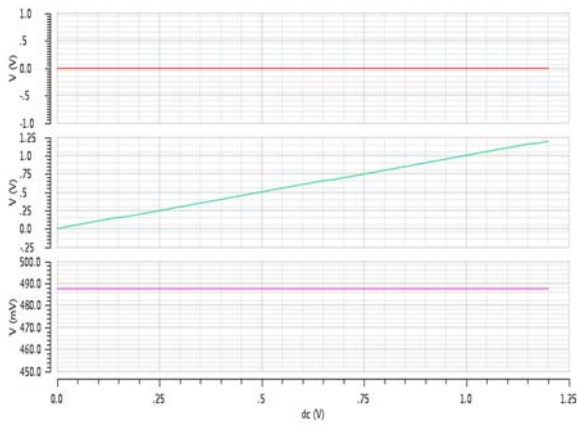


Fig. 7. DC Response of SISO Shift Register in 90 nm Technology.

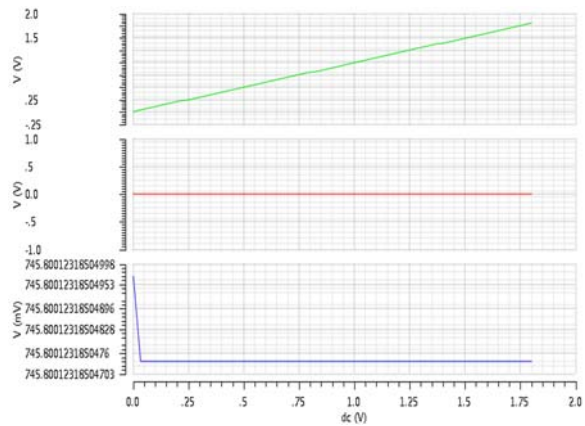


Fig. 8. DC Response of SISO Shift Register in 180 nm Technology.

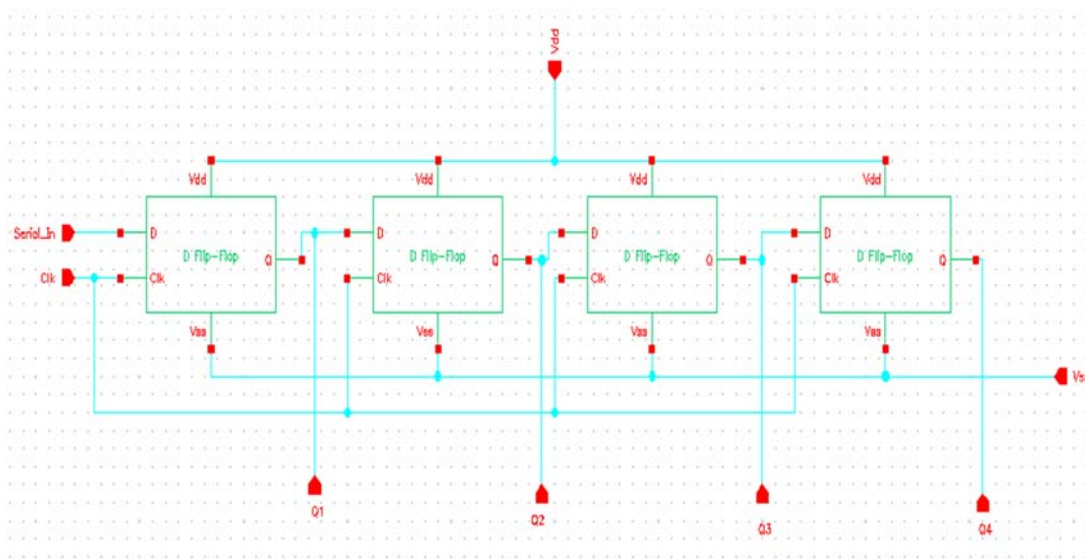


Fig. 9. Schematic of 4-bit SIPO Shift Register.

The logic of developed SIPO register has been verified using analog simulation. The transient responses of proposed SIPO register are shown in Fig. 10 and Fig. 11 for different nanometer technologies.

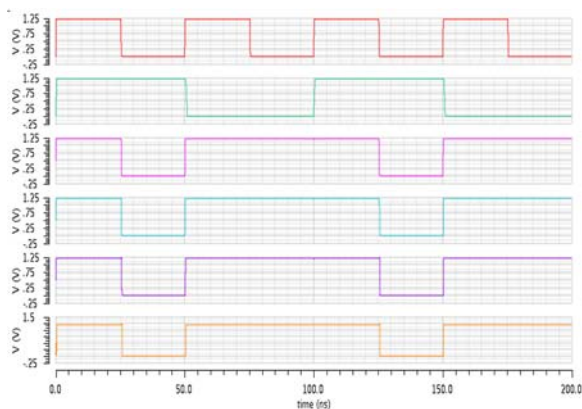


Fig. 10. Transient Response of SIPO Shift Register in 90 nm Technology.

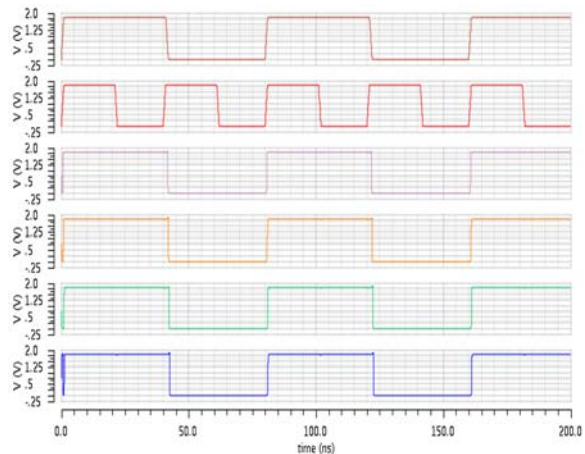


Fig. 11. Transient Response of SIPO Shift Register in 180 nm Technology.

Fig. 12 and Fig. 13 show the DC response of SIPO shift register for 90 nm and 180 nm technology nodes.

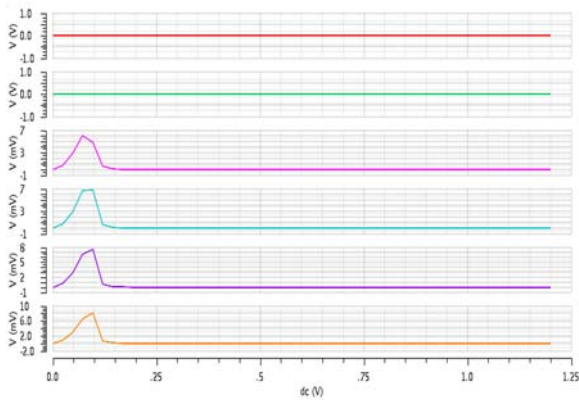


Fig. 12. DC Response of SIPO Shift Register in 90 nm Technology.

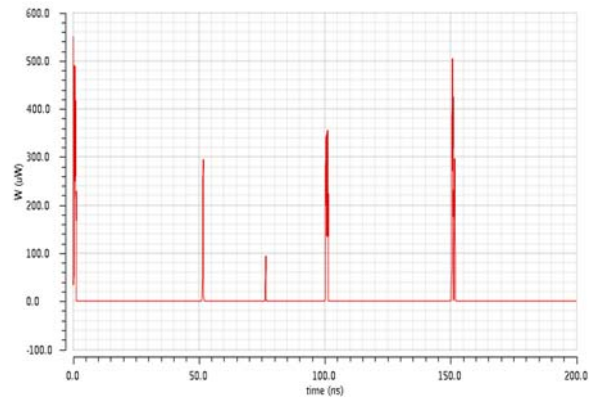


Fig. 15. Power Response of SISO Shift Register in 180 nm Technology.

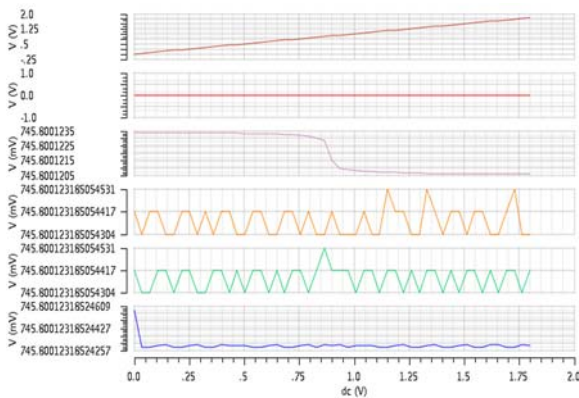


Fig. 13. DC Response of SIPO Shift Register in 180 nm Technology.

#### 4. Performance Analysis

The schematic designs have been simulated for 90 nm and 180 nm technology nodes. Different parameters are taken into consideration for its evaluation. These are Power, Delay and Power-Delay-Product (PDP). The variation of the most essential parameter i.e., power with respect to time can be seen in Fig. 14 and Fig. 15 for SISO shift registers.

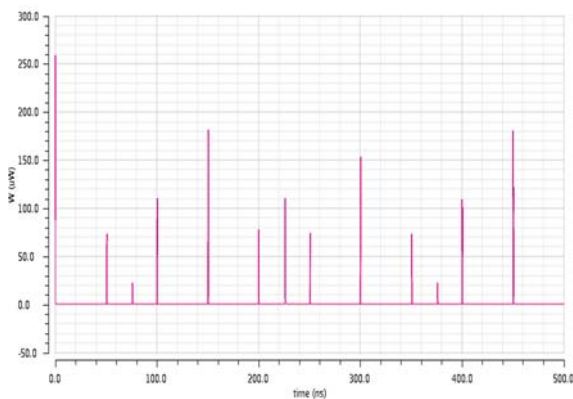


Fig. 14. Power Response of SISO Shift Register in 90 nm Technology.

Table 3 shows the parameter comparison for different technologies. It can be observed from the table that lower the technology node, lesser is the amount of power required by it and faster is the speed as the delay amount decreases significantly.

Table 3. Performance Analysis of Proposed SISO Design.

| Parameter | 180 nm   | 90 nm   |
|-----------|----------|---------|
| Power     | 513 uW   | 161 uW  |
| Delay     | 363.8 ps | 164 ps  |
| PDP       | 186.6 fJ | 26.4 fJ |

The parametric comparisons prove that SISO shift register works more efficiently for the 90 nm node. It thus shows that it consumes much less amount of power as compared to others and with also less amount of delay as well as PDP. The variation of power with respect to time is visualized in Fig. 16 and Fig. 17 for 90 nm and 180 nm technologies for SIPO shift register respectively.

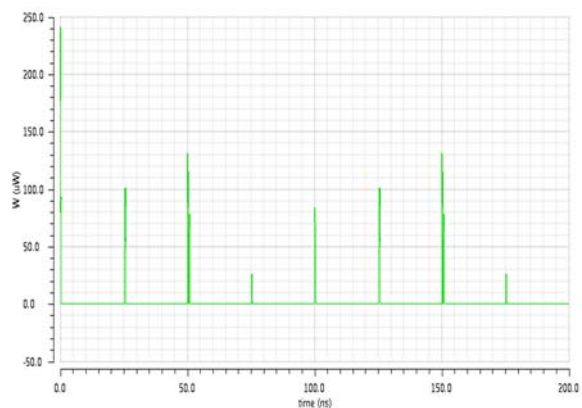


Fig. 16. Power Response of SIPO Shift Register in 90 nm Technology.

Fig. 18 shows that 90 nm design for SISO shift register has an improvement of 68.61 % power with respect to 180 nm technology. Fig. 19 depicts an improvement of 54.92 % delay from 180 nm

technology. Fig. 20 represents that improvisation of 85.85 % in terms of PDP from 180 nm technology.

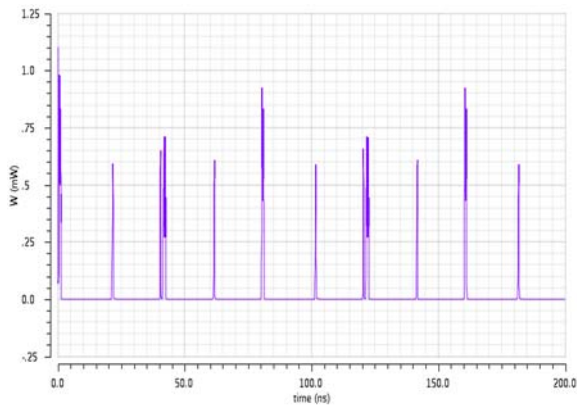


Fig. 17. Power Response of SIPO Shift Register in 180 nm Technology.

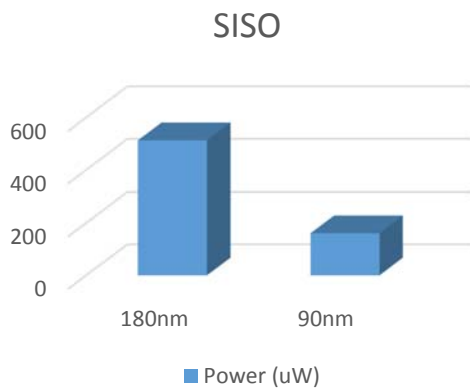


Fig. 18. Graphical comparison of Power consumption.

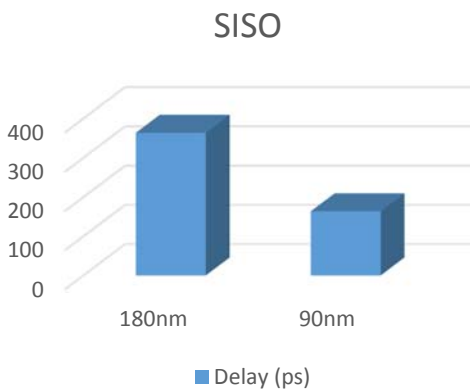


Fig. 19. Graphical comparison of Delay.

Table 4 shows parameter comparison of SIPO shift register for different nanometer technologies.

Fig. 21 shows that 90 nm design for SIPO shift register has an improvement of 67.75 % power with respect to 180 nm technology. Fig. 22 depicts an improvement of 53.32 % delay from 180 nm technology. Fig. 23 represents that improvisation of 84.97 % in terms of PDP with respect to 180 nm technology.

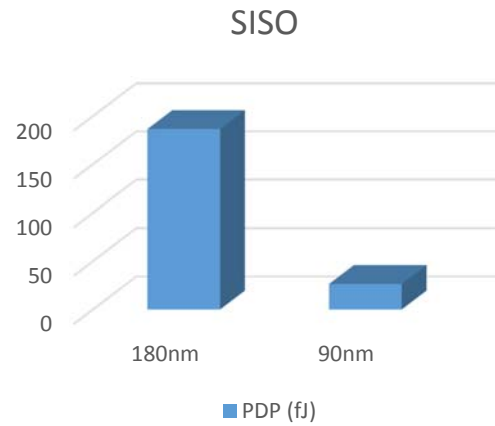


Fig. 20. Graphical comparison of PDP.

Table 4. Performance Analysis of Proposed SIPO Design.

| Parameter | 180nm    | 90nm    |
|-----------|----------|---------|
| Power     | 549 uW   | 177 uW  |
| Delay     | 321.4 ps | 150 ps  |
| PDP       | 176.4 fJ | 26.5 fJ |

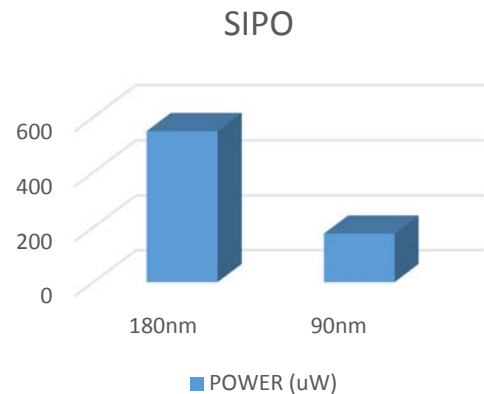


Fig. 21. Graphical comparison of Power.

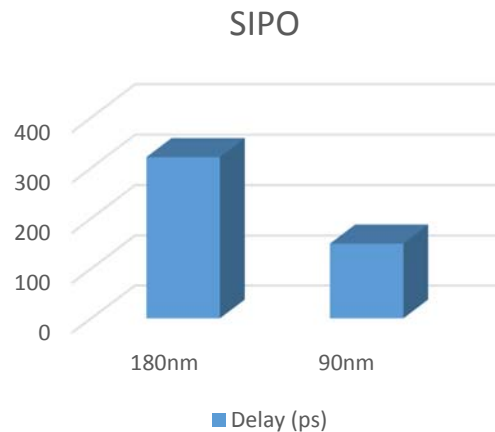


Fig. 22. Graphical comparison of Delay.

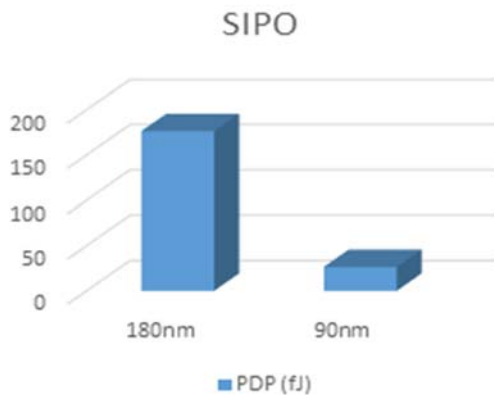


Fig. 23. Graphical comparison of PDP.

## 5. Conclusions

Power and delay optimized 4-bit serial shift registers are designed and analyzed by utilizing the concept of technology scaling. The proposed designs have been developed by using D Flip Flop modules based on optimized NAND gates. 90 nm technology based design shows vast improvement in terms of power, delay and Power-Delay-Product (PDP). The power consumption of 90 nm based SISO design is 161 uW as compared to 513 uW power in case of 180 nm technology. On the other hand 90 nm technology based SIPO design has shown 177 uW power consumption as compared to 549 uW in case of 180 nm technology. The SISO design has shown delay of 164 ps and 363.8 ps for 90 nm and 180 nm technologies respectively. The delay of SIPO based design are 150 ps and 321.4 ps for 90 nm and 180 nm technologies. So 90 nm technology based design show better results in terms of power consumption and delay.

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