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An Ultra-Low Power CMOS-based Temperature Sensor for Implantable Systems

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Abstract: This work presents the design of an ultra-low power temperature sensor based on TSMC 0.18 um CMOS technology which can be utilized in implantable systems. The sensor has a sensitivity of 600 μV/°C over the physiological temperature range of 35 to 40 °C, powered by 0.4 V supply rail and dissipates only around 67 nW of power. The design is also robust against low frequency noise, and has achieved likewise a signal-noise-ratio (SNR) of 51 dB. The MOS transistors have all been biased in sub-threshold. The design has comparable performance to MOS-based implantable temperature sensor designs, and has dissipated the least amount of power.

Keywords: CMOS Temperature Sensor, Sub-Threshold MOS, Ultra-Low Power Circuit.

1. Introduction

Body temperature is a very important parameter that is related to or influences the organ functions. The normal body temperature is around 37 °C. Once this temperature falls below 35 °C, a condition called "Hypothermia" occurs. This can affect the function of the cardiovascular, respiratory and nervous systems [1]. Meanwhile, if the temperature rises to above 40 °C, severe "Hyperthermia" occurs. Prolonged hyperthermia causes the human body to experience heat stress and can cause heat stroke [2]. Continuous monitoring of temperature is essential to the treatment of traumatic brain injury [3]; and has also been utilized for implantable hemodynamic monitoring of patients specifically for valve pressure computations [4].

Some of the systems for temperature sensing include: the implantable cytochrome P-450 molecular biosensor that dissipates 1.4 μW for temperature sensing in the physiological range [5]; the implantable capillary fabricated micro-temperature sensor which featured a temperature sensitivity of 3.84 mΩ/°C in the physiological range [6]; a small-sized and high-sensitivity thermistor (Betatherm) which has a negative temperature coefficient of resistance and has been implanted in animal models [7]; a bioresorbable silicon-based electronic sensor for chronic monitoring of the brain temperature [3]; and fiber optic-based temperature sensors for tissue monitoring during electromagnetic heating for cancer therapy, for patient monitoring during MRI [8].

For chronic monitoring, implantable systems are normally utilized. However, implantable systems can also cause internal localized heating depending on their power density which could be detrimental to the surrounding tissue. The allowable power density of an implantable system at an average should be around 1 mW/cm^2 [5].

The most common implementation of a silicon-based sensor is the vertical PNP transistor whose base-emitter voltage has a Complementary to Absolute

Temperature (CTAT) response slope of -1.6 mV/°C. However, the BJT suffers from several issues most specifically the leakage current which constitutes unnecessary power dissipation. A better solution to this is the use of CMOS-based temperature sensors.

As a design criterion, an implantable chip must dissipate in the sub-μW range [9] with a supply voltage of around 0.5 V. There have been several different CMOS-based circuits that catered for implantable temperature monitoring [9-12]. These involve temperature to frequency sensing [9, 10], ratiometric temperature sensing with ADC interface [11], time to digital temperature sensors where temperature can be calculated using a reference clock and a temperature-dependent frequency or pulse [12], and a MOSFET-based sensing element to translate external temperature into a voltage which incorporates a low power voltage-current converter, and counters [13]. Such circuits feature a power dissipation in the range of sub-μW which is applicable for implantable systems. Two common circuits that generate temperature sensitive responses are shown in Fig. 1. The change in the base-emitter junction potential (ΔV_{BE}) has a proportional to absolute temperature (PTAT) response, whereas the base-emitter barrier potential (V_{BE}) is CTAT. This was achieved since the ΔV_{BE} is proportional to the current (I_{ptat}) ($I_{ptat} = U_T * R * ln(C)$), which has a PTAT response, multiplied to the resistance.

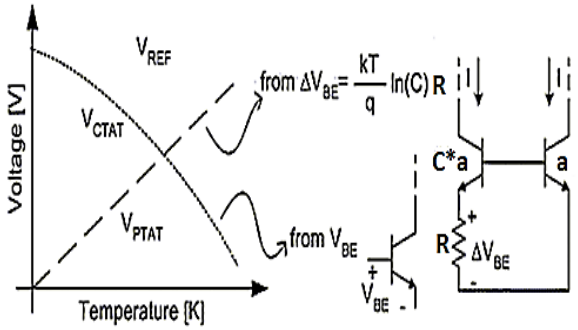

Fig. 1. Bipolar Junction Transistor-based temperature sensors (Note that C is the area multiplier, in reference to a unit area of "a" for the BJT).

In this work, we propose a simple and high performance temperature sensor that is based on sub-threshold MOS devices and has been designed for low power dissipation. The design has been implemented using TSMC 0.18 μm technology obtained from MOSIS wafer test run. LTSPICE was used to simulate the design.

2. The Designed Ultra-Low Power CMOS Temperature Sensor

The implemented circuit is shown in Fig. 2. The circuit consists of the diode connected MOS (M2), the current source MOS driver (M3) that provides the biasing current to M2 to setup its operating condition, MOS capacitors M4 and M6 that form a capacitive voltage divider that biases the current source M3, and the common-source amplifier (M5) with active diode connected load NMOS (M1). The MOS transistors are operated in sub-threshold or weak inversion since the supply rail (V_{DD} = 0.4 V) is much less than the MOS threshold voltage. For the TSMC 0.18 μm process, the NMOS and PMOS transistors have a threshold voltage of 0.6 V and -0.7V, respectively. To filter supply coupled noise that emanates from background biopotential signals, or supply voltage variation, two extra MOS capacitors have been implemented. These MOS transistors are M7 and M8.

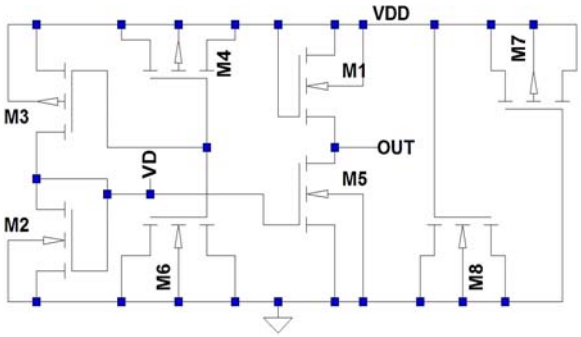

Fig. 2. Self-Extracting temperature sensor based on diode connected MOS and current source amplifier in subthreshold operation.

All the MOS capacitors formed by M4, M6, M7 and M8 have been biased in sub-threshold. In such case the resulting individual capacitances are due to the gate-bulk (C_{GB}), and the overlap capacitances of the gate-source (C_{GS}) and the gate gate-drain (C_{GD}). These capacitances are shown in Fig. 3.

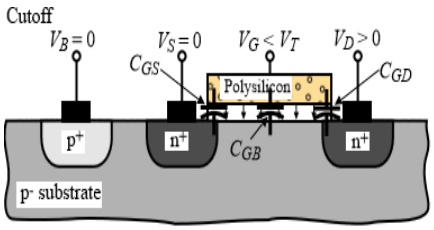

Fig. 3. MOS capacitor in sub-threshold (Cut-off) operating region [14].

The corresponding output capacitances are computed using the following equations:

$$C_{GB} = C_{ox}(W_{eff})(L_{eff}) + 2C_{GBO}(L_{eff}), \quad (1)$$

$$C_{GS} = C_{ox}(LD)(W_{eff}) \approx C_{GSO}(W_{eff}), \quad (2)$$

$$C_{GD} = C_{ox}(LD)(W_{eff}) \approx C_{GDO}(W_{eff}), \quad (3)$$

where LD = 90 nm (lateral diffusion), W_{eff} = effective width of the MOS, L_{eff} = effective length, C_{GDO} = 806 pF/μm (gate-drain overlap capacitance), C_{GBO} = 1 pF/μm (gate-bulk overlap capacitance), C_{GSO} = 806 pF/μm (gate-source overlap capacitance), and C_{OX} = 8.4 fF/ μm^2.

With an MOS having an aspect ratio of 400/0.18 (W_{eff}/L_{eff}), the effective MOS capacitance in subthreshold is thus:

$$C_{total} = C_{GB} + C_{GS} + C_{GD}, \quad (4)$$

which yields: ~ 4.8 pF per MOS capacitor. The MOS capacitors M4 and M6 form a voltage divider that biases the current source M3; whereas, M7 and M8 form the supply noise filter capacitors. Usage of MOS capacitors reduce the overall area budget as compared to using Metal-Insulator-Metal (MiM) capacitors available in the technology.

MOS capacitors are used for this application because they do not dissipate any current from VDD to ground. Furthermore, the MOS cap will have minimal temperature coefficient when in sub-threshold condition due to the non-existence of a depletion area below the gate. The TCF of the overlap capacitances, C_{GSO}, C_{GDO}, C_{GBO} is very minimal in the order of 25 ppm/^{o}C [14].

Meanwhile, the output of the diode connected MOS can be derived using the MOS current in sub-threshold:

$$I_D = I_o exp\left(\frac{V_{GS}}{nU_T}\right)\left(1 - exp\left(\frac{-V_{DS}}{U_T}\right)\right), \quad (5)$$

where n = PN junction emission coefficient, (for Si: 1 – 1.5), U_T = kT/q (thermal voltage), and I_O = subthreshold current (~pA range) with V_{GS} or V_{DS} = 0. With $V_{GS} = V_{DS}$, the equation simplifies to:

$$I_D = I_o exp\left(\frac{V_{GS}}{nU_T}\right)\left(1 - exp\left(\frac{-V_{GS}}{U_T}\right)\right), \quad (6)$$

Obtaining an expression for V_{GS} gives:

$$V_{GS} = U_T\sqrt{n * ln\left(\frac{I_D}{I_O}\right)} \approx U_T\sqrt{ln\left(\frac{I_D}{I_O}\right)}, \quad (7)$$

$$V_{GS} = \frac{kT}{q}\sqrt{ln\left(\frac{I_D}{I_o}\right)} \quad (8)$$

Based from Eqn. (4), the diode connected output (VGS) has a linear response with temperature (T). Since the MOS is N-Channel (NMOS), the charge q is negative. Hence, the negative slope in the temperature response curve of the diode connected MOS which is shown in Fig. 3.

The sub-threshold current (I_D) is provided by M3. To improve on the slope, a common-source gain stage has been included. The small signal voltage gain (A_V) of such amplifier is:

$$A_V = -g_m R_{OUT} = -\frac{g_{m5}}{g_{ds1}+g_{ds5}}, \quad (9)$$

where $g_m = \frac{\partial i_{ds}}{\partial v_{gs}}$ (transconductance), and $g_{ds} = \frac{\partial i_{ds}}{\partial v_{ds}}$ (channel conductance). Using Eqn. (1) to get the g_m and g_{ds}, gives:

$$g_m = \frac{\partial i_{ds}}{\partial v_{gs}} = \frac{\partial}{\partial v_{gs}}\left(i_o exp\left(\frac{v_{gs}}{nU_T}\right)\left(1 - exp\left(\frac{-v_{ds}}{U_T}\right)\right)\right), \quad (10)$$

$$g_m = i_o exp\left(\frac{v_{gs}}{nU_T}\right), \quad (11)$$

$$g_{ds} = \frac{\partial i_{ds}}{\partial v_{ds}} = \frac{\partial}{\partial v_{ds}}\left(i_o exp\left(\frac{v_{gs}}{nU_T}\right)\left(1 - exp\left(\frac{-v_{ds}}{U_T}\right)\right)\right), \quad (12)$$

$$g_{ds} = \frac{\partial i_{ds}}{\partial v_{ds}} = i_o exp\left(\frac{v_{gs}}{nU_T}\right)\left(exp\left(\frac{v_{ds}}{U_T}\right)\right), \quad (13)$$

$$g_{ds} = \frac{\partial i_{ds}}{\partial v_{ds}} = i_o exp\left(\frac{v_{gs}}{nU_T} + \frac{v_{ds}}{U_T}\right) \quad (14)$$

The resulting overall output voltage equation as a function of the thermal voltage U_T by combining Eqns. (8), (9), (11) and (14) is:

$$A_V = \frac{\Delta v_{out}}{\Delta v_{gs}}, \quad (15)$$

$$v_{out} = A_V v_{gs} = -\frac{g_{m5}}{g_{ds1} + g_{ds5}} v_{gs}, \quad (16)$$

$$v_{out} = -\frac{g_{m5}}{g_{ds1}+g_{ds5}}\left(\frac{-kT}{q}\sqrt{ln\left(\frac{I_D}{I_O}\right)}\right), \quad (17)$$

$$v_{out} = \frac{i_o exp\left(\frac{v_{gs}}{nU_T}\right)}{i_o exp\left(\frac{v_{ds1}}{nU_T} + \frac{v_{ds1}}{U_T}\right) + i_o exp\left(\frac{v_{gs5}}{nU_T} + \frac{v_{ds5}}{U_T}\right)} \times \left(\frac{kT}{q}\sqrt{ln\left(\frac{I_D}{I_O}\right)}\right), \quad (18)$$

$$v_{out} = \frac{i_o exp\left(\sqrt{ln\left(\frac{I_D}{I_O}\right)}\right)}{i_o exp\left(2\sqrt{ln\left(\frac{I_D}{I_O}\right)}\right) + i_o exp\left(\sqrt{ln\left(\frac{I_D}{I_O}\right)} + \frac{v_{out}}{U_T}\right)} \times \left(\frac{kT}{q}\sqrt{ln\left(\frac{I_D}{I_O}\right)}\right) \quad (19)$$

3. The Designed Ultra-Low Power CMOS Temperature Sensor Simulation Results

The sensor has achieved a temperature coefficient (TCF) of ~600 µV/ºC which is stable over the physiological temperature range of 35 to 40 ºC as shown in Fig. 4. The response of the diode connected MOS has been improved by the common source amplifier by a factor of -1.6 V/V since the TCF of V_D is -360 µV/ºC. The coefficient is fairly stable over a ± 10 % supply variation. These are shown in Fig. 4.

The simulated temperature resolution of the circuit is around ±0.01 ºC as shown in Fig. 5. The corresponding power dissipation is around 68 nW with a voltage supply rail of 0.4 V.

Meanwhile, the temperature sensor has been verified to have ultra-low noise performance as depicted in Fig. 6. The circuit generates only about 185 nV $\sqrt{Hz}$ of low frequency noise resulting to about a Signal-Noise Ratio (SNR) of ~52 dB. The SNR is computed using Eqn. (20) as follows:

$$SNR\ (dB) = 20log_{10}\left(\frac{v_{out(40)} - v_{out(35)}}{v_{noise(low_{freq})}}\right) \qquad (20)$$

Because of the designed temperature sensor's power dissipation and supply voltage requirement, it can be powered by energy harvested sources such as biochemical reactions, kinetic energy, etc., and thus can function over a long period of time.

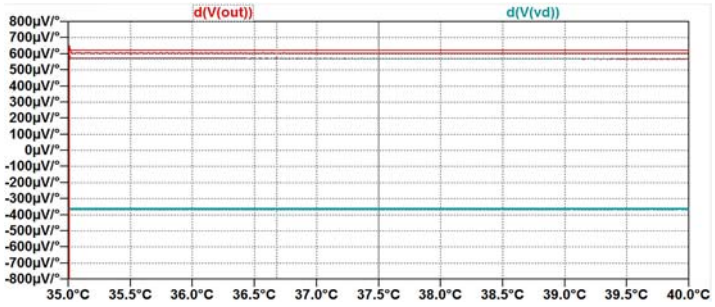

Fig. 4. Temperature sensitivity of the diode connected MOS (V_D), and the complete circuit output (V_{OUT}) versus the physiological temperature range (35 to 40 ºC) and various supply voltages (0.36 V, 0.40 V, 0.44 V).

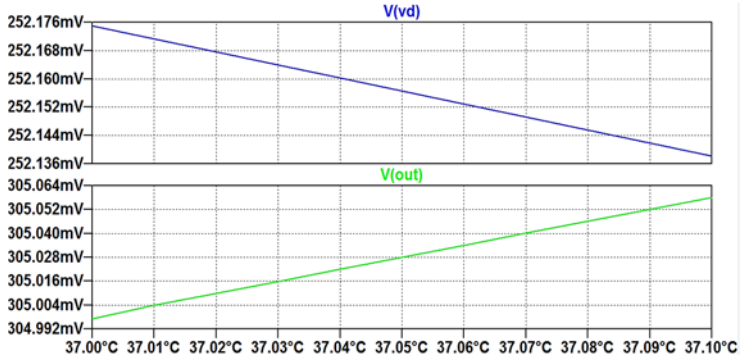

Fig. 5. Responses of the diode connected MOS (V_D), and the complete circuit output (V_{OUT}) versus temperature showing a temp resolution of 0.01 ºC.

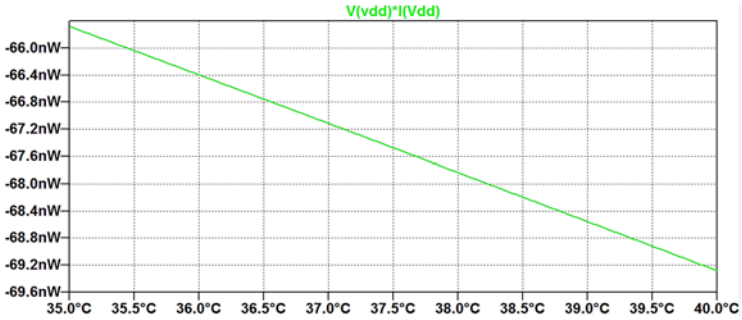

Fig. 6. Circuit power dissipation over the target physiological temperature range.

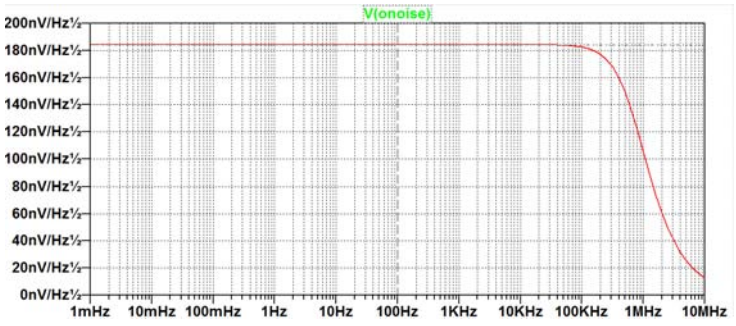

Fig. 7. Noise performance of the CMOS temperature sensor showing the low output referred noise spectrum.

Table 1 shows a comparison of the achieved performance specification for benchmarking our design. Our design has comparable performance results based on resolution and TCF. Our design has achieved an even low power dissipation. Meanwhile Table 2 lists the aspect ratios of the MOS devices used in the design.

Table 1. Performance Specifications Benchmarking.

No.	[12]	[10]	[9]	This Work
Technology	0.18 µm	65 nm	0.18 µm	0.18 µm
Power Dissipation	119 nW	100 µW	290 nW	~67 nW (simulation)
Resolution	+1/-0.8°C	1°C	0.5°C	0.01°C (simulation)
Temp. Sensing Range	-10 to 30°C	30 to 50°C	0 to 50°C	0 to 75°C (within +/- 5 % droop)
Supply Voltage	0.5 V	0.7 V	0.5 V	0.4 V

Table 2. MOS Aspect Ratios and Functions.

MOS transistor	Width	Length	Multiplier	Function
M2	20 µ	0.18 µ	2	Diode connected Sensor
M3	5 µ	0.18 µ	1	Bias current source
M4	20 µ	0.18 µ	20	PMOS cap voltage divider
M6	20 µ	0.18 µ	20	NMOS cap voltage divider
M5	5 µ	0.18 µ	1	Common source amplifier
M1	20 µ	0.18 µ	20	Common source amplifier load
M7	20 µ	0.18 µ	40	Supply Filter Cap
M8	20 µ	0.18 µ	40	Supply Filter Cap

4. Conclusion

This work was able to present the design of an ultra-low power temperature sensor based on TSMC 0.18 µm CMOS technology which can be utilized in implantable systems. Simulation results show that the sensor has a comparable power dissipation, resolution and range as compared to literature. The sensor has achieved a TCF of 600 µV/°C over the physiological temperature range of 35 to 40°C, powered by 0.4 V supply rail and dissipates only around 67 nW of power. The design is also robust against low frequency noise, and has achieved likewise a signal-noise-ratio (SNR) of 51 dB.

Recommendation

It is recommended for further studies to verify if such design is scalable to other technology nodes.

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