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An Efficient Method for Extraction of Transfer Function of H-Tree Clock Distribution Networks

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Abstract: An efficient derivation methodology is proposed for extracting general transfer function of H-Tree clock distribution network. This is an accurate, fast and simple method to determine transfer function of any balanced tree structures with branching factor of two. This approach is caused a highly accurate and simple method to evaluate the 50 % propagation delay at output nodes of the binary balanced trees. *Copyright © 2009 IFSA.*

Keywords: Transfer function, H-Tree clock distribution network, Binary balanced trees, Propagation delay

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1. Introduction

In deep sub-micron VLSI technology, clock distribution network has become an increasingly challenging problem for VLSI designs and careful design of clock networks is essential in high-performance VLSI circuits. Clock network distributes the clock signal from the clock source to the local sink nodes on a chip. The design of the clock network determines the clock frequency and the behavior of the synchronized circuits on a chip. A clock distribution network is often structured as a balanced tree [1].

As technology advances, the delays of transistors and local interconnect scale down. As a result, the local clock frequency is projected to increase significantly [2], [3]. Global interconnects delay of clock distribution network increases with technology scaling because their lengths do not scale. In fact, since the chip size and the number of transistors are projected to increase, the length and number of global interconnects will increase. Consequently, the global interconnect lines will be the limiting blocks of overall performance of a system-on-a-chip [4]. In order to achieve improvement in circuits design, accurate method for calculating global interconnects delay is very important. A clock distribution network is often structured as a balanced tree.

The paper is organized as follows. In section 2, the methodology for extraction of transfer function of H-tree structures is described. The objective of section 3 is comparison the results from our method with HSPICE simulations. Finally, some conclusions are offered in section 4.

2. Methodology

One of the most common structures in clock distribution networks are H-tree structures. Fig. 1 shows an H-tree clock distribution in two levels. In each technology, the first and the second levels at top of any metal layers are separated. The first level is in a higher metal layer than the second one. Note that the input source voltage can see two parallel and equal loads from its left and right hand side that is connected to the central node of the H-tree structure.

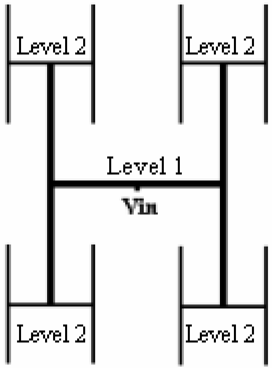

Fig. 1. Two-level H-tree Structure.

Because of the symmetry of the H-tree structure, it can be divided in two halves, each half is equivalent to a binary balanced trees. A balanced tree is a tree where the impedances of the sections that constitute each level are equal, making the paths to the all sinks identical. Therefore this structure has an equal delay in all of its output nodes. A balanced tree with a binary branching factor and n levels has 2^n-1 branches. In the two-level H-tree structure, each half transfers to four-level binary balanced trees with 15 branches. For half of the structure shown in Fig. 1, we can assume a four-level balanced tree structure as of Fig. 2 where a driver with an output resistance R_d is connected to the root of the tree N_0. All of the output nodes are called leaves and connected with load buffers which can be used to drive the trees in the next level. The load buffers are modeled by capacitors. All of the branches in the tree are represented by distributed RLC transmission lines.

It is obvious for calculating the delay at the output nodes, we need to find the transfer function between the output node and the input source node. We derive the transfer function of all of the branches along the unique path from the voltage source to an output node concerning the load impedance at the far end of each branch. By multiplying all of these transfer functions we can reach to the general transfer function for the whole system.

Each interconnect branch is represented by a distributed RLC transmission line, where l is the interconnect length, and R, L, and C are the resistance, inductance, and capacitance per unit length, respectively [5]. The load at the far end of branch is Z_L. The transfer function of a single branch is

$$H(s) = \frac{1}{\cosh\theta + (Z_c/Z_L)\sinh\theta}, \tag{1}$$

where Z_c and θ are the characteristic impedance and propagation constant of the branch and are given by

$$Z_c = \sqrt{\frac{L}{C}}\sqrt{1+\frac{R}{sL}} \tag{2}$$

$$\theta = sl\sqrt{LC}\sqrt{1+\frac{R}{sL}} \tag{3}$$

The transfer function from the voltage source to an output node is the product of the transfer function of all of the branches along the unique path from N_0 to the output node. It can be shown that the transfer function is obtained as

$$H(s) = \frac{\frac{Z_{in,N_0}}{2}}{R_d + \frac{Z_{in,N_0}}{2}} \prod_k \frac{1}{\cosh\theta_k + (Z_{c,k}/Z_{L,k})\sinh\theta_k} = \frac{Z_{in,N_0}}{2R_d + Z_{in,N_0}} \prod_k \frac{1}{\cosh\theta_k + (Z_{c,k}/Z_{L,k})\sinh\theta_k} \tag{4}$$

where $Z_{in,N0}$ is the input impedance seen from N_0, and k is the index covering each branch in the path from N_0 to the output node. To clarify the reason behind including resistance $2R_d$ in Fig. 2, notice that because of dividing the voltage in the root of the tree, we have to multiply the transfer function of the tree by the coefficient which can be observed in (4). $Z_{in.N0}$ is equivalent to the visible load from N_0 in the left and the right side. After removing any half, for considering the its loading effect, we halve $Z_{in.N0}$ which is equivalent to doubling the output resistance of driver and removing the other half.

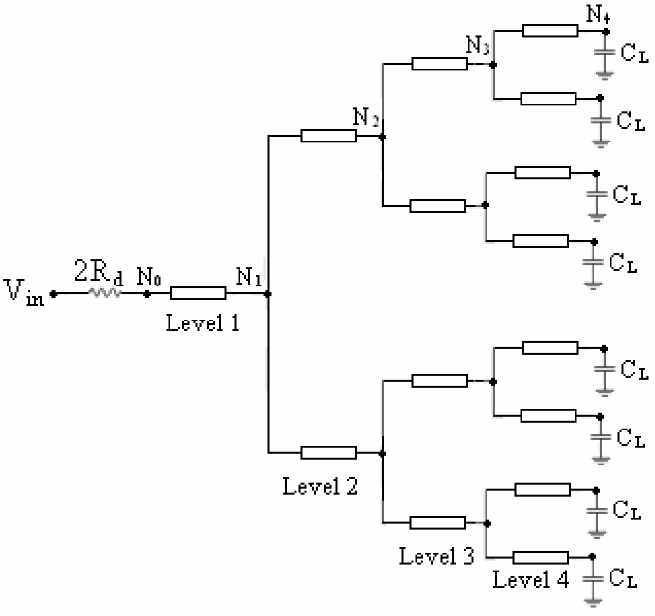

Fig. 2. Four-level binary balanced tree.

For the branch of level k with load $Z_{L,k}$ at the far end, the input impedance seen from the near end of branch is [5]

$$Z_{in,k} = Z_{c,k}\frac{Z_{L,k} + Z_{c,k}\tanh\theta_k}{Z_{c,k} + Z_{L,k}\tanh\theta_k} = \frac{\cosh\theta_k + Z_{c,k}\sinh\theta_k / Z_{L,k}}{\cosh\theta_k / Z_{L,k} + \sinh\theta_k / Z_{c,k}} \tag{5}$$

$Z_{c,k}$ and θ_k are the characteristic impedance and propagation constant of the branch of level k. For a node with multiple fanout, the load impedance seen at this node is the parallel combination of the input impedance of the downstream branches which are connected to this node.

Load impedance at the far end of entire branch is equal with half of input impedance in near end of next line. Therefore for the n-level binary balanced tree that output nodes connected to C_L can be written

$$Z_{L,k} = Z_{in,N_{(k-1)}} = \frac{Z_{in,(k+1)}}{2} \qquad k = (n-1),\ldots,1 \tag{6}$$

$$Z_{L,n} = \frac{1}{sC_L} = Z_L, \tag{7}$$

where $Z_{L,n}$ is the branch load impedance of level n.

By referring to the transfer function in (4) and using the expressions (5), (6) and (7), the general transfer function is defined

$$H = \frac{1}{(2r_d)B_1 + A_1}, \tag{8}$$

where

$$A_{k-1} = A_k\cosh\theta_{k-1} + 2B_kZ_{c,k-1}\sinh\theta_{k-1} \quad (k = n:2) \tag{9}$$

$$B_{k-1} = A_k\frac{\sinh\theta_{k-1}}{Z_{c,k-1}} + 2B_k\cosh\theta_{k-1} \qquad (k = n:2) \tag{10}$$

A_n and B_n , relative to the branch of level n are defined by

$$A_n = \cosh\theta_n + \frac{Z_{c,n}\sinh\theta_n}{Z_L} \tag{11}$$

$$B_n = \frac{\cosh\theta_n}{Z_L} + \frac{\sinh\theta_n}{Z_{c,n}} \tag{12}$$

We can see that the equations (9), (10), (11) and (12) consist the three factors, $\cosh\theta$, $Z_c\sinh\theta$ and $\sinh\theta/Z_c$. Since (9), (10), (11) and (12) includes hyperbolic function of the complex frequency s, the inverse Laplace transform is difficult to drive directly.

To calculate the delay of binary balanced tree structures, its exact transfer function should be converted to an equation containing polynomials in powers of s. In order to simplify the problem, these factors are expressed as a series in the powers of s. In this work, we consider the expansion of three mentioned factors once to the power of s^2 and in another time to the power of s^4, and in each time we calculate the delay by substituting in the exact transfer function. Series expansion of mentioned factors are obtained as

$$\begin{aligned}\cosh(\theta) &= 1+\frac{1}{2!}l^2RCs+(\frac{1}{2!}l^2LC+\frac{1}{4!}l^4R^2C^2)s^2+\\&(\frac{2}{4!}l^4RLC^2+\frac{1}{6!}l^6R^3C^3)s^3+(\frac{1}{4!}l^4L^2C^2+\frac{1}{8!}l^8R^4C^4+\frac{3}{6!}l^6R^2LC^3)s^4+\ldots\end{aligned} \tag{13}$$

$$\begin{aligned}Z_c\sinh(\theta' l) &= lR+(lL+\frac{1}{3!}l^3R^2C)s+(\frac{2}{3!}l^3RLC+\frac{1}{5!}l^5R^3C^2)s^2+\\&(\frac{1}{7!}l^7R^4C^3+\frac{1}{3!}l^3L^2C+\frac{3}{5!}l^5R^2LC^2)s^3+(\frac{3}{5!}l^5RL^2C^2+\frac{4}{7!}l^7R^3LC^3+\frac{1}{9!}l^9R^5C^4)s^4+\ldots\end{aligned} \tag{14}$$

$$\begin{aligned}\frac{1}{Z_c}\sinh(\theta) &= lCs+\frac{1}{3!}l^3R\ C^2s^2+(\frac{1}{3!}l^3LC^2+\frac{1}{5!}l^5R^2C^3)s^3+\\&(\frac{2}{5!}l^5RLC^3+\frac{1}{7!}l^7R^3C^4)s^4+\ldots\end{aligned} \tag{15}$$

According to the order in which we do the expansion in addition to number of levels in a tree structure, the order of the denominator of general transfer function will change. For example, for a four level tree structure that its branches factors are expanded to power of s^2, considering the output load of $Z_L=1/sC_L$, the denominator of the net transfer function will be from power of nine. Attention that all of effects and features of the interconnects and loading effects are considered in the coefficients of powers of s in the denominator of transfer function. Since the second-order approximation for tree structures has an acceptable accuracy [5], so, the net transfer function can be approximated with a system of power of two. Attention that in this approximation, all of effects and features of the interconnections and loadings are considered as coefficient of powers of s and s^2.

3. Results and Examples

An exponential input signal that more accurately characterizes the signals in VLSI circuits is applied to the two-level H-tree clock network. In this example, the interconnect parameters are specified in Table 1 for technology nodes of 180 nm, 70 nm and 60 nm [7]. Also the input signal parameters are τ=50 ps and V_{dd}=1 V. The driver resistance and load capacitances are R_d = 10 Ω and C_L =150 fF. The Table 1 shows the propagation delay time at output nodes. The propagation delay time is defined as the maximum time from the input crossing 50 % to the output crossing 50 %. In each of Fig. 3, Fig. 4 and Fig. 5 are compared the time-domain response of output voltage from the general transfer function with HSPICE simulation at different technology.

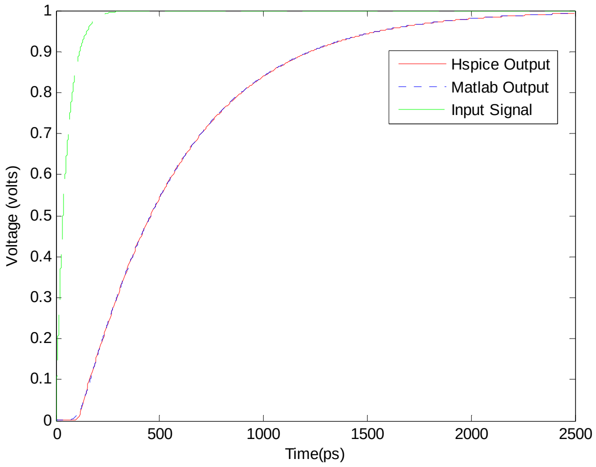

Fig. 3. Comparison of Output Response from General Transfer Function and with HSPICE (Technology Node: 180 nm).

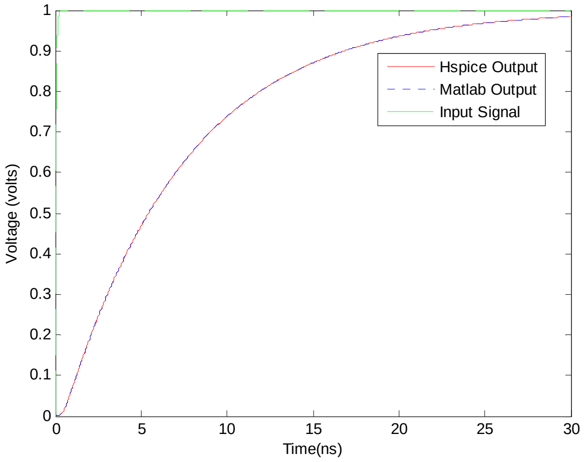

Fig. 4. Comparison of Output Response from General Transfer Function and with HSPICE (Technology Node: 70 nm).

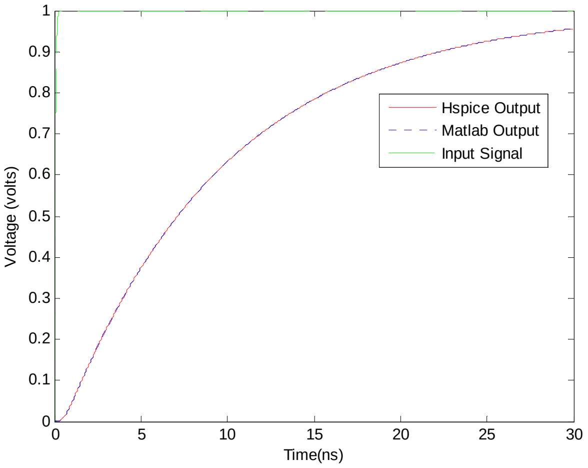

Fig. 5. Comparison of Output Response from General Transfer Function and with HSPICE (Technology Node: 65 nm).

Table 1 shows the high accuracy of the proposed general transfer function by comparing the delay calculation results with HSPICE simulation. Therefore, the general transfer function has an acceptable level of accuracy.

Table 1. Comparison of the Propagation Delay from Our General Transfer Function with HSPICE.

Technology Node	Level 1	Level 2	Level 3	Level 4	50 % Propagation Delay (ps)			Error Percentage	
					HSPICE	Our General Transfer Function			
						Series Expansion of Factors up to s^2	Series Expansion of Factors up to s^4	Series Expansion of Factors up to s^2	Series Expansion of Factors up to s^4
180 nm	l=5 mm	l=5 mm	l=2.5mm	l=2.5 mm	421.52	421.3	425	0.05 %	0.8 %
	w=860nm	w=860nm	w=80 nm	w=800nm					
	t=1720nm	t=1720nm	t=1600nm	t=1600nm					
70 nm	l=5mm	l=5mm	l=2.5mm	l=2.5mm	5399.8	5400	5400	0.003 %	0.003 %
	w=185nm	w=185nm	w=125nm	w=125nm					
	t=370nm	t=370nm	t=250nm	t=250nm					
65 nm	l=5mm	l=5mm	l=2/5mm	l=2.5mm	7095.3	7096	7096	0.01 %	0.01 %
	w=150nm	w=150nm	w=105nm	w=105nm					
	t=315nm	t=315nm	t=220.5nm	t=220.5nm					

4. Conclusions

The obtained equation for transfer function of H-tree Structure is a general and comprehensive equation without any approximation. To determine the delay of this structure, its exact transfer function should be converted to an equation containing polynomials in powers of s. To do this work, we consider series expansion of each branch factors up to s^2. So, we can see that the transfer function of n-level tree structure is of degree 2n+1 and have highest accuracy to calculate the delay. The coefficients of powers of s in the denominator of transfer function are affected from the whole structure. Future work includes the second-order approximation of general transfer function.

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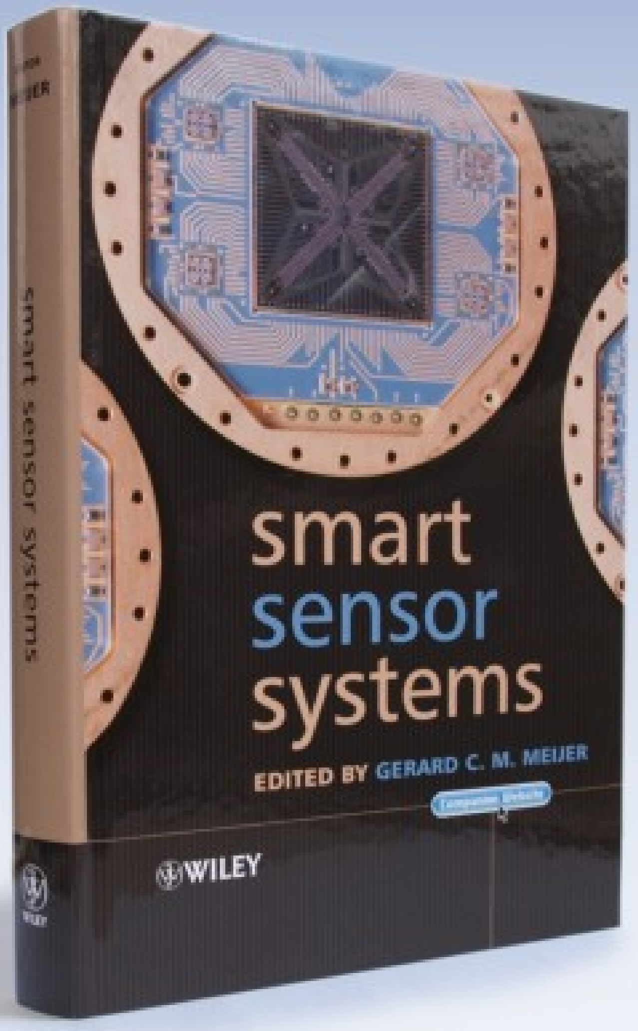

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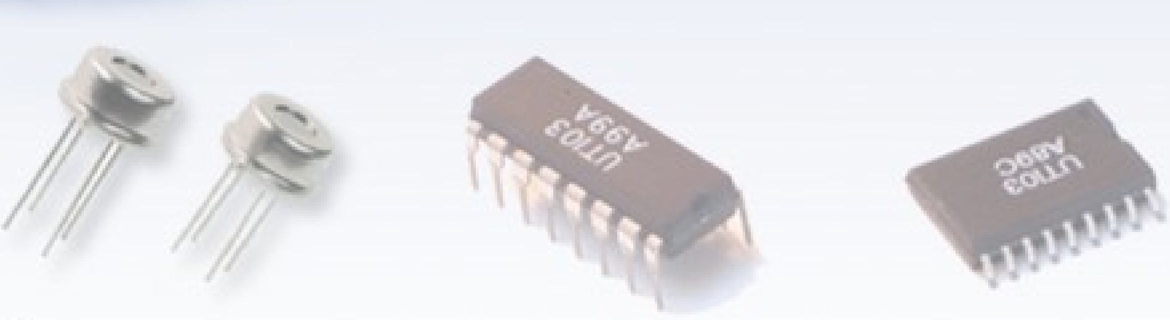

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