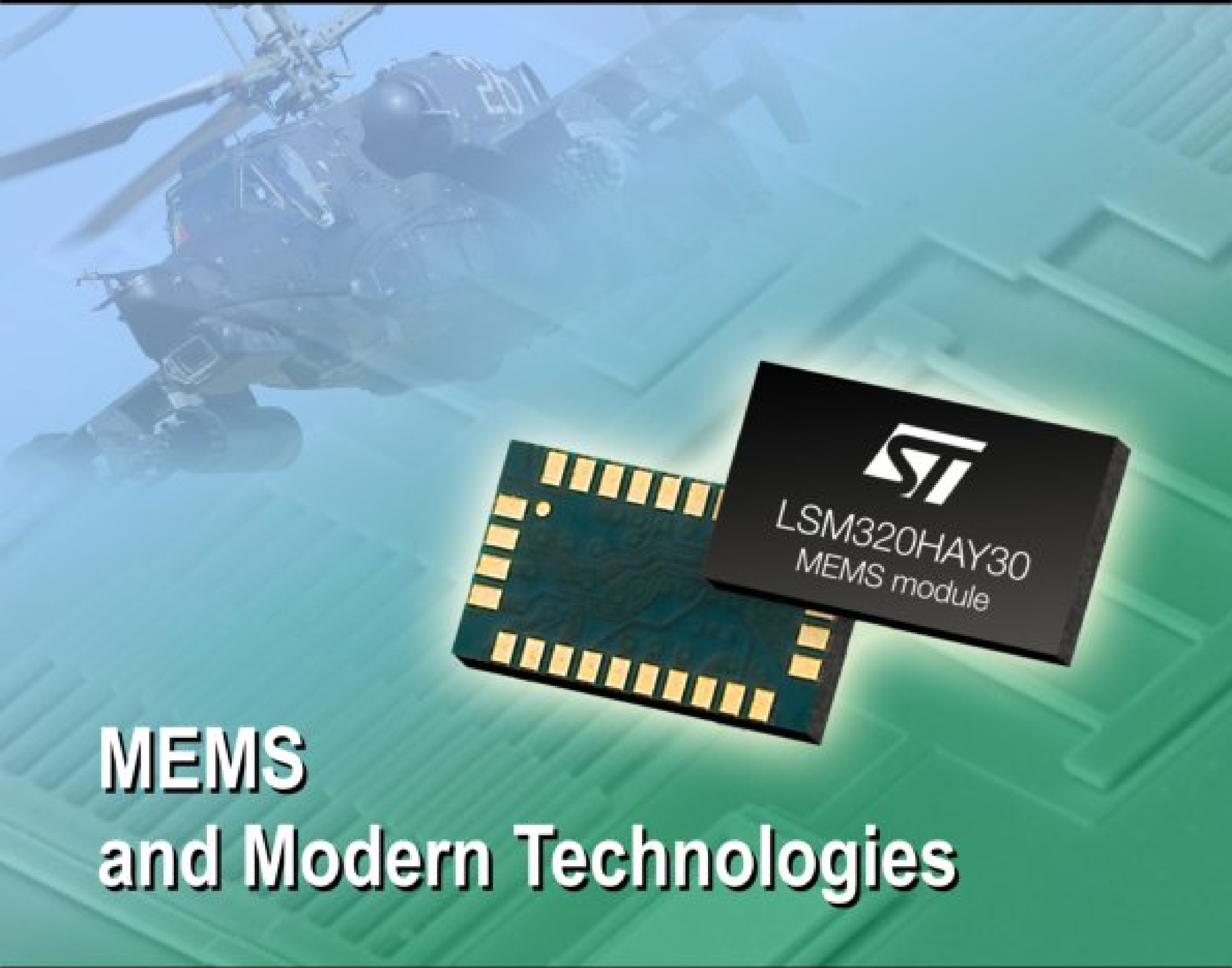
ISSN 1726-5479

# SENSORS & TRANSDUCERS

vol. 139
4/12



## MEMS and Modern Technologies

International Frequency Sensor Association Publishing

# Sensors & Transducers

**Volume 139, Issue 4,**
**April 2012**
**www.sensorsportal.com**
**ISSN 1726-5479**

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**Sensors & Transducers Journal**

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**Volume 139**
**Issue 4**
**April 2012**

**www.sensorsportal.com**

**ISSN 1726-5479**

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*Sensors & Transducers Journal, Vol. 139, Issue 4, April 2012, pp. 1-23*

**Sensors & Transducers**

**ISSN 1726-5479**

*http://www.sensorsportal.com*

# MEMS Non-Silicon Fabrication Technologies

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*Received: 31 March 2012 /Accepted: 23 April 2012 /Published: 30 April 2012*

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**Abstract:** MEMS technology, due to their potential of compactness and negligible DC-power consumption, has found applications in every field such as communication, automation, navigation, bio-sensors etc. MEMS technology has created the feasibility of making monolithic systems which was not feasible with VLSI technology. Initially MEMS devices were developed using Silicon micromachining. Since a decade, research is being carried out to explore non-Silicon fabrication technologies for MEMS. Various non-Silicon fabrication technologies such as printed circuit board (PCB), low temperature co-fired ceramic (LTCC) and liquid crystal polymers (LCP) in addition to new upcoming technologies such as polymer core conductor and polydimethylsiloxane (PDMS) are being explored to realize MEMS. This paper presents substrate materials with their characteristics, fabrication process and application for these non-Silicon fabrication micromachining technologies.

***Keywords:*** Printed circuit board, Low temperature cofired ceramics, Liquid crystal polymers, Polymer core conductor, Poly-dimethyl siloxane, Microsystem, MEMS.

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## 1. Introduction

Recently, MEMS technology has emerged as a revolutionary technology to realize sensors, communication systems, biosensors, etc. Because Silicon micromachining is a mature technology, MEMS are preferred to be fabricated on Silicon. Silicon technology is most suitable for VLSI because of its high accuracy in achieving small dimensions, but we don't need small features with high precision in MEMS technology.

Since years, research is being carried out to develop MEMS non-Silicon fabrication technologies such as printed circuit board (PCB), low temperature cofired ceramics (LTCC), liquid crystal polymers (LCP), polymer core conductor and poly-dimethyl siloxane (PDMS). There are many groups working on MEMS non-Silicon fabrication technologies. Pagel et al [1] reported microfluidic microsystems using multilayer stacks, Goel et al [2] and Ramadoss et al [3] has demonstrated monolithic phased antenna array, Ghodsian et al reported RF MEMS switch [4], Cetiner et al explored tunable antenna [5] on printed circuit board using PCB micromachining processes. Golonka group at Wroclaw University of Technology has explored MEMS and MEMS sensors [6], Gongora-Rubio et al manufactured meso-scale EMS (electro-mechanical system) thermal flow sensor [7] on LTCC substrate. Reconfigurable phased antenna array [8, 9], RF modules [10-13] and MEMS sensors [14, 15] has been reported using liquid crystal polymer (LCP) technology. In polymer core conductor technology, polymer core is coated with metal which is more favourable for RF MEMS applications. It is due to skin effect in which most of the current is confined to outermost portions of the conductor. Passive RF modules such as spiral and solenoid inductor structures, transformer, co-axial core inductor [16, 17] have been reported using polymer core conductor technology. PDMS is being considered for microfluidic MEMS which are most suitable for bio applications [18], microfuel cell array [19]. Many fabrication processes has been developed for these technologies depending on the substrate material characteristics; but still there is need to develop improved & cost effective fabrication processes.

This paper provides an insight on substrate materials and their characteristics, and micro-fabrication processes for each of non-Silicon fabrication technologies of PCB, LTCC, LCP, polymer core conductor and PDMS technology. A brief overview of their applications in MEMS and RF MEMS is also provided.

## 2. Printed Circuit Board (PCB) Technology

Printed circuit board (PCB) was originated in 1904 by Frank Sprague, but it was commercially used 50 years later. PCB is made of thin dielectric base material coated with conductor on both sides. Base dielectric provides mechanical support to electrical circuits as well as components and coated conductor is used to make electrical contacts. Copper is preferred conductor in PCB technology due to its high electrical conductivity [20, 21]. There are different resins being used as PCB dielectric. Some of the PCB base materials with their dielectric properties are listed in Table 1.

**Table 1.** PCB base materials.

| PCB base materials | Glass transition temperature (Tg)°C | Dielectric constant $\varepsilon_r$ | Loss tangent tanδ | Dielectric strength (V/mil) |
|---|---|---|---|---|
| Alumina | 1700 | 4.5 | - | 220 [22] |
| *FR4 epoxy | 125 | 4.1 | 0.02 | 1100 [20] |
| Multifunctional epoxy | 145 | 4.1 | 0.022 | 1050 [20] |
| Tetra-functional epoxy | 150 | 4.1 | 0.022 | 1050 [20] |
| *BT/Epoxy | 185 | 4.1 | 0.013 | 1350 [20] |
| Cyanate Ester | 245 | 3.8 | 0.005 | 800 [20] |
| Polyimide | 285 | 4.1 | 0.015 | 1200 [20] |
| Teflon | NA | 2.2 | 0.0002 | 450 [20] |
| Flourene based resin | 230 | 3.2 | 0.002 | 5000 [23] |

*FR4: Diglycidyl ether of tetrabromobisphenol A
*BT: Bismaleimide trazine

Initially, PCB substrates were used only for electronic circuitry. Recently, fabrication of MEMS using PCB technology is reported due to low cost fabrication equipments and ease of micromachining technology. Advantages of using PCB technology over Silicon technology for MEMS are listed below:

1. Manufacturing cost of PCB substrates is low compared to conventional semiconductor substrates such as Silicon or Gallium Arsenide.
2. PCB technology does not need high class clean room and sophisticated fabrication equipments like conventional semiconductor technology.
3. PCB substrate is compatible with organic substrate which makes it suitable for MCML (Multi Chip Module Laminate) technology [15].
4. Packaging is required to protect the MEMS device against environmental harsh conditions. Packaging of MEMS fabricated with Silicon micromachining is still a critical issue. Mostly, MEMS packaging cost is high or comparable to the device fabrication cost. Packaging related issues and package cost can be avoided with PCB technology because in this, substrate itself acts as a package.
5. PCB substrates of different thicknesses and wide range of dielectric constants with low loss tangents are commercially available. These properties make it suitable for RF MEMS components.
6. PCB fabrication utilizes multilayer technology which makes it highly economic process. All layers are patterned individually and aligned using alignment marks. An epoxy of certain viscosity [1, 24, 25] is used to bond all layers under certain temperature and pressure [24, 25] which is a low cost process compared to the Silicon wafer bonding which needs very sophisticated and expensive equipments.

Disadvantages of PCB Technology:

1. Surface roughness of PCB copper clad is high which limits the fabrication to attain minimum feature size.
2. PCB substrate cannot be used for devices which need to be exposed to high temperatures.

### 2.1. Fabrication Processes for PCB Technology

Silicon technology fabrication processes cannot be used for PCB technology because PCB substrate cannot sustain at high temperature. PCB fabrication processes are low temperature (<250 ºC) processes. Fabrication processes reported for PCB technology are discussed:

#### 2.1.1. Thin Film Deposition

Deposition is one of the high temperature processes of Silicon micro-fabrication. A low temperature deposition process of high density inductively coupled plasma chemical vapor deposition (HDICP CVD), which is developed specifically for PCB substrates.

High Density Inductively Coupled Plasma Chemical Vapor Deposition (HDICP CVD) [26]: Chemical vapor deposition (CVD), Plasma Enhanced chemical vapor deposition (PECVD) and other conventional deposition techniques are high temperature processes and cannot be used for PCB substrate. A low temperature (90 ºC -170 ºC) deposition process of high density inductively coupled plasma chemical vapor deposition (HDICP CVD) technique is reported specific for PCB substrates.

HDICP CVD utilizes high density plasma of $10^{10}$-$10^{11}$ ions/cm$^3$ place of plasma density used in PECVD of $10^9$ ions/cm$^3$. HDICP CVD method uses a commercially available inductively coupled plasma (ICP) reactor (Bethel Materials Research, Irvine, CA) to inductively couple RF power, with designed antenna array and a set of magnets with Faraday shield copper tapes wrapped around them to increase the plasma density and to adjust the plasma profile. HDICP CVD is being used to deposit $SiN_x$ on PCB substrate. It uses $SiH_4$+$N_2$ (in palce of $NH_3$), less hydrogen reactants which deposits high dielectric properties $SiN_x$. Comparison between HDICP CVD and PECVD processes and deposited film characteristics are listed in Table 2 [26].

**Table 2**. Comparison between Silicon nitride film deposited by PECVD and HDICP CVD [26]. Reproduced from H.-P. Chang, J. Qian, B. A. Cetiner, F. D. Flaviis, M. Bachman, Design and process considerations for fabricating RF MEMS switches on printed circuit boards *Journal of Microelectromechanical Systems* 14 no. 6 pp. 1311-1322, (2005) © IEEE.

| **Process parameters** | **PECVD** | | **HDICP CVD** | |
|---|---|---|---|---|
| Process gases | SiH4:NH3:N2 | SiH4:NH3:N2 | SiH4:N2 | SiH4:N2 |
| Process temperature | 250 ºC | 300-400 ºC | < 190 ºC | < 100 ºC |
| Wet etch rate in BHF (Aº/min) | 600-650 | 200-300 | 50 | 200-300 |
| Concentration | >25@% | 2025@% | <15@% | <20@% |
| Film stress (MPa) | 100-600 (compressive) | 100-800 (compressive) | 150-600 (compressive) | 100-800 (compressive) |
| Surface roughness(nm) | 2.5 | 3.1 | 2.0 | 1.6 |
| Dielectric strength (MV/cm) | ~8 | ~8 | >9 | >9 |

### 2.1.2. Planarization

PCB uses thick metal clad layers which make the surface rough. Couples of surface planarization techniques are mentioned below to improve its surface profile for successive processes. PCB substrates are commercially available with Copper clad of 18 µm to 105 µm thickness deposited on 100 µm to 1500 µm thick base [24] where large thickness of copper clad causes rough surface. In some cases, because of this copper clad surface roughness, reliability and working performance of the devices is significantly impaired. To reduce the surface roughness of copper clad, techniques adopted are called as planarization techniques. Some of these are:

a. Polishing and planarization;
b. Compressive molding planarization (COMP).

#### 2.1.2.1 Polishing and Planarization Process

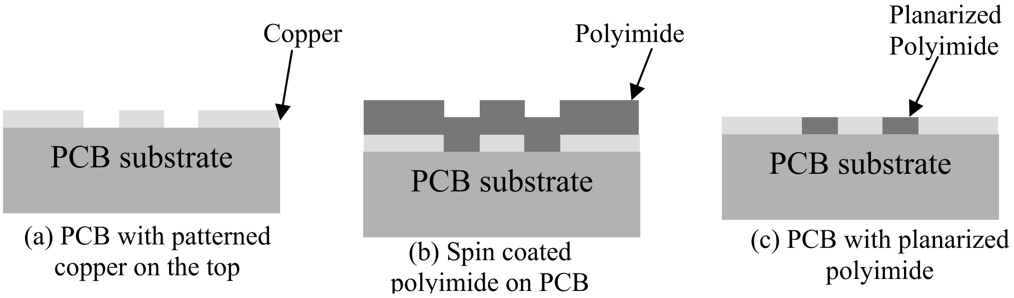
This is a two steps process which includes planarization and polishing.

*Planarization:* Conductor traces are patterned on the PCB copper clad Fig. 1 (a). As shown in Fig. 1(b), 18-20 µm thick polyimide (depending on the copper clad thickness) is spin coated on patterned copper of 17.5 µm thickness and then placed on hot plate by raising temperature from room temperature to 220 °C with rate of 6.9° C/min and kept for 1hr at 220 °C to cure the polyamide layer. Polyamide film surface profile is same as that of lower copper surface. This is followed by next step of polishing [4].

*Polishing:* Polyimide is polished in two steps. First, polyimide surface is polished with Silicon carbide fine powder sheet to remove the polyimide up to Copper surface Fig. 1(c). Although it may cause scratches and cuts on the surface, but this can be reduced in second step. Second step is to polish the surface with diamond paste of 6um particles on nylon cloth. This technique will in turn reduce the root mean square surface roughness up to 30 nm or even less [4].

### 2.1.2.2. Compressive Molding Planarization (COMP)

Compressive molding planarization (COMP) is utilized if device has membrane structures such as RF-Switch, varactors, filters, resonators, phase shifters etc. Copper clad is pattered Fig. 2 (a). In this technique, thick layer of photo-resist (PR) is spin coated on patterned copper as shown in Fig. 2 (b) and a smooth surface like glass is kept on the top of the spun coated photoresist Fig. 2 (b). Second step is to apply high temperature (100 ºC) and pressure (40Psi). High temperature is to melt and to re-flow the photoresist under smooth surface to planarize the PR Fig. 2 (c). This planarized PR acts as sacrificial for membrane. Later on PR is etched using acetone. Only drawback of COMP is low reliability of device because voids formation (Fig. 2 (d)) may take place in the PR during this process which may cause air bubble entrapment when high temperature is applied [4, 27]. Surface roughness can be reduced to less than 50 nm and 10 % uniformity in film thickness can be obtained over 2.5×2.5 $cm^2$ by controlled COMP process [26].

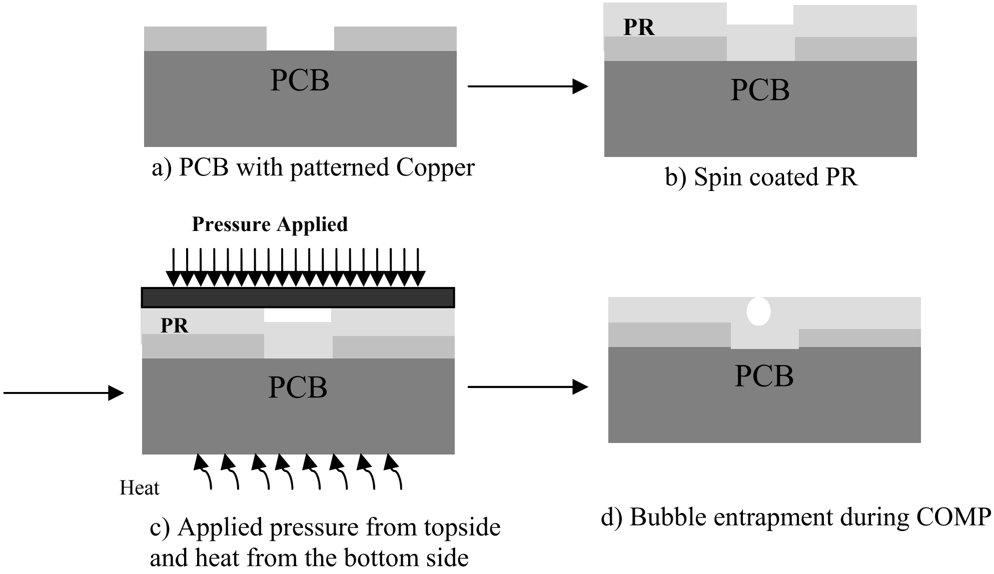


(a) PCB with patterned copper on the top

(b) Spin coated polyimide on PCB

(c) PCB with planarized polyimide

**Fig. 1.** Polishing and planarization process [4]. Reproduced from B. Ghodsian, C. Jung, B. A. Cetiner, F. D. Flaviis, Development of RF-MEMS switch on PCB substrates with polyimide planarization *IEEE Sensors Journal* 5 no. 5 pp. 950-955 (2005) © IEEE



a) PCB with patterned Copper

b) Spin coated PR

c) Applied pressure from topside and heat from the bottom side

d) Bubble entrapment during COMP

**Fig. 2.** COMP process steps [4]. Reproduced from B. Ghodsian, C. Jung, B. A. Cetiner, F. D. Flaviis, Development of RF-MEMS switch on PCB substrates with polyimide planarization, *IEEE Sensors Journal* 5 no. 5 pp. 950-955 (2005) © IEEE.

### 2.1.3. Micro-vias in PCB

Mechanical drilling can be used to drill through holes of diameter >200 μm in PCBs. Smaller size holes <50 μm is prelim requirement for high package density. Laser is reliable method to drill microvias in PCB with high resolution depending on the laser wavelength, beam energy density, composition and thickness of the substrate. Some of the lasers types used for drilling are radio-frequency excited carbon dioxide laser, transversely excited atmospheric carbon oxide laser, 3rd harmonic Nd:YAG laser, Krypton fluoride (KrF) excimer laser [22]. Lasers are utilized depending on the substrate materials as listed in Table 3:

**Table 3**. Comparison in drilling techniques [22].

| | Radio-frequency excited carbon dioxide laser | Transversely Excited atmospheric carbon oxide laser | 3rd harmonic Nd:YAG laser | KrF excimer laser |
|---|---|---|---|---|
| Wavelength | $CO_2$ laser emits light in far infra-red region 10.6 | Emits Same wavelength as $CO_2$ laser | operated ultra violet spectrum 355 nm | Operates at short wavelength 248 nm |
| Laser Pulse width and output power | Pulse width of range 30-100 µs with average output power of 200 W at 10 kHz | Short pulses of 1 µs with high peak power of $10^6$~$10^7$ W at 100 Hz | Few nanoseconds and high output peak power | 20 ns<br>High peak power of several megawatts |
| Drilling speed | Drilling is done sequentially | Depending on the optics demagnification, processing area can be varied from 2*2 $mm^2$ to 5*5 $mm^2$ | Microvias are drilled sequentially | Microvias exposed within laser beam area drilled simultaneously |
| Compatibility of the PCB material | This is used to drill holes in FR4 with narrower range than and of lower quality but with low taper walls than TEA $CO_2$. | This technique is good for FR4 with E- glass fiber reinforcement material to drill high quality vias with consistent taper angle and smooth walls with optimal energy density range 12-18 $J/cm^2$ | This technique can be used to drill holes with smooth walls of high aspect ratio 20:1. minimum achievable diameter is 50 µm | It is used to drill holes in polyamides for high resolution vias with laser energy density of $3J/cm^2$. It can provide vias of size <50 µm |

### 2.1.4. Other Processes

In PCB lithography, ink-jet printer printout is used as mask (no sophisticated or costly mask production equipments are required to make mask) [28]. Lithography and etching processes can be performed similar to Silicon fabrication, but PCB lithography and etching do not need high class clean room. Dry film photoresist technique is used for lithography which does not need spinner; and also there is no substrate size constraint.

## 2.2. Applications of PCB Technology

The PCB technology is compatible for multilayer fabrication which includes stack of PCB substrates together to construct the device. The multilayer PCBs are used to fabricate fluidic channels, temperature sensors, capacitance bubble detector, valves, pressure sensors, micropump. These sensors/devices can be integrated with electronics circuitry on the same PCB substrate [1, 24, 25]. Multilayer stack of PCB substrates has been demonstrated to develop a micropump. This micropump is made of four double sides 70 µm copper coated PCB with total thickness 800 µm aligned as sown in Fig. 3 [24]. Patterned 8 µm thin kapton foils and four doubled sided copper plated PCB are properly aligned and fixed using adhesives. It is worth to note that PCB technology has found applications in optics [29, 30] also. The conductivity sensor, temperature sensor, and pressure sensor are combined on the PCB substrate to make salinity sensing device [31]; which is used to monitor and analyze the marine water, fresh water, industrial water etc.

The complete RF system cannot be fabricated on conventional substrates i.e. Silicon or Gallium arsenide because radiating elements (antenna) do not work efficiently on high dielectric constant substrates. RF MEMS devices fabricated on conventional substrates are mounted on PCB using wire bonding to construct RF system. Wire bonding may cause impedance mismatching and increase in signal losses at the interface which need to be compensated by adding matching network. RF MEMS devices fabricated on conventional substrates need to be packaged individually which further add in device cost [32]. This can be avoided by integrating RF MEMS devices and other components of the RF system on the same PCB substrate. There is full ESA (electronically steerable antenna) system consisting of power divider, RF MEMS phase shifter and antenna on single PCB substrate [33]. A monolithic phased antenna array is shown in Fig. 4 [2]. A monolithic electronically steerable antenna (ESA) is reported by Sundaram et al [34] also. An array antennas with 50 % impedance bandwidth from 4 GHz to 6 GHz with CPW feed utilizes RF MEMS switches with antenna on PCB substrates [5, 35]. The PCB MEMS phase shifter with very low insertion loss of 0.56 dB at 9 GHz [3] and RF MEMS switches with insertion loss 0.4-0.45 dB with isolation greater than 20 dB for frequency range 1-30G Hz [36] are mentioned in literature. Except that there are switches fabricated by depositing Silicon nitride using HDCIP CVD deposition process at low temperature compatible to PCB to get high breakdown voltage and COMP planarization technique to get smooth surface for further layers [26, 37,38]. PCB based low cost coplanar patch antenna with varactors of tunable frequency from 5.545 GHz at 0 V to 5.185 GHz at 116 V having return loss of the CPA is better than 40 dB over the tuning range of 360 MHz [39].

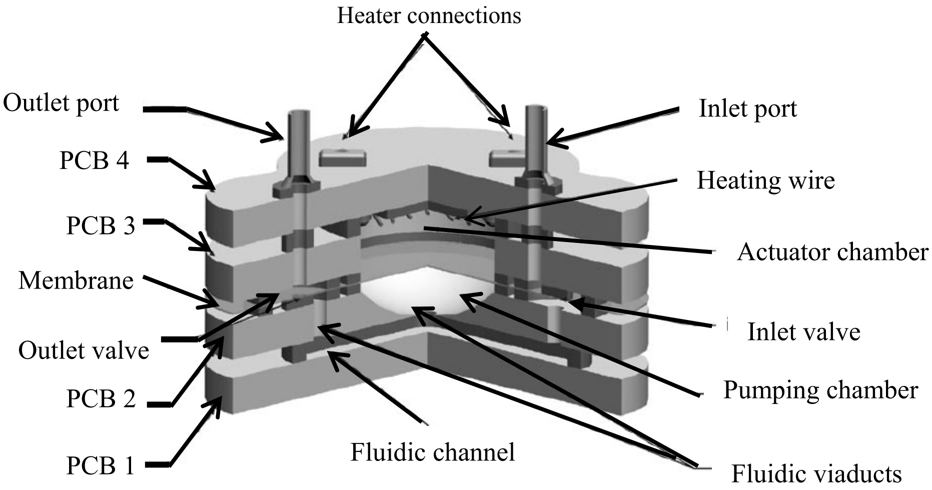
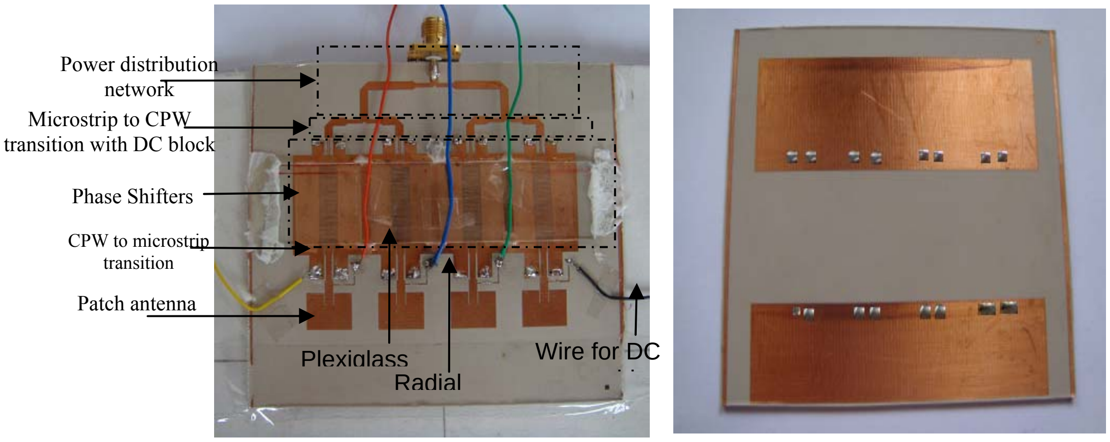


**Fig. 3.** Cross-sectional view of the micropump using multilayer technology [24]. Reproduced from A. Wego, S. Richter, L. Pagel, Fluidic MEMS based on printed circuit board technology, *Journal of Micromechanics and Microengineering,* IOP publisher 11 pp. 528–531, doi:10.1088/0960-1317/11/5/313 (2001) © IOP Publisher.

## 3. Low Temperature Co-fired Ceramics (LTCC)

Multilayer ceramic substrate was originated in late 1950’s by RCA Corporation using current process technologies. These ceramics were demonstrated by firing at high temperature of 1600 ºC, there called as HTCC (high temperature co-fired ceramic). During early 1990s many Japanese and American electronics developed low temperature co-fired ceramic (LTCC) multilayer boards. Fujitsu and IBM were first to use LTCC in commercial applications [40].



(a) (b)

**Fig. 4.** PCB based System (a) top side, (b) backside of phased antenna array [2]. Reproduced from P. Goel, K. J. Vinoy, A low-cost phased array antenna inte-grated with phase shifters cofabricated on the laminate, *Progress in Electromagnetics Research B,* 30, pp. 255-277 (2011) © *Progress in Electromagnetics Research. Reproduced courtesy of the Electromagnetic Academy.*

LTCC is made of Green sheet which in turn is made by casting slurry of ceramic powder (45 % $Al_2O_3$, 40 % glass) and organic components (15% solvent, plasticizer and binder) [41] into tape using doctor blade. This is a flexible material. Vias for conduction between layers and patterns are screen printed on green sheets using conductive paste. Screen printed layers are aligned under heat and pressure to laminate. A multilayer substrate is obtained by firing conductor and ceramic together and driving off organic binder [40]. A typical LTCC multilayer process is illustrated in Fig. 5.

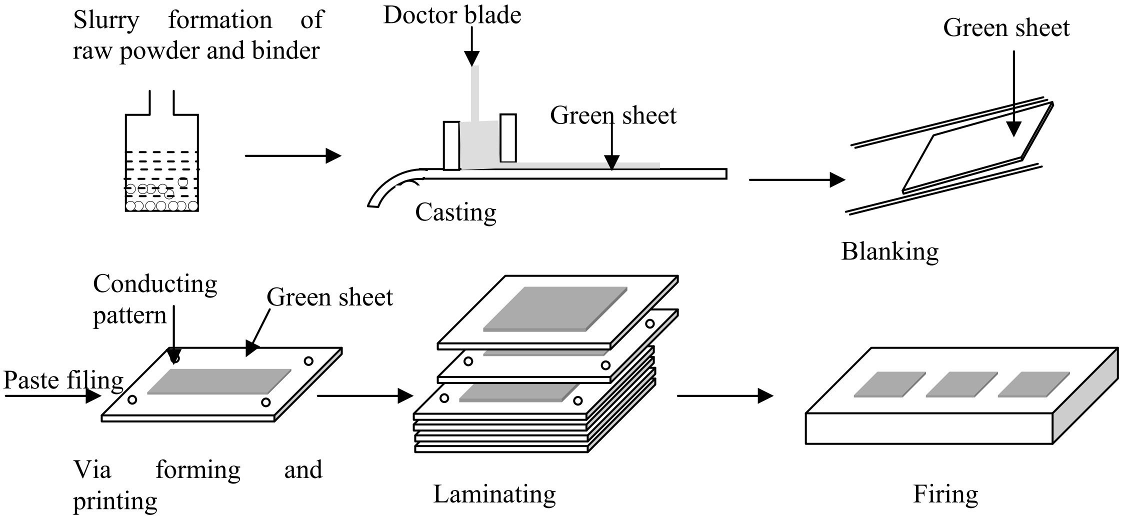


**Fig. 5.** LTCC manufacturing process [40]. Reproduced from Y. Imanaka, *Multilayer low temperature cofired ceramic (LTCC) technology,* Fujitsu Laboratories Ltd. Japan Springer (2005) © Springer.

LTCC can be used to fabricate both MEMS and ICs, to implement monolithic devices. Some of the advantages of LTCC usage are listed below:

1. LTCC board can be used for substrate as well as package.
2. It is a multilayer technique which helps in miniaturizing and making highly dense interconnections in the system. Now days, up to 80 layers can be arranged with proper alignment. LTCC's multilayer

nature helps in fabricating 3D structures [7]. 3D fabrication helps in reducing device size which further decreases interconnection length and consequently parasitics could be reduced [42]. Secondly LTCC substrates are patterned separately for each layer. Therefore unlike any conventional fabrication technology, manufacturing defect in any layer can be rectified by repeating the process for that particular layer [43].

3. Thick and thin film components, active and passive components can be fabricated all together and on both sides of LTCC [44].
4. Important features of LTCC are: wider range of electrical properties, mechanical and thermal properties comparable to Silicon or pyrex substrates [7].
5. Earlier LTCC was specifically used for RF devices because of their high density interconnection feasibility, low dielectric constant and low loss materials. But because of their flexibility in fabrication to make 3D structures made it useful for various MEMS.

On the other hand, disadvantages of LTCC technology are:

1. Low mechanical strength, low thermal conductivity, high tolerance (±0.3 % along x, y and ±0.5 % along z direction) [7].
2. Features size of <1 mm cannot be attained (generally 1 mm to 100 mm) [7, 42],

### 3.1. Fabrication Processes for LTCC Technology

LTCC is made using dielectric tapes, connecting vias, external and internal conductors and passive components (resistors, capacitors, inductors). Passive components (resistors, capacitors and inductors) can be made using screen printing. Vias can be fabricated using mechanical punching, laser micromachining, numerically controlled milling or jet vapor etching. Casting and embossing are to create cavities and channels. All layers are stacked, registered, laminated and then cofired to make 3D structures [7, 44].

#### 3.1.1. Screen Printing

Screen printing is done to pattern conductor traces on LTCC substrate. As shown in Fig. 6 [45], mask and screen is mesh of wires kept in aligned fashion to pattern metal. Screen is a mesh structure made of stainless steel wires. Diameter of wires, number of strands in the mesh and viscosity of the emulsion are optimized according to the requirement. RF MEMS applications need very narrow width conductor tracks which are possible using small diameter screen to get large aperture ration with thin emulsion [45]. Conductor paste made by pressing metallic powder, solvent and glass binder on the LTCC substrate using comb or squeeze through printing screen [40, 45].

#### 3.1.2. Micromachining

$CO_2$ laser and excimer laser, or a diamond cutter can be used for micromachining small structures [7].

#### 3.1.3. Via Punching

Vias are made in green sheet for interconnection between layers. Vias can be punched using numerically controlled (NC) drilling, milling or laser micromachining techniques. Recently Nd-YAG laser has been used for via punching and also fine holes can be made depending on the power and focus of the beam [40]. Via holes are made using either any of these methods or mechanically with die. Vias of diameter 80 μm can be made and more than 1,11,000 vias can be made in 100 $mm^2$ area [46].

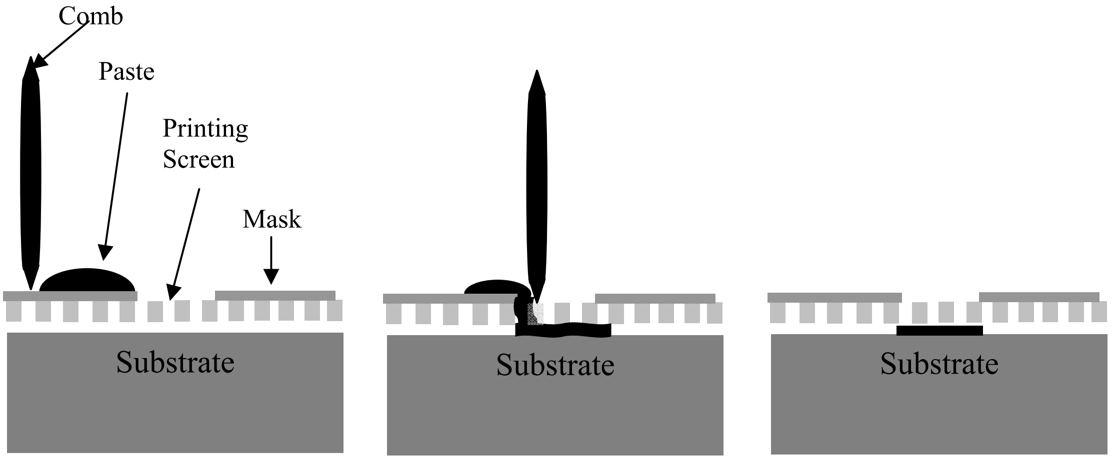


**Fig. 6.** Screen printing process flow to get pattered conductor tracks [45]. Reproduced from A. Lamminen, Design of millimeter-wave antennas on low temperature co-fired ceramic substrates, *Master's Thesis* Espoo, (2006) © Lammimen.

### 3.1.4. Lamination

All the patterned layers are stacked in aligned manner under heat and pressure to laminate the stack. Lamination is done at temperature range 60 ºC-110 ºC under pressure of 2200-3600 psi uniformly. Lamination process should be homogenous because in-homogeneity causes shrinkage of the substrates. Lamination temperature and pressure vary from system to system [7, 40, 46].

### 3.1.5. Co-firing

Cofiring is done to make single system by fixing LTCC substrates altogether. Laminated stack of LTCC is placed in furnace, first at 500 ºC to evaporate binder material and then at 900 ºC for conductor and ceramic sintering together [40].

## 3.2. Applications of LTCC Technology

Although the major application of LTCC technology is in RF/millimeter wave devices, but versatility of LTCC material properties makes it useful for many other applications including especially MEMS, and bio-MEMS. Initially this technology was used for fabrication of MEMS devices whereas microelectronic components were fabricated on conventional semiconductor substrate but later it was found compatible for microelectronics technology too. Some of the LTCC applications are listed as: MEMS based thermistor flow sensors [7], almost same TCE of silicon and LTCC made it possible to transfer probes from silicon to LTCC to fabricate probe card using LTCC multilayer technology [47, 48]. Bio-compatibility of LTCC substrates found applications in making lab-on chip sort of MEMS in which major issue is of fabricating microchannels, which is possible using laser micromachining, milling etc techniques [6, 41, 43, 49, 50]

Apart from that LTCC found applications in the field of chemical sensors, micropump [51], solid micro-thrusters for micro-spacecraft for accurate altitude and orbit control [52], base material for optical fibers because of it's highly integrable features [53], optics integrated with fluidic micro-channels to see the impact of optics on flow is also discussed [54], heating and cooling microsystems, micro-fluidic systems [6]. A multilayer CO and $CH_4$ gas sensor using gas sensitive material $SnO_2$ (Fig. 7) [55]. Gas sensitive layer is made of pure $SnO_2$ or $SnO_2$ doped with Pd, where Pd acts as catalyst. Smaller window made in all the layers is for proper heat distribution, and bigger window made in bottom two layers is to obtain proper sensor temperature at low heating power [55].

In the beginning, major application of LTCC was in RF devices due to low loss substrate and dense interconnection properties. Macroscale mechanical switches cause low loss but bulky, whereas semiconductor electronics switches are light but lossy. LTCC overcomes both the challenges because of its integration compatibility. 9-layers LTCC substrate with 32 switches integrated to create 4x4 switch matrix with excellent RF performance up to 7 GHz is demonstrated [56]. Secondly, LTCC is reported to integrate antenna, transceiver, amplifier, and antenna switch, all RF modules as single system, without limiting its performance of power, efficiency, and directivity unlike Silicon technology [57]. LTCC could be used as substrate as well as packaging material for RF-devices, as reported [58]. Beauty of this technology is to make 3D structures (Fig. 8 [59]) which takes 75 % lesser space than planar inductors. It is clear that all the sides of the spiral inductor are fabricated on different metallic layers [59]. Zhao et al [60] demonstrated PHEMT and LDMOS power amplifier utilizing LTCC technology.

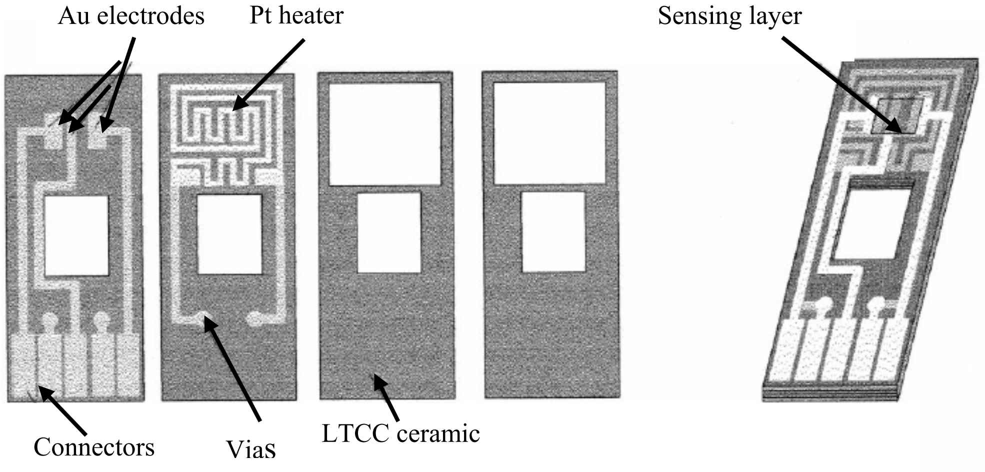


**Fig. 7.** Multilayer $SnO_2$ gas sensor using stack of LTCC substrates [55]. Reproduced from H. Teterycz , J. Kita, R. Bauer, L. J. Golonka, B.W. Licznerski, K. Nitsch, K. Wiśniewski, New design of an $SnO_2$ gas sensor on low temperature cofiring ceramics, *Sensors and Actuators B, Elsevier*, 47, pp. 100-103 (1998) © *Elsevier.*

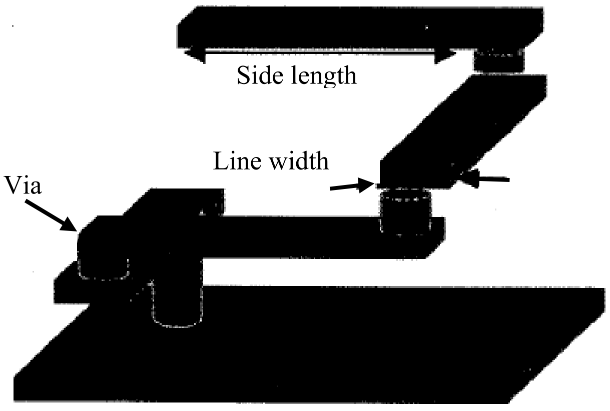


**Fig. 8.** Schematic diagram of 3D inductor [59]. Reproduced from R. J. Pratap, S. Sarkar, S. Pinel, J. Laskar, Gary S, Modeling and optimization of multilayer LTCC inductors for RF/Wireless applications using neural network and genetic algorithms, *IEEE Electronic Components and Technology Conference* (2004) © IEEE.

## 4. Liquid Crystal Polymer (LCP) Technology

LCP is a thermoplastic material and came into picture in 1970’s. These were commercially known only in 1980s when its polymer resins were available. It consists of densely packed polymer chains of aromatic polyesters in aligned manner. Molecular structure of liquid crystal polymer is shown in Fig. 9, which is made of two aromatic rings A and A′ which can be either benzene ring or derivative of benzene. Side chain group R and R’ can be alkyl ($C_nH_{2n+1}$), alkoxy ($C_nH_{2n+1}O$), acyloxyl, alkylcarbonate, alkoxycarbonyl, etc. Linkage Xs are made of stilbene (-CH=CH-), ester (-COO-), azoxy (-N ≡ N-), schiff base (-CH=N-), acetylene (-C≡C-), and diacetylene ( –C≡C-C≡C-) [61].

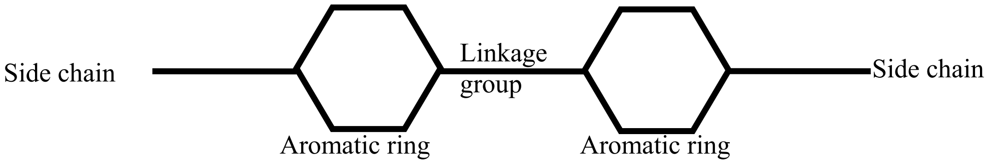


**Fig. 9.** Molecular structure of liquid crystal polymer [61]. Reproduced from Iam-Choon Khoo *Liquid Crystals,* Hoboken New Jersey Published by John Wiley & Sons Inc second edition, (2007) © John Wiley & Sons.

Polymer such as Kapton is used in MEMS fabrication but LCP is being considered better due to cost which is around 50-80 % lower than Kapton. Secondly LCP polymers can be directly bonded to other substrate by thermal lamination, whereas Kapton need adhesive to make bond with other substrate. Comparison in properties of LCP and Kapton is listed in Table 4.

**Table 4.** Comparison between LCP and Kapton properties [14]. Reproduced from X. Wang, J. Engel, C. Liu, Liquid crystal polymer (LCP) for MEMS: processes and applications, *J. Micromech. Microeng,* IOP publisher, 13, 2003, pp. 628-633, doi:10.1088/0960-1317/13/5/314 © IOP publisher.

| **Parameters** | **LCP (Vectra A-50)** | **Kapton (HN200)** |
|---|---|---|
| Melting temperature (°C) | 280 | >400 |
| Dielectric constant | 2.8 | 3.5 |
| Loss factor, tan $\delta$ | 0.004 | 0.002 |
| Moisture absorption (%) | <0.02 | 2.8 |
| Coefficient of thermal (ppm/°C) | 0–30 | 20 |
| Expansion controllable | Controllable | |
| Tensile strength | 30 Kpsi | 34 Kpsi |
| Tensile modulus | 1.3 Mpsi | 370 Kpsi |
| Specific gravity | 1.4 $kgm^{-3}$ | 1.42 $kgm^{-3}$ |

Some of the important properties of LCP are mentioned below:

1. LCP polymers are with loss factor 0.004 and relative permittivity of ~3, which is approximately constant for 0.5 to 40 GHz frequency range. Therefore LCP are suitable for wide band RF applications [14, 62].
2. Negligible moisture effects even at elevated temperatures which is good for RF MEMS applications [14, 62].
3. Excellent chemical compatibility as it is not attacked by commonly used solutions such as: HF, buffered HF, photoresist, developers, acetone and alcohol [62].
4. Low substrate cost as its manufacturing is easy [62].
5. It is near hermetic material and low thermal coefficient of expansion which can be controlled during fabrication [62, 63].

6. The unique feature of polymers technology over Silicon technology is high mechanical fracture limit and biocompatibility [14].
7. LCPs properties: high thermal stability, low flammability, low moisture absorption and its thermoplastic in nature which is recyclable. All these properties of LCP make it suitable material for packaging [14]

LCP is a thin and flexible material which needs specific fabrication processes to fabricate MEMS. Fabrication processes developed specifically for LCP technology are discussed here.

### 4.1. Fabrication Processes of LCP Technology

LCP films are thin and flexible which makes difficult to conduct processes of spin coating, lithography and deposition on it directly. Secondly LCP are made of polymers which needs special kind of etching processes. Fabrication processes for LCP technology are described below:

### 4.1.1. Spin Coating/lithography and Metallization

LCPs are thin and flexible which may cause warpage during spin coating of photoresist. Therefore LCP films are bonded to planar surfaces such as Silicon wafer to avoid warpage during spinning. LCP films are bonded to Silicon wafer with dissolvable adhesives to remove Silicon wafer on completion of process. There may be warpage issues during high temperature processes which can be avoided by performing process in intervals which would help in limiting the heat [14].

### 4.1.2. Etching

A suspended flap supported by two flexural cantilevers is reported in [14] as shown in Fig. 10 using RIE in oxygen plasma. Surface roughness increased from 190 nm to 1.138 µm before and after RIE process respectively. Etch rate of vectra A-950 LCP in oxygen plasma is of 0.22~0.27µm/min at power of 350 W under chamber pressure of 500 mTorr. Laser micromachining is commonly used for etching the LCP films. Minimum feature size of 25 µm can be attained. Conventional MEMS fabrication techniques of lithography, metallization, and plasma etching are used with proper modification to obtain lower feature size.

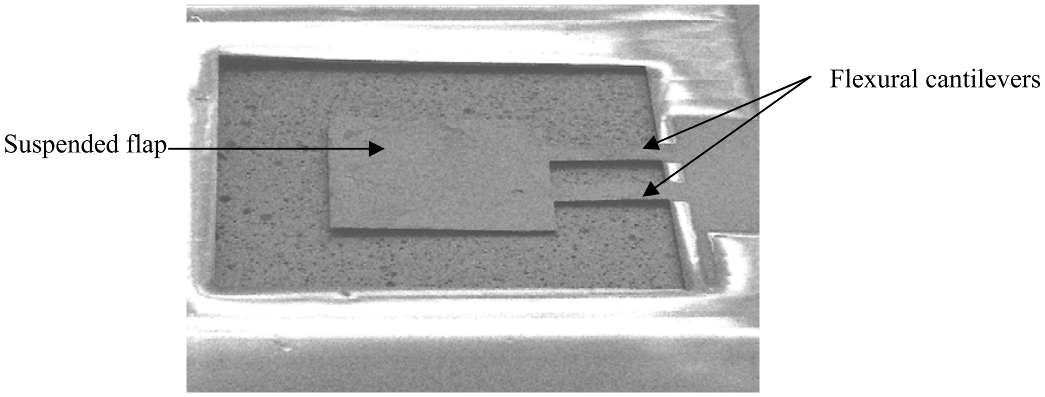


**Fig. 10.** The SEM image of a suspended flap supported by two flexural cantilevers [14]. Reproduced from X. Wang, J. Engel, C. Liu, Liquid crystal polymer (LCP) for MEMS: processes and applications, *J. Micromech. Microeng* IOP publisher, 13, pp. 628-633 (2003), doi:10.1088/0960-1317/13/5/314 © IOP publisher.

#### 4.1.3. Drilling Holes

Excimer laser is used to etch the LCP film in controlled manner to make cavity or steps. Laser micromachining is used for LCP films etching. $CO_2$ engraving laser of 10 μm wavelength is used to make through holes in LCP films because of its high power and fast cutting speed [63]. LCP and metals can be etched selectively by using laser pulses of different fluence [64].

LCP polymers are patterned with these processes to realize MEMS. MEMS applications using LCP technology are discussed next.

### 4.2. MEMS Applications of LCP Technology

The MEMS capacitive sensor is demonstrated using multilayer LCP lamination technique because LCP polymers layers can be strongly bonded using thermo-compression bonding at 150 psi and 280 ºC (280 ºC is melting temperature of one of the multilayer structure). Reported sensitivity of fabricated novel capacitive pressure sensor is 4.8 mV/kPa [65]. The LCP polymers can be used for environmental sensing system using PCBMEMS based technology to measure the conduction, temperature, depth of ocean under harsh conditions such as salinity, temperature, and pressure of ocean [66]. LCP found applications to fabricate micro-fluidic channels, planar neuron probes, and micro-tactile sensors. It can be bonded to conventional substrate such as glass, silicon with strong force using lamination bonding to make sealed micro-fluidic channels [62]. LCP polymers can be used to fabricate flow sensor, tactile sensor because of its flexibility [14]. LCP technology is compatible for multilayer stack arrangements to reduce the space without compromising the system performance. Schematic of phased array antenna system fabricated by stacking LCP films using multilayer technology is shown in Fig. 11 [8]. In this, LCP has been used as package which is similar to system on package technology.

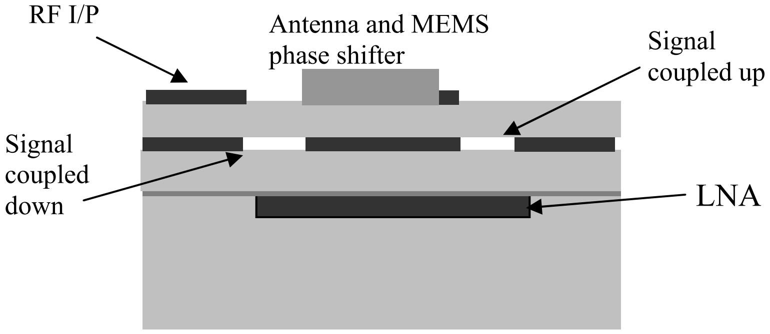


**Fig. 11.** Multilayer system-on-package (SOP) phased array antenna utilizing LCP multilayer technology [8]. Reproduced from N. Kingsley, G. E. Ponchak, J. Papapolymerou, Reconfigurable RF MEMS phased array antenna integrated within a liquid crystal polymer (LCP) system-on-package, *IEEE Transactions on Antennas and Propagation,* 56, No. 1, pp. 108-118 (2008) © IEEE.

Dielectric properties of LCP make it useful for RF MEMS applications. LCP can be used to realize system-in-packaged (SIP) RF devices. Most important application of LCP polymer based SIP are RF MEMS because of low dielectric constant and low loss tangent of LCP materials which are comparable to FR4 and LTCC [67, 68] as listed below in Table 5.

**Table 5.** Comparison in substrate materials [68]. Reproduced from D. C. Thompson, O. Tantot, H. Jallageas, G. E. Ponchak, M. M. Tentzeris,J. Papapolymerou, Characterization of liquid crystal polymer (LCP) material and transmission lines on LCP substrates from 30 to 110 GHz, *IEEE Transactions on Microwave Theory and Techniques,* 52, No 4, 2004, pp. 1343-1352, © IEEE.

| Substrate Material | Dielectric Constant | Loss tangent | Frequency (GHz) |
|---|---|---|---|
| FR4 PCB | 4 | 0.025 | <10 |
| LTCC | 5.7-9.1 | 0.0012-0.0063 | <12 |
| LCP | 2.9-3.2 | 0.002-0.0045 | <105 |

Its measured dielectric constant variation over frequency range of 2 GHz-110 GHz is 2.36 to 2.37, which makes it suitable for wide band applications [69]. MEMS phase shifter in LCP package is already demonstrated with reliable performance [11], an integrated RF-module fabricated on multilayer LCP substrates with top and bottom PCB substrate to provide mechanical strength to the system is also reported [10], low cost and light weight 4X8 antenna array with 2-bit phase shifter using MEMS switches with multiple layers of LCP substrate with loss less than 0.5 dB per bit [9]. RF MEMS switch fabricated using LCP thin films have applications in phase shifter, filters etc. [63]. Delay line microstrip 2-bit phase shifter fabricated on LCP using MEMS switches showed performance of average return loss 22.5 dB and average insertion loss 0.98 dB per bit [13]. RF MEMS switch fabricated on LCP is shown in Fig. 12 [12].

## 5. Polymer Core Conductors Technology

As is clear from the name that polymer is being used as core with metal coating. It is difficult to process thick metallic layer compared to polymers which is made convenient with this technology. Major use of this technology is in RF-devices. This is because, at high frequency, signal attenuates while moving from conductor surface to inside along depth/thickness. Therefore a hollow conductor of thickness five times the skin depth, is same as solid conductor at high frequencies [16]. Until now, SU-8 is being considered as the most promising material for core realization due to its versatile nature. SU-8 polymer was developed in 1980 by IBM. In the beginning it was used in microelectronics as high resolution negative photoresist. Later this material, because of its ultra thick spin coating on substrate as photoresist and structural material, found applications in MEMS. Basic structure of SU-8 is shown in Fig. 13.

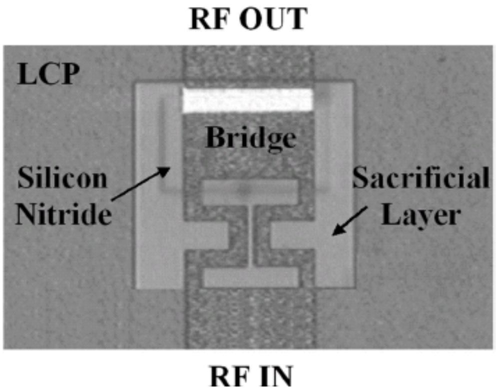


**Fig. 12.** RF MEMS switch fabricated on LCP [12]. Reproduced from N. Kingsley, S. K. Bhattacharya, J. Papapolymerou, Moisture lifetime testing of RF MEMS switches packaged in liquid crystal polymer, *IEEE Transactions on Components and Packaging Technologies,* 31, No 2. pp. 345-350 (2008) © IEEE.

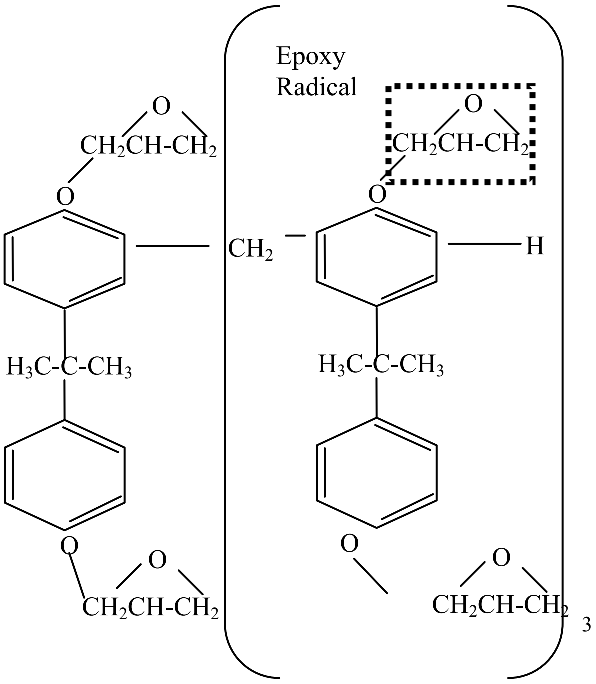


**Fig. 13.** SU-8 molecular model [70]. T. Namazu, S. Inoue, K. Takio, T. Fujita, R Maenaka, K. Koterazawa, Visco-elastic properties of micron-thick SU-8 polymers measured by two different types of uniaxial tensile tests, *IEEE,* pp. 447-450, (2005) © IEEE.

Major features of polymer core conductor are:

1 Polymer core conductors can be used for high aspect ratio metallic structures [16]. This process can be used to make thick (up to thousands of microns) structures.

2 In applications, were substrate to metal gap is required to reduce substrate effects on device which are useful especially at high frequency [71].

3 Double expose single develop process of SU-8 made this technology very easy and cheap to process [16].

### 5.1. Fabrication Processes of Polymer Core Conductors Technology

A typical process to realize polymer core conductors is discussed here. A thick layer of SU-8 is spun coated Fig. 14 (a). SU-8 is patterned using double exposure and single development to get bridge structure Fig. 14 (b, c). After double exposure, SU-8 polymer links are only at the bridge structure and remaining SU-8 gets etched away during development Fig. 14 (d) [16]. Thin metal layer can be electroplated on the substrate as well as below and top of SU-8 bridge to make polymer core conductor.

### 5.2. MEMS Applications of Polymer Core Conductor Technology

3D structures of polymer core conductor found applications in making microelectrode arrays (MEAs) with microfluidic ports for profusion channels to study complex networks morphologies and tissue slices [72]. Polymer core conductor properties made it useful for transmission over ACSR (aluminum conductor steel reinforced) even at macro scale [73].

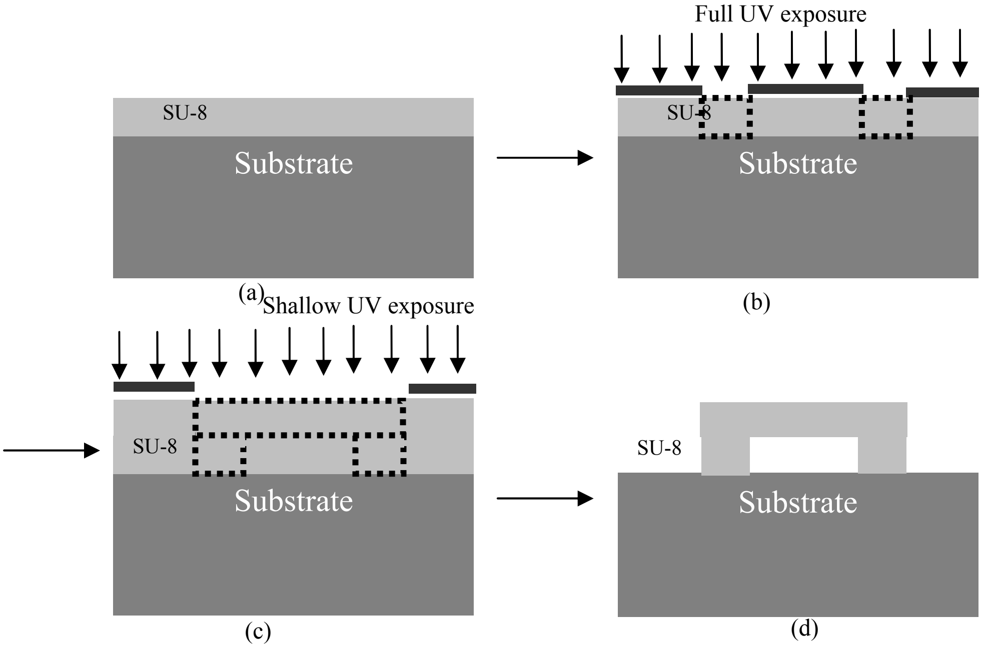


**Fig. 14.** Double exposure single development technique [16]. Reproduced from Yong-Kyu Yoon, Jin-Woo Park, Mark G. Allen, Polymer-core conductor approaches for RF MEMS, *Journal of Microelectromechanical Systems,* 14, No. 5 (2005) © IEEE.

The performance of a device operating at millimeter wavelength is highly influenced by substrate properties. Substrate effects can be reduced using polymer core conductors. High Q inductors and antennae are already reported in literature. A 50 µm thick spiral inductor with Q factor 95 for 1.1 nH and solenoid inductor of 500 µm height with Q factor 71 are reported [74, 75]. Air core inductor fabricated using double exposure single develop fabrication process is shown in Fig. 15. Patch antenna is the most popular antenna where performance is degraded due to substrate effects but 3D antennae formed with this technology can overcome these drawbacks. As monopole driven YAGI-UDA antenna with wide bandwidth 12 %, air lifted patch antenna having BW 7 %, magnetically lifted monopole antenna with BW 20.7 % , CPW fed quarter wavelength monopole antenna for W-band (75 GHz-110 GHz) [71], integrated filters in air cavity on silicon wafer [76].

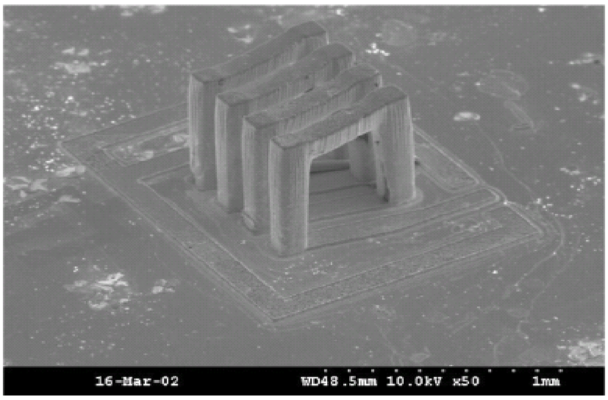
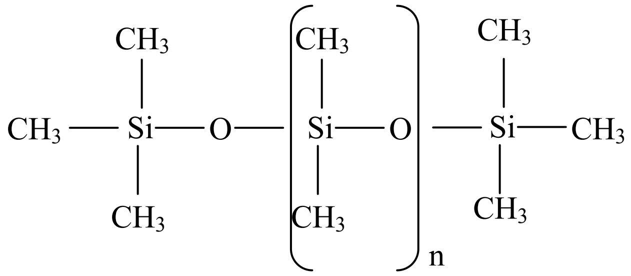


**Fig. 15.** SEM photograph of air core inductors double expose single develop fabrication process [16]. Reproduced from Yong-Kyu Yoon, Jin-Woo Park, Mark G. Allen, Polymer-core conductor approaches for RF MEMS, *Journal of Microelectromechanical Systems* 14 no. 5 (2005) © IEEE.

## 6. Polydimethylsiloxane (PDMS) Technology

The Polydimethylsiloxane (PDMS) is an elastomer polymer synthesized by mixing liquid monomer and cross-linker. Polymerization reaction takes place on heating and forms solid elastomer [77]. Chemical formula of PDMS is as shown in Fig. 16:



$$CH_3-Si(CH_3)_2-O-[Si(CH_3)_2-O]_n-Si(CH_3)_2-CH_3$$

**Fig. 16.** Polydimethylsiloxane (PDMS) polymer structure [78]. Reproduced from P. L. Baron, J. Casanovas, J. P. Guelfucci, R. L. S. Hoi, Photoconductivity induced by VUV photons in Polydimethylsiloxane and Polymethylphenylsiloxane oils, *IEEE Transactions on Electrical Insulation,* 23, No 4, pp. 563-570 (1988) © IEEE.

Elastomer polymers can be stretched 2-10 times of the original dimension like a rubber and its elasticity is controlled by precursors i.e. monomer and cross-linker. PDMS is one of the most widely used polymers in MEMS technology [77, 79]. Patterning of PDMS using mold is simple and fast compared to etching and bonding in semiconductor technology [80]. In some applications, flexible substrate is better to use because of light weight, low cost, and more flexibility over conventional semiconductor substrate [81]. These can develop feature size of the order of nm by casting. It is one time process to make master mould of desired structure [82].

### 6.1. Fabrication Process of PDMS Technology

PDMS structures are fabricated using mould where SU-8 [83] and Silicon [84, 85] are most commonly used master moulds to realize structures. PDMS fabrication process using silicon mould is shown in Fig. 17 which is carried out in six steps. Initially, Silicon wafer is spin coated with photo resist (Fig. 17 (a)). Photoresist is patterned using lithography (Fig. 17(b)) and developed using developer to attain pattern on photoresist (Fig. 17(c)). Silicon etching is done using DRIE from the exposed parts of the wafer (Fig. 17(d)). PDMS is poured on the clean master mould and cured in oven (Fig. 17(e)). Cured PDMS is peeled from the silicon wafer and PDMS cantilever array is ready (Fig. 17(f)).

### 6.2. MEMS Applications of PDMS Technology

The 3D micro channels fabricated in PDMS are reported in [80], which is made of many thin PDMS layers where each layer is patterned using master mould made of silicon. An array of temperature sensor on PDMS [81] is shown in Fig. 18. Silicon is used as the base as well as mould. Base is required during spin coating whereas mould is used for patterning the PDMS.

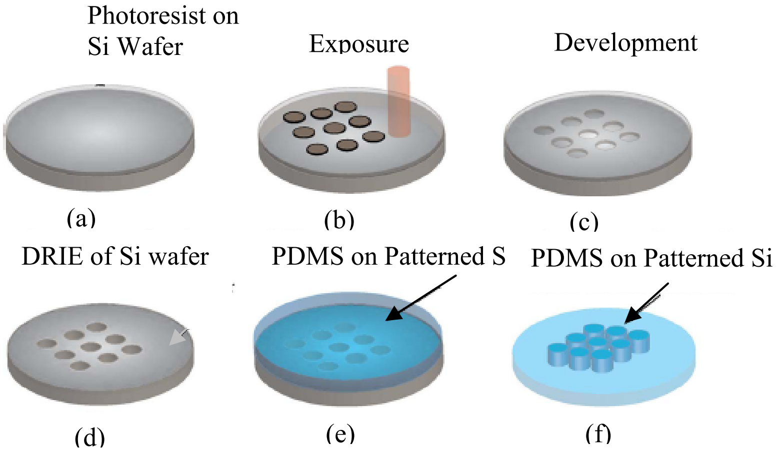


**Fig. 17.** Fabrication steps for making the microcantilever array on PDMS (a) Spin photoresist on Si wafer (b) define patterns on photoresist by exposure (c) develop exposed wafer (d) perform DRIE to pattern silicon (e) Pour PDMS on cleaned wafer, and cure in oven (f) Peel cured PDMS from silicon wafer to obtain device [85]. Reproduced from K. A. Addae-Mensah, S. Retterer, S. R. Opalenik, D. Thomas, N. V. Lavrik, J. P. Wikswo, Cryogenic etching of silicon: an alternative method for fabrication of vertical microcantilever master molds, *Journal of Microelectromechanical Systems*, Vol. 19, no. 1, pp-64-74, (2010) © IEEE.

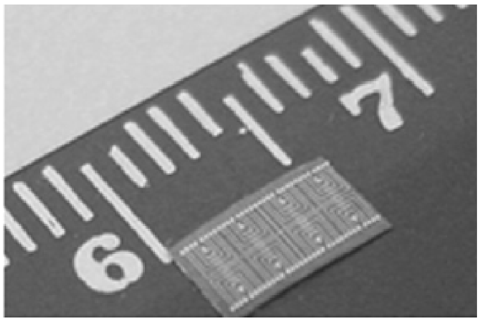


**Fig. 18.** Array of 8 × 8 temperature sensor of size 2.5 mm × 5.5 mm on PDMS [81]. Reproduced from S. Y. Xiao, L. F. Che, X. X. Li, Y. L. Wang, A novel fabrication process of MEMS devices on polyimide flexible substrates, *Microelectronic Engineering,* Elsevier, 85, pp. 452-457 (2008) © Elsevier.

## 7. Conclusion

Presently, microsystem technology is one of the most promising technologies. MEMS technology created the feasibility of making monolithic systems which was not feasible with IC technology. Due to its benefits of compactness, low DC power consumption, and to realize monolithic integrated system, this is one of the fastest growing technologies. Despite many advantages of MEMS technology, this technology is not much used in field due to its issues of high fabrication cost and integration issues. In conventional systems, MEMS component are realized on semiconductor substrate using micromachining techniques and packaged individually to integrate in system. These issues can be overcome with non-silicon fabrication technologies where MEMS as well as other components can be fabricated on the same board. This paper provides an idea about various non-silicon MEMS fabrication technologies with an overview of their applications in MEMS/RF MEMS.

Recent years witnessed significant research activities and remarkable advances in development of microsystems. In this regard, need was felt to review the evolution of non-silicon microfabrication technologies for microsystems. This paper will help the researchers to select fabrication technology depending on application, available fabrication facility, and cost.

## Acknowledgment

The author would like to thank Prof. K. J. Vinoy, Microwave Laboratory, Department of Electrical Communication Engineering, Indian Institute of Science, Bangalore, for his guidance and support throughout this work. I would like to thank Mukesh, working in Samsung, Bangalore, India for his help in finalizing the manuscript.

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**Sensors & Transducers Journal**

# Guide for Contributors

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## Aims and Scope

*Sensors & Transducers Journal (ISSN 1726-5479)* provides an advanced forum for the science and technology of physical, chemical sensors and biosensors. It publishes state-of-the-art reviews, regular research and application specific papers, short notes, letters to Editor and sensors related books reviews as well as academic, practical and commercial information of interest to its readership. Because of it is a peer reviewed international journal, papers rapidly published in *Sensors & Transducers Journal* will receive a very high publicity. The journal is published monthly as twelve issues per year by International Frequency Sensor Association (IFSA). In additional, some special sponsored and conference issues published annually. *Sensors & Transducers Journal* is indexed and abstracted very quickly by Chemical Abstracts, IndexCopernicus Journals Master List, Open J-Gate, Google Scholar, etc. Since 2011 the journal is covered and indexed (including a Scopus, Embase, Engineering Village and Reaxys) in Elsevier products.

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Contributions are invited on all aspects of research, development and application of the science and technology of sensors, transducers and sensor instrumentations. Topics include, but are not restricted to:

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- Sensor instrumentation;
- Virtual instruments;
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