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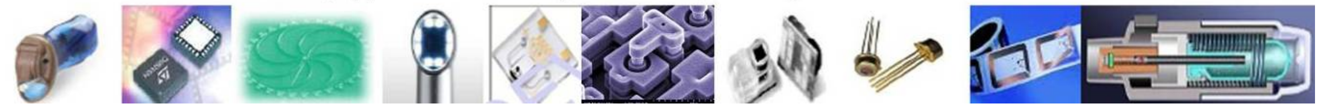

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The Impact of High Dielectric Permittivity on SOI Double-Gate Mosfet Using Nextnano Simulator

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Abstract: Performance of high-k Double-Gate SOI MOSFETs is studied and compared to silicon dioxide based devices. This is achieved by computing variation of threshold voltage, swing subthreshold, leakage current and drain-induced barrier lowering (DIBL) with respect to different gate bias (V_G) when gate length (L_G) decreases. This comparison is pinpointed taking SiO_2 and HfO_2 as gate oxides. Furthermore, quantum effects on the performance of DG MOSFETs are discussed. It is observed that less EOT with high permittivity reduces the tunnel current and serves to maintain high drive current, when compared with device using SiO_2 dielectric. Our results show that the characteristics of SOI Double Gate MOSFET with HfO_2 are superior to that of a device with SiO_2 dielectric. *Copyright © 2012 IFSA.*

Keywords: DG-MOSFET; Quantum effects; Nextnano3d; Modeling.

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1. Introduction

Over the past years, silicon-based electronic technology has been improved through downscaling MOSFETs, resulting in higher device performance and density. However, it has been expected that this downscaling will reach its limits about the gate of 5 nm around the year 2020 or so. The 2006 edition of the ITRS (International Technology Roadmap for Semiconductors) forecasts a minimum feature size of 18 nm-node, a physical gate length of 7 nm for the year 2018 [1]. According to ITRS, a very thin gate insulator with EOT (Equivalent Oxide Thickness) less than 1 nm is required for both high performance and low power consumption CMOS devices. The thinner oxide lets more current leak between the gate and the substrate, driving up power consumption and better on- and off-state control [2]. In order to obtain a very thin EOT, we need to use high-k gate insulator such as HfO2 which is the most promising candidate, since it possesses high dielectric constant and good thermal stability in contact with silicon [2, 3].

Another way to overcome short channel effects (SCE) is the use of multiple-gate structures on undoped SOI (Silicon On Insulator). One of these architectures is the Double Gate MOSFET (SOI DG-MOSFET) intended to control the channel very efficiently by applying a gate contact to both sides of the channel [4]. The intrinsic channel Double Gate MOSFET needs to rely solely on gate work function to achieve multiple threshold voltages on a chip due to the absence of body doping, which is efficient tool to adjust the threshold voltage in Double Gate MOSFET with doped channel [5, 6].

From the very beginning of semiconductor technology, it was thought that numerical, physics-based analysis of devices could help a great deal in their understanding. Nowadays, simulation and modeling of semiconductor devices have become one of the most important development methodologies in industry and research alike [7]. In this work we use the nextnano code to simulate a DG-MOSFET with high-k gate dielectric. This simulation tool is based on the self-consistent solution of the Schrödinger, Poisson and current equations [8, 9]. The coupled Poisson-Schrödinger system is solved by an approximate quantum charge density, which is employed inside of Poisson's equation in order to estimate the dependence of the density on the potential through Schrödinger's equation. Using this estimator the coupling between both equations is much decreased and rapid convergence is achieved. The electronic structure is calculated within a single-band or multiband k .p envelope function approximation. The included model for the carrier transport is a Wentzel–Kramer–Brillouin (WKB)-type approach also known as quantum-drift-diffusion (QDD) method, where the carriers are locally in equilibrium, charactized by a local Fermi level [10, 11].

The outline of the paper is as follows. Section II describes device structure. Section III presents some theoretical aspects. Section IV shows the simulation results using Quantum-drift-diffusion method. Using different gate oxide, the DIBL, subthreshold slope, and I_{on} current versus I_{off} current under different EOT are presented and compared, also the gate direct tunneling current as function of the gate voltage are presented. Section V concludes the paper.

2. Device Structure

The structure of the proposed device is shown in Fig. 1.

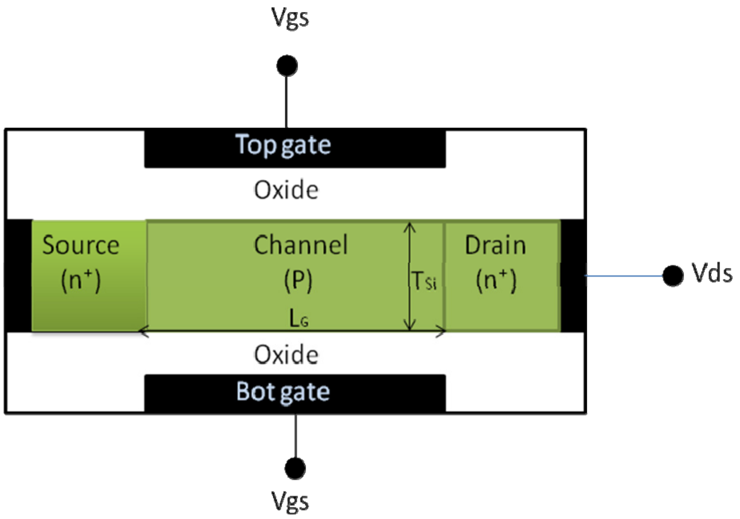

Fig. 1. Symmetrical DG-MOSFET considered in this work.

This symmetric structure is characterized by p-type doped Si channel of width 5 nm. This channel is embedded between two heavily n-doped source and drain regions of length 10 nm that are connected to source and drain contacts. The junctions are assumed to be abrupt. The doping concentration of channel and source/drain are 10^{16} cm^{-3}, 10^{20} cm^{-3} respectively. The polysilicon gates with work function 4.1 eV are separated from the Si channel by an oxide layer and the power supply voltage V_{DD} is 0.7 V. A channel length of 7 nm is chosen to study the performances of the device and kept constant for easy comparison. At this channel length limits, the susceptibility of the transistor to short channel effects (SCE) is monitored in several ways such as threshold voltage (V_{TH}), leakage current (I_{off}) and drain induced barrier lowering (DIBL). An even higher I_{on} current and decreased subthreshold slope can be obtained by the careful choice of a gate dielectric. In this way we take different oxide thickness (5 nm, 1.5 nm, 1 nm and 0.8 nm) with two Si channel width (5 nm and 3 nm) for both SiO_2 and HfO_2.

3. Theoretical Aspects

The model of carrier transport used in this paper is the quantum-drift-diffusion model as implemented in nextnano. This model uses the first moment of the Boltzmann equation to determine the current and the quantum mechanics to calculate the carrier density.
The basic equations are as follows:
The Poisson equation:

$$\nabla\uparrow 2\ (= q/\varepsilon \cdot (n - p - C)\ , \tag{1}$$

Here φ denotes the electrostatic potential, q is the elementary charge, C is the net ionized dopant charge density, ε is the static permittivity and n, p are electron and hole densities.

The electron and hole densities are determined by the continuity equation:

$$\nabla \vec{J}_{\lfloor} n - q\ (n/(t = q \cdot R\ , \tag{2}$$

$$\nabla \vec{J}_{\lfloor} p - q\ (p/(t = -q \cdot R\ \ , \tag{3}$$

where J_n and J_p are the electron and hole particle current densities.

The current relations for electrons and holes:

$$\vec{J}_{\lfloor} n = q \cdot n \cdot (_{\lfloor} n \cdot \vec{E}_{\lfloor} n + q \cdot D_{\lfloor} n \cdot \nabla_{\lfloor} n\ , \tag{4}$$

$$\vec{J}_{\lfloor} p = q \cdot p \cdot (_{\lfloor} p \cdot \vec{E}_{\lfloor} p\ \ - q \cdot D_{\lfloor} p \cdot \nabla_{\lfloor} p\ , \tag{5}$$

here μ_n, μ_p are the mobilities, and $D_{n;p}$ are the diffusion constants.

The charge density $n_c(x)$ for carriers of type c is calculated by assuming the carriers to be in a local equilibrium characterized by local quasi-Fermi levels $E_{FC}(x)$

$$n_c(x) = \sum_i \left|\psi_{ic}(x)\right|^2 f\left(\frac{E_{Fc}(x) - E_{ic}}{k_B T}\right), \tag{6}$$

ψ_{ic} and E_{ic} are respectively wave function and energy of eigenstate i that have been obtained from solving the multiband Schrodinger-Poisson equation [8].

The local quasi-Fermi levels $E_{F,c}(x)$ are determined by global current conservation $\nabla \cdot j_C = 0$, where the current J_c is assumed to be given by the semi-classical relation:

$$j(x) = \mu(x)n(x)\nabla E_{F,n}(x), \tag{7}$$

The EOT (Equivalent Oxide Thickness) used in this work is that obtained by classical Electrostatic theory in planar devices where [12]:

$$EOT = \frac{k_{SiO_2}}{k_{high-k}} T_{high-k} = 0.18\, T_{high-k}, \tag{8}$$

The SiO_2 and HfO_2 permittivities (k_{SiO2}, k_{high-k}) are 3.9 and 21.2 respectively, T_{high-k}: high-k material thickness.

Due to the increase of the gate dielectric thickness, the leakage current I_g by tunnel effect is then significantly reduced .Indeed, this one decrease exponentially with the gate dielectric thickness [13, 14].

$$I_g = \frac{A}{T_{high-k}} \exp\left[-2T_{high-k}\sqrt{\frac{2m^* q}{\hbar^2}\left(\Phi_B - \frac{V_{high-k}}{2}\right)}\right], \tag{9}$$

with:

A: constant;
m^*: carriers effective mass;
q: electron charge;
$\hbar$: Planck constant;
ΦB : unevenness between the level of the Si conduction band and high k material;
V_{high-k} : Loss of voltage through the dielectric.

For long channel devices, the sub-threshold slope, which is the gate voltage excursion required to increase the drain current by one decade in the weak inversion regime, results from the voltage sharing between the gate dielectrics and the depletion region of the transistor. It is expressed as:

$$S = \frac{KT}{q}\ln(10)\left[1 + \frac{Cdep}{Cox}\right], \tag{11}$$

where k is the Boltzmann constant, q the elementary charge, T the temperature, $Cdep$ and Cox the depletion and the gate oxide capacitances, respectively.

While in bulk MOSFETs, the depletion capacitance is about one third of the gate capacitance, leading to typical sub-threshold values of 80mV/dec, the depletion charge in thin film devices is simply the product of the channel doping times the film thickness. This charge is thus independent from the gate voltage and, consequently, the depletion capacitance $Cdep$ is null, which gives an ideal sub-threshold swing of 60 mV/dec at room temperature [15-17].

The use of a thin silicon active film allows a significant reduction of the capacitive coupling between the source/drain electrodes and the channel. Short channel effects are then mainly controlled by adjusting first the thickness of the silicon film, and second the gate dielectric thickness. That way, very good MOSFET electrostatic control (DIBL below 100mV/V and sub-threshold swing below 80mV/dec) can be achieved when the ratio between the channel length and the film thickness ratio (L_{ch}/T_{Si}) is larger than 4. [18, 19].

Threshold voltage is reduced because of SCE and DIBL according to the following relation:

$$V_{TH} = V_{TH0} - \alpha \frac{\varepsilon_{Si}}{\varepsilon_{ox}} EI (V_{bi} + V_{DS}) \ , \tag{12}$$

where V_{TH0} is the long-channel threshold-voltage, V_{TH} is the short-channel threshold-voltage, α is a constant, epsilon Si is the dielectric constant of silicon, epsilon ox is the dielectric constant of the gate oxide, V_{bi} is the built-in voltage between source and drain, and V_{DS} is the applied bias between them. Keeping all other parameters constant, threshold voltage is reduced by increasing the factor EI (electrostatic integrity) which is a function of channel and oxide thicknesses [20]. For a conventional MOSFET the EI relation is given by the voltage doping transformation model as:

$$EI = \left[1 + \frac{T_{Si}^2}{L_{el}^2}\right] \frac{t_{ox} t_{dep}}{L_{el}^2} \ , \tag{13}$$

EI increases if channel length L_{el} is decreased. In order to limit the increase in I, the thicknesses of oxide and depletion (in the numerator) have to be decreased. There is a limit to how small these thicknesses can be made. Now the EI relation for a DGFET is given by:

$$EI = \left[1 + \frac{\left({T_{Si}}/{2}\right)^2}{L_{el}^2}\right] \frac{[(\frac{(t]_{ox}}{2})(\frac{t_{dep}}{2})}{L_{el}^2} \ , \tag{14}$$

In other words, all the terms in the numerator are reduced by half, hence relaxing the need to reduce the thicknesses to a very small scale. This also means that for the same channel length, and oxide and channel thicknesses, EI of a DGFET is a fraction of that of a conventional MOSFET.

4. Results

Using the proposed model, the DIBL is calculated for $V_{DS} = 50$ mV and plotted as a function of the oxide thickness (EOT) in Fig. 2. The evolution of the barrier for T_{Si} varying between 5 nm and 3 nm illustrates clearly the dependence of the drain-induced barrier lowering (DIBL) on permittivity and Si channel width. The range of variation of the DIBL for SiO_2 based device is from 0.02 eV for $T_{Si} = 5$ nm to 0.063 eV for T_{Si}=3 nm. The DIBL is decreased for HfO_2 based device and varies from 0.015 eV for T_{Si}=5nm and 0.023 eV for T_{Si}=3 nm. From this figure it can be concluded that HfO_2 has a great impact on the reduction of DIBL.

Fig. 3 illustrates the effect of high permittivity on subthreshold slope. It is well known that a small subthreshold slope is highly desired since it improves the ratio between the on- and off-currents. It is clear from Fig. 3 that for SiO_2 the subthreshold slope is degraded by almost 400 % when the oxide thickness is reduced from 0.8 nm to 5 nm for a channel width of 5 nm. While for HfO_2 the subthreshold slope is less degraded (only 148 %) for the same channel width. The figure also show that reducing the channel width (T_{Si}) to 3nm the same trends as already are observed for both SiO_2 and

HfO_2. The subthreshold slope takes a minimum value 90 mV/dec at EOT=1.5 nm. We can conclude that subthreshold characteristics of SOI DGMOSFET based HfO_2 are clearly better than SiO_2 based device, but remains far from ITRS recommendation as the subthreshold slope S should not be higher than 80 mV/dec.

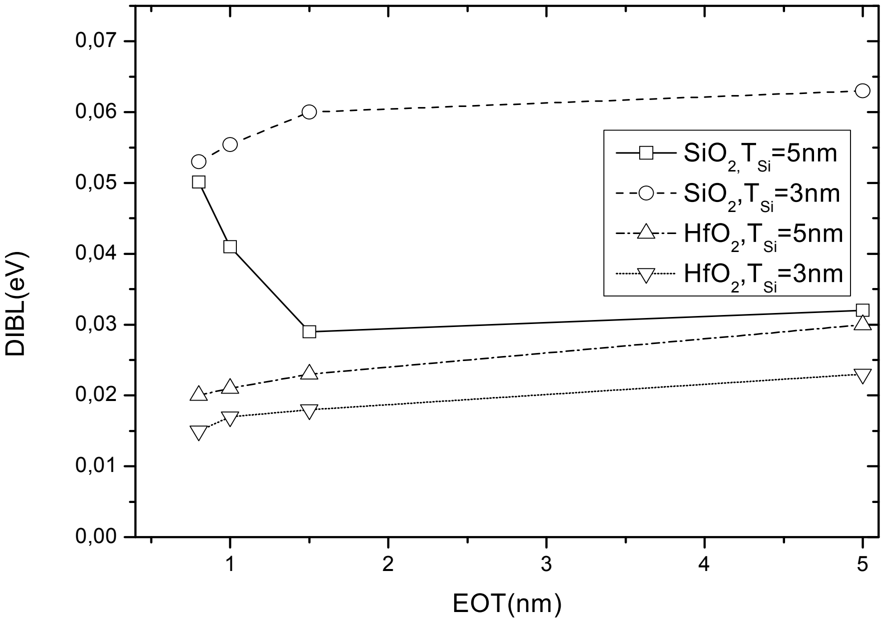

Fig. 2. DIBL as a function of the oxide thickness EOT (nm).

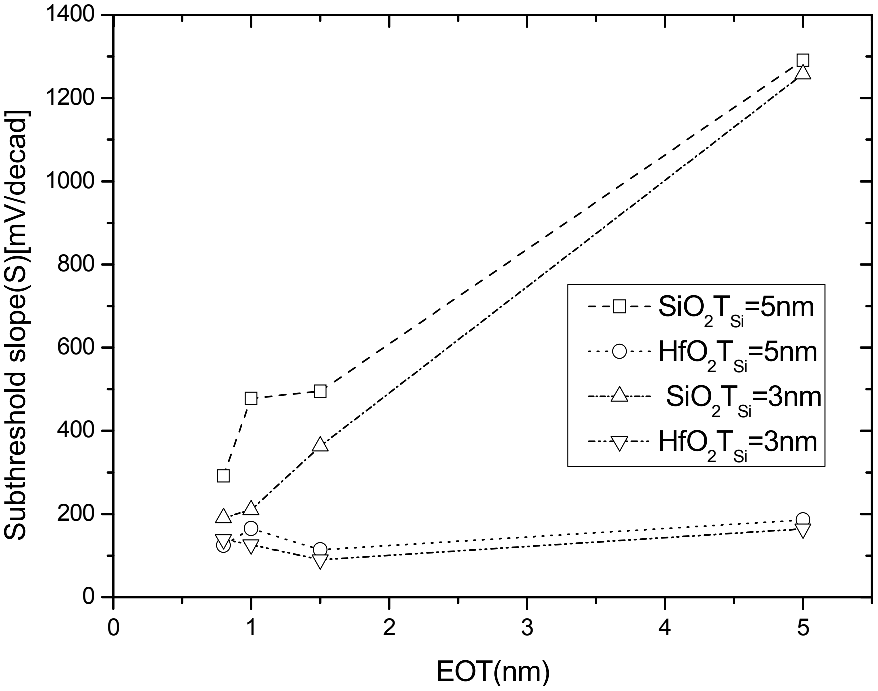

Fig. 3. Subthreshold slope as a function of EOT.

It is well-known that gate leakage current is negligible compared to on-state current of MOSFETs, however it dominates in stand-by mode. Following this statement we show in Fig. 4 and Fig. 5 the gate direct tunneling current as function of the gate voltage at V_{DS}=V_{DD}=0.7 V. The gate direct tunneling current becomes increasingly important when reducing the physical oxide thickness T_{ox} to 0.8 nm, and becomes much higher when replacing SiO_2 with HfO_2. For T_{ox} varying between 5 nm and 0.8 nm, the gate current increases from $9 \cdot 10^{-9}$ A/m to 0,14 A/m for SiO_2 and from 10^{-7} A/m to 2 A/m for HfO_2. In terms of equivalent oxide thickness we observe a slightly lower leakage current for HfO_2 compared to SiO_2.

The influence of the silicon channel width (T_{Si}) on the leakage current has been studied in order to investigate if it is possible to reduce the leakage current by adjusting the silicon channel width. It is well established that leakage current and short channel effects become more important when reducing the channel length.

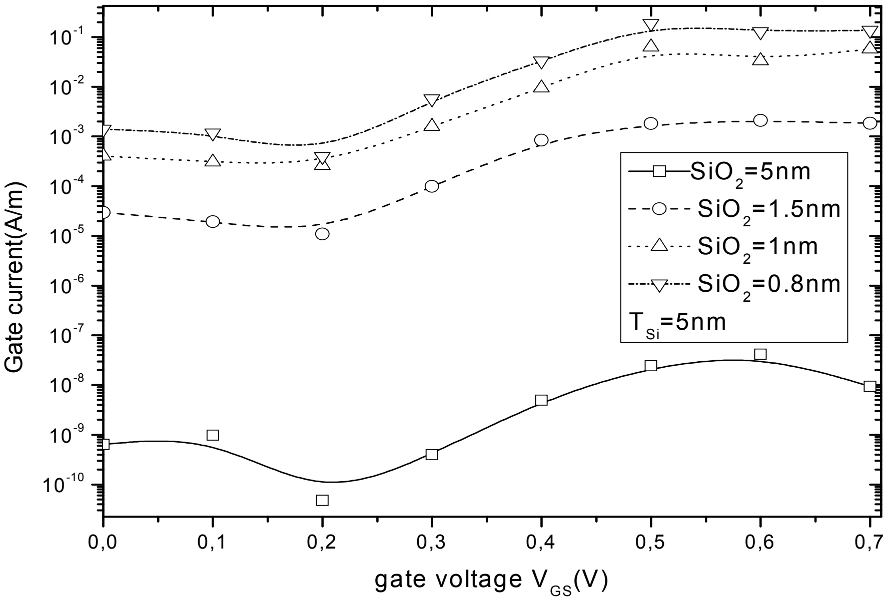

Fig. 4. Gate current as function of gate voltage for SiO_2.

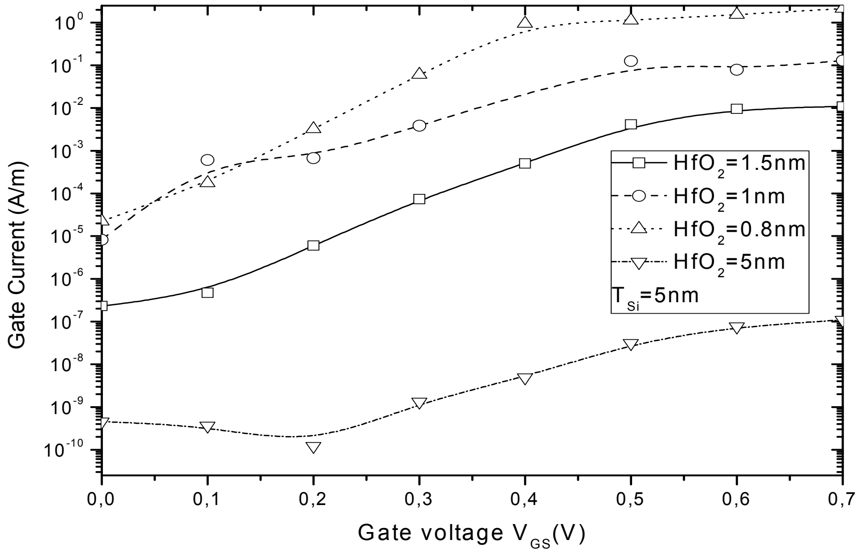

Fig. 5. Gate current as function of gate voltage for HfO_2

Fig. 6 and Fig. 7 show gate direct tunneling current as function of the gate voltage for T_{Si}=3 nm and at $V_{DS}=V_{DD}$=0.7 V. The same trends are observed as stated obove for T_{Si}= 5 nm. For a physical thickness T_{ox} varying between 5 nm to 0.8 nm the gate direct tunneling current increases from $3.6 \cdot 10^{-8}$ A/m to 0,31 A/m for SiO_2 and from $1.6 \cdot 10^{-7}$ A/m to 2,4 A/m for HfO_2. Taking into account that the EOT for HfO_2 is 0.18 of its physical thickness, we can conclude that HfO_2 is a best candidate for the reduction of the leakage current.

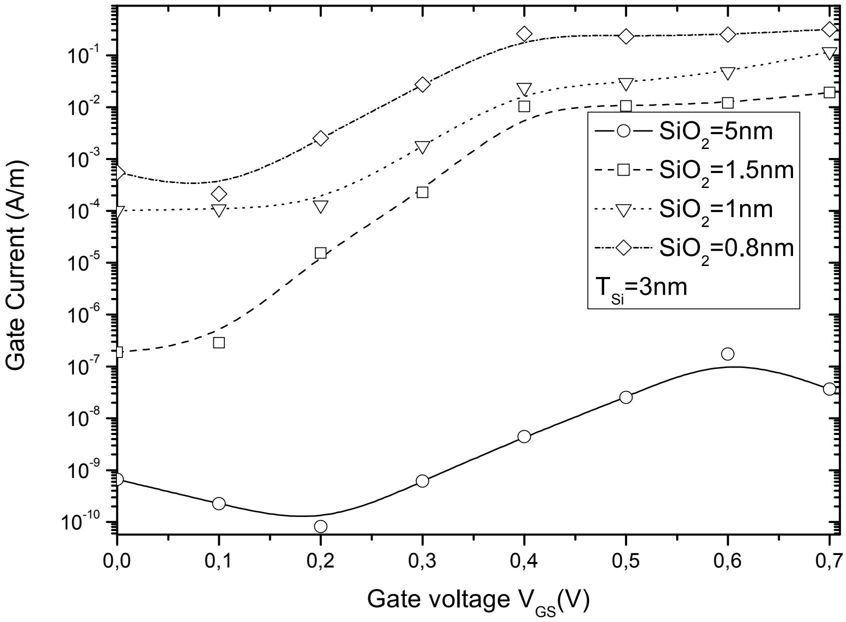

Fig. 6. Gate current as function of gate voltage for HfO_2.

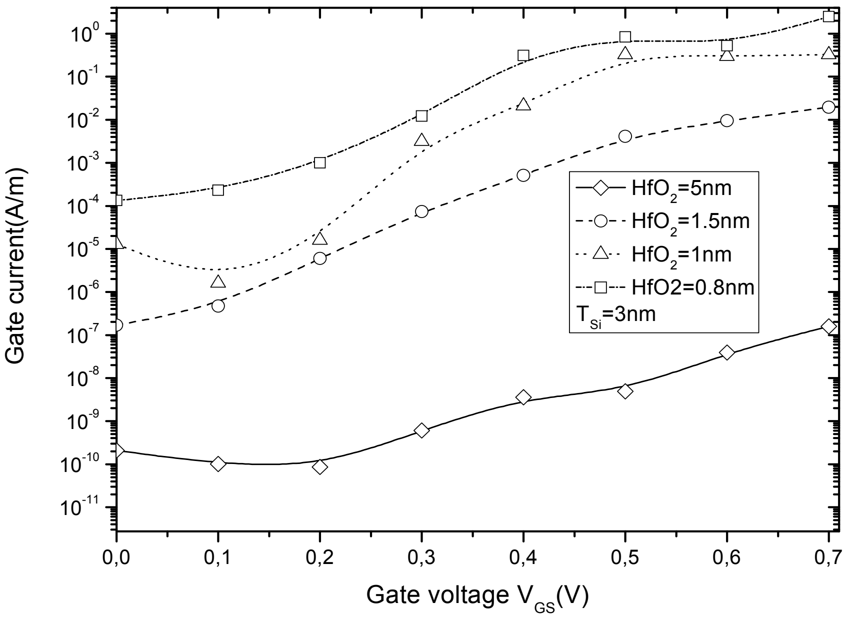

Fig. 7. Gate current as function of gate voltage for HfO_2.

Fig. 8 shows gate direct tunneling current as function of the gate voltage for $V_{DS}=V_{DD}$=0.7 V, V_{GS}=0.7 V.The gate direct tunneling current takes a minmum value when the oxide thickness is reduced from 0.8 nm to 5 nm for both channel widths.

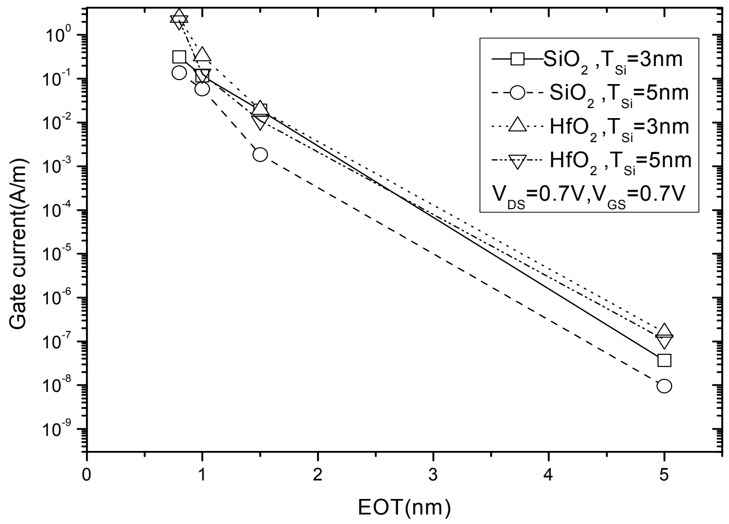

Fig. 8. Gate current as function of gate voltage for HfO_2 and SiO_2.

The I_{on} current versus I_{off} currrent for different EOT and for two channel width is represented in Fig. 9. The high permittivity increases I_{on} and decreases I_{off} for various EOT, for HfO_2 at EOT=0.8 nm, I_{on} current value tends towards 1002.02 A/m with I_{off} currrent value equal to 0.15 A/m, besides the SiO_2 I_{on} current value which is equal to 717 A/m with I_{off} currrent value equal to 35.208 A/m but when reducing the Si width channel to 3 nm, we obtained a little values for I_{on} current and I_{off} currrent than 5 nm width channel, in this case I_{on} current is much weak, which is cannot meet the ITRS predicted value.

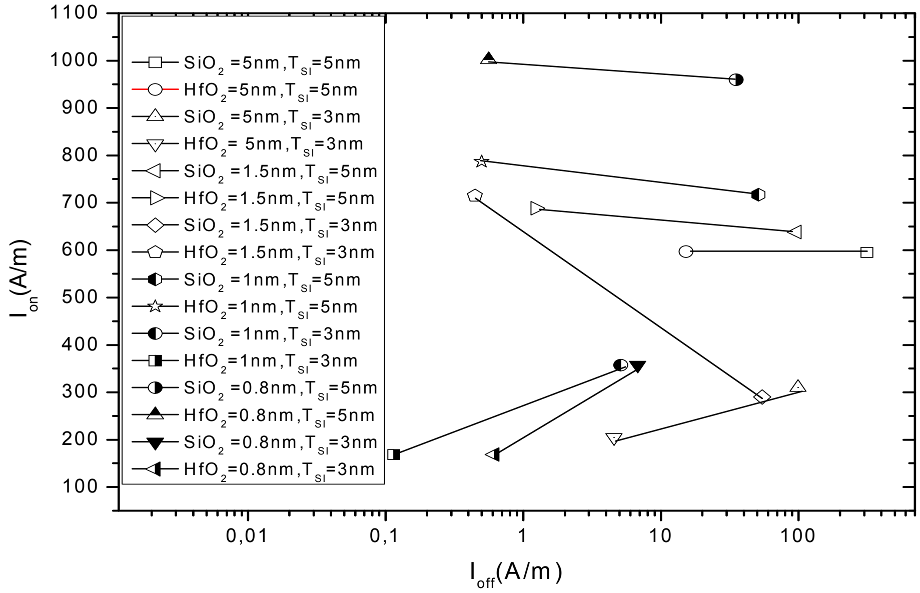

Fig. 9. I_{on} as As a function of I_{off}.

The conduction band and electron density for SiO_2 and HfO_2 along the DG in the centre of the body ($y=T_{Si}/2$) are plotted in Fig. 10, Fig. 11 for two different bias voltages .The conduction band edge at 0.7 V gate voltage for both SiO_2 and HfO_2 is labelled with ‘cb’ and the quantum electron density with ‘e q D’. The conduction band in the Si channel is lower than Fermi level .The Fermi level is almost flat equal to -0.35 eV for SiO_2 and in the case of HfO_2 is equal to -0.27 eV.

For different gate bias voltages as shown in the figures of electron density, the HfO_2 electron density significantly differs from SiO_2 thus it varies from $5.451 \cdot 10^{18}$ cm^{-3} to $0.89 \cdot 10^{18}$ cm^{-3} respectively at V_{GS}=0.7 V and V_{GS}=0 for SiO_2 and from 25.410^{18} cm^{-3} to 0.15310^{18} cm^{-3} respectively at V_{GS}=0.7 V and V_{GS}=0 for HfO_2.

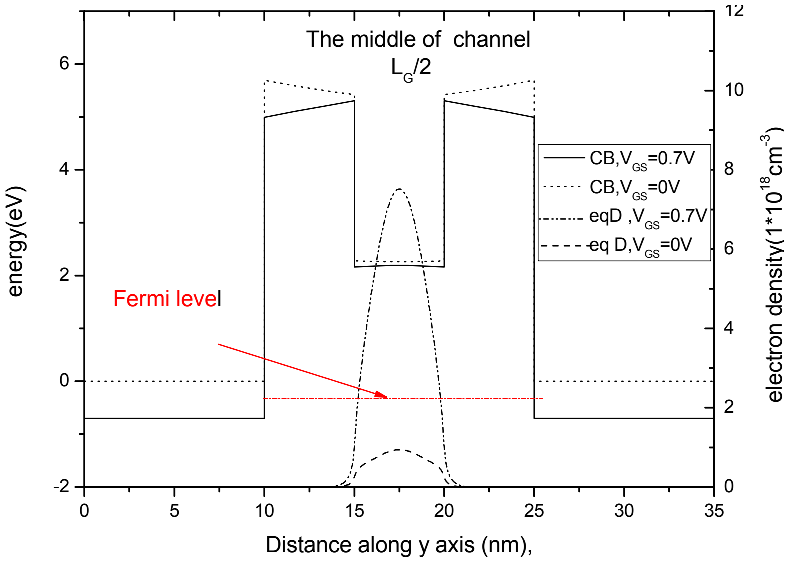

Fig. 10. Conduction band and electron density of SiO_2 along the y-axis.

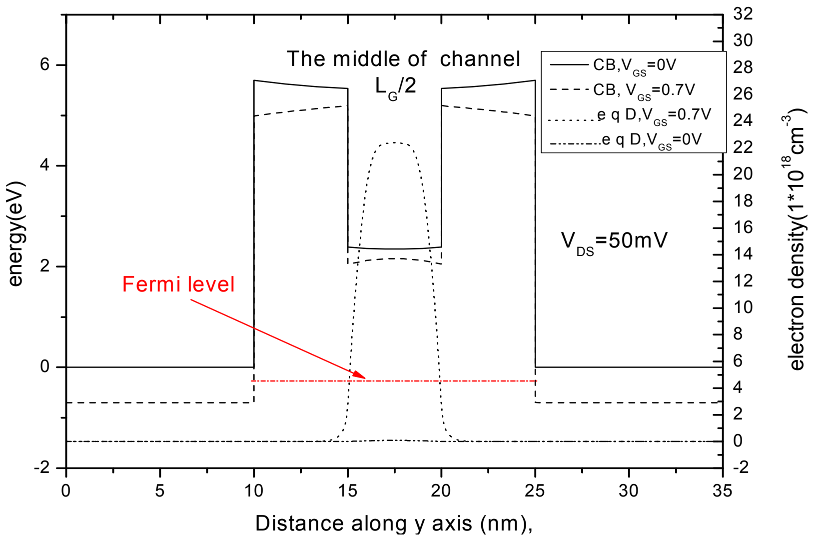

Fig. 11. Conduction band and electron density of HfO_2 along the y-axis.

The electron density along the DG in the centre of the body ($y=T_{Si}/2$) are plotted in Fig. 12, Fig. 13 for different EOT for both HfO_2, SiO_2.

Electron density for SiO_2, HfO_2 as shown in Fig. 12, Fig. 13, these figures show a slice through the middle of the device ($y=T_{Si}/2$=constant) under a drain bias of 50 mV. It can clearly see that the electron density has the highest values in the middle of the channel and not at the Si/SiO_2 and Si/HfO_2 interfaces. The quantum mechanical density is practically zero at the Si/SiO_2 and Si/HfO_2 interfaces because due to the SiO_2 and HfO_2 barriers, the wavefunctions tends to zero at the Si/SiO_2 and Si/HfO_2 interfaces.

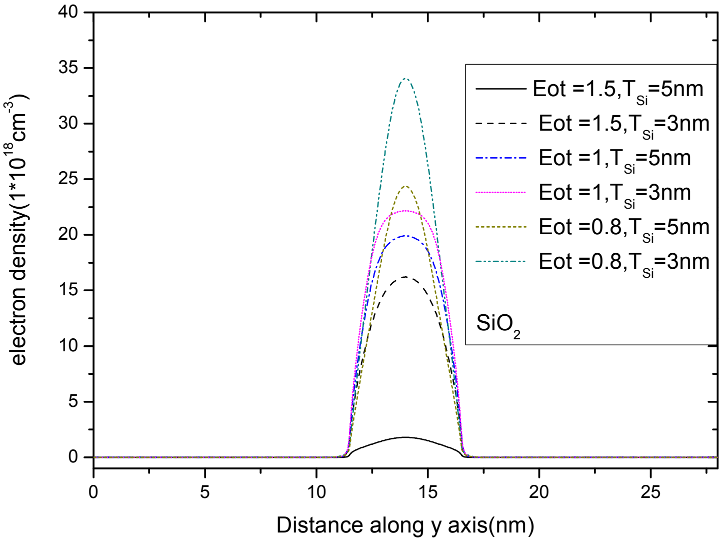

Fig. 12. Electron density as function of y axis.

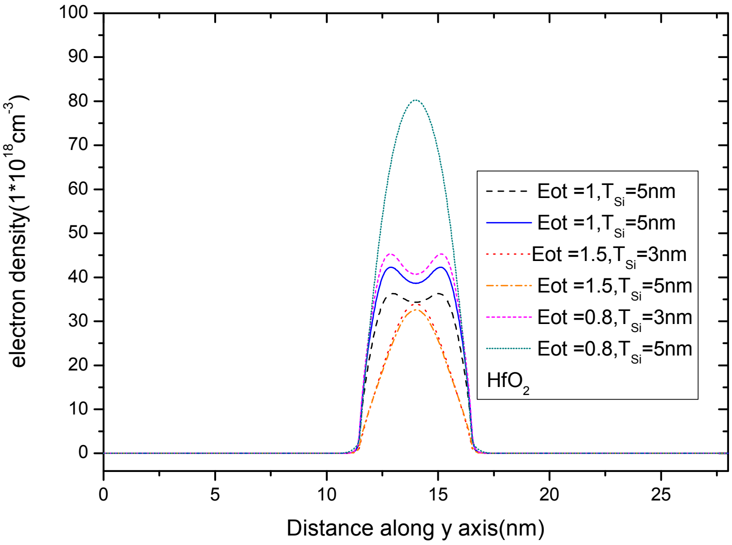

Fig. 13. Electron density as function of y axis with different EOT.

For gate bias voltage equal to 0.7 V as shown in the figures of electron density, the HfO_2 electron density significantly differs from SiO_2 and takes its maximum when reducing T_{Si} to 3 nm. Table 1 confirms these results, the SiO_2 electron density for various EOT varies from $6.741\cdot10^{18}$ cm^{-3} to $24.54\cdot10^{18}$ cm^{-3} at T_{Si}=5 nm and from $16.15\cdot10^{18}$ cm^{-3} to $34.17\cdot10^{18}$ cm^{-3} at T_{Si}=3 nm; the HfO_2 electron density for various EOT varies from 31.9510^{18} cm^{-3} to 45.57 at T_{Si}=5 nm and from 3 3.9510^{18} cm^{-3} to 80.48310^{18} cm^{-3} at T_{Si}=3 nm for HfO_2.

Table. 1. Comparison between HfO_2, SiO_2 Electron density.

EOT	**T_{Si}=5 nm, SiO_2 Electron density ($1*10^{18}$ cm^{-3})**	**T_{Si}=5 nm , HfO_2 Electron density ($1*10^{18}$ cm^{-3})**	**T_{Si}=3 nm , SiO_2 Electron density ($1*10^{18}$ cm^{-3})**	**T_{Si}=3 nm , HfO_2 Electron density ($1*10^{18}$ cm^{-3})**
1.5 nm	6.74	31.95	16.15	33.95
1 nm	19.8	36.35	22.17	42.36
0.8 nm	24.54	45.57	34.17	80.48

5. Conclusions

In order to improve subthreshold slope and to suppress drain-induced barrier lowering in SOI MOFET, double gate architecture and high-k dielectric are introduced in this paper. The simulations were conducted using the nextnano code which uses a quantum-drift-diffusion model for carrier transport taking into account quantum confinement effects. It s concluded that hafnium oxide is one of the best candidate to replace SiO_2, due to its extremely high subthreshold slope. Also HfO_2 is effective at reducing I_{off} current and maximizing the ratio of I_{on}/ I_{off}.

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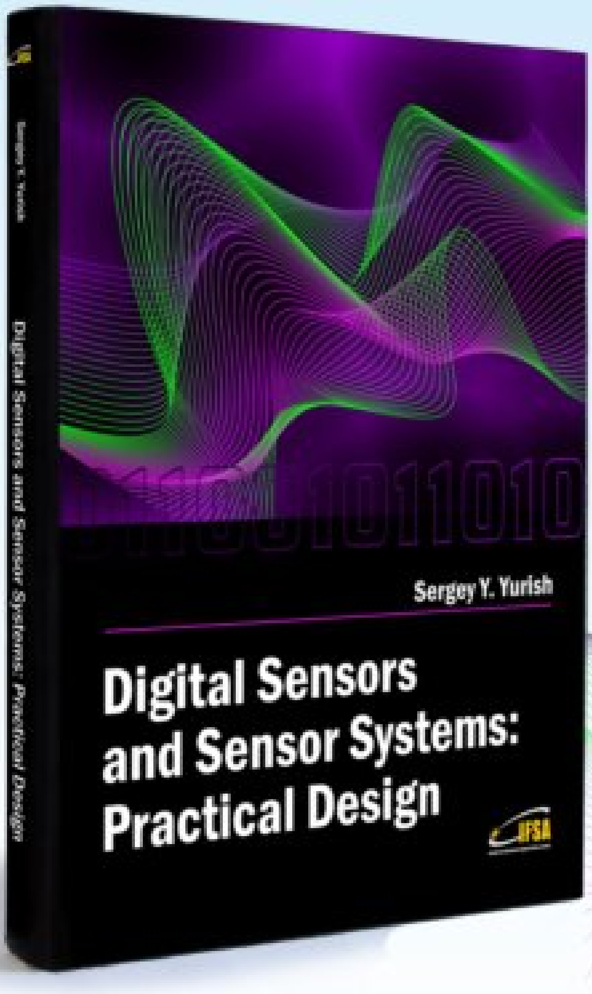
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