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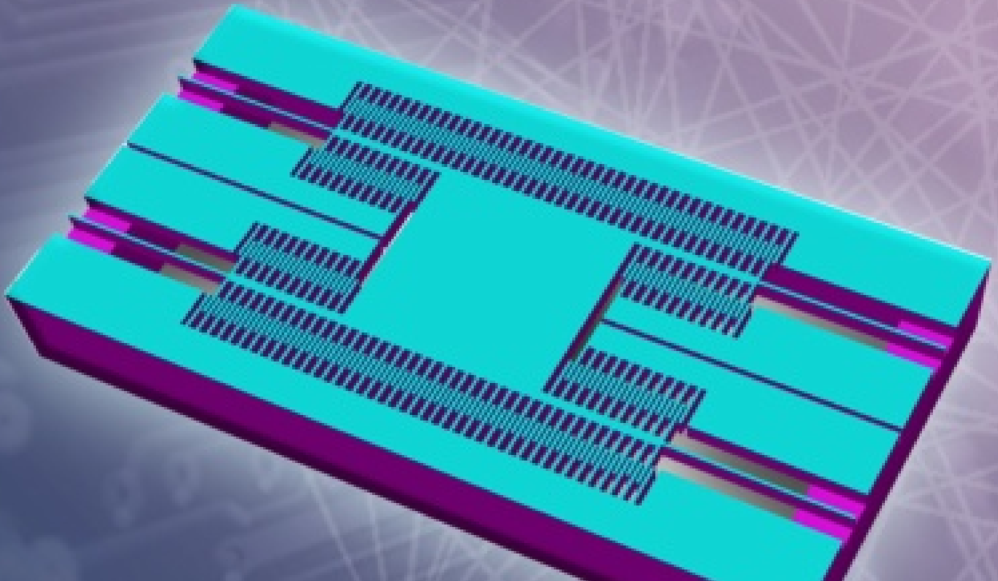

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DC Characterization and Post-CMOS Processing of a Microcantilever Sensor

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Abstract: Microcantilever sensors have attracted marvelous consideration in recent years and numerous chemical and biological detections have been performed. Monolithic integration of a microcantilever with the signal processing electronics can not only lower the sensor development cost but also reduce the total system size. However, the curling of the microstructures fabricated in the composite metal–oxide thin-film of the CMOS-MEMS process, greatly affects the overlapping area between the static and moveable capacitive comb fingers and hence offers potential challenges in capacitive sensing. This paper reports fabrication of a microcantilever using post-CMOS micromachining technique. Backside deep reactive ion etching is used to keep a silicon layer attached with the thin-film and hence control the buckling of the cantilever. DC characterization of the sensor has been carried out. The experimental results are compared with the theoretical model, in order to estimate any manufacturing tolerance caused deviation of the parameters from the designed values.

Keywords: CMOS-MEMS, DRIE, Post-CMOS, MEMS, Microcantilever sensor.

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1. Introduction

MEMS based microcantilever sensors are emerging as innovative devices in physical, chemical, and biological fields due to low fabrication cost, small size and low power consumption [1-5]. A microcantilever is a simple MEMS structure whose process of micromachining is easy in the mass production phase. The microcantilever sensors provide promising sensor solutions that are accurate, reliable and portable. Furthermore, there are evidences that microcantilever based sensors are very sensitive; for example, gases in parts per billion [6] and even mass measurements at attogram level [7] have been reported. In order to turn a microcantilever into a chemical sensor, it has to be coated with an adsorbent layer. The analyte molecules from the surrounding environment are captured in the adsorbent layer. The microcantilever chemical sensor can be operated into two modes; static and dynamic. An excitation mechanism, in the dynamic mode, is used to actuate the cantilever at its resonance frequency, and the shift in the resonance frequency caused by analyte adsorption is sensed, whereas in the static mode the deflection of the microcantilever, due to the adsorption of the analyte is measured.

CMOS technology is the most common fabrication technology for integrated circuits (IC) [8, 9]. The fabrication of new smart sensor systems has been realized in recent years due to the fast CMOS technology development. Monolithic micromachining of micromechanical components, which enables fabrication of multi element sensor arrays with micro-electronics on a single chip, is more beneficial as compared to the conventional technologies. Monolithic integration of micro devices not only minimizes the total system size but also reduces the manufacturing cost. In addition, with monolithic integration of the MEMS sensor with the signal processing electronics, the parasitic capacitances and resistances associated with interconnects between the MEMS structures and processing electronics are highly reduced. With a lower parasitic capacitances and resistances, one gets a higher signal to noise ratio and the efficiency of the sensor is enhanced.

There are three categories of the CMOS-MEMS technology, namely the pre-CMOS, intermediate CMOS and post-CMOS. The post-CMOS technology is important among mentioned categories. It has advantages of using in-born materials from CMOS technologies; leading to reduced prototyping time, maskless front side processing, and non-stick dry release. In principle, the CMOS thin film, deposited on the top of the wafer during CMOS process, can only be used as the structure of the microcantilever. However, in that case, the released MEMS structure is curled due to difference in residual stresses occurring in different layers. The curling of the microstructures greatly limits the device size [8, 9], creates packaging and coating issues. In addition, curling of the structural parts greatly affects the overlapping area between the static and moveable capacitive comb fingers and hence offers potential challenges in capacitive sensing. Deep reactive ion etching (DRIE) technologies can be used to achieve high aspect ratios from 20:1 to 30:1 and has the ability to control the curling formation in structure by adding underneath silicon with the CMOS thin film [8, 9].

This paper reports post-CMOS MEMS processing and DC characterization of a cantilever based sensor.

2. Design of the Microcantilever Sensor

As the target foundry for the fabrication of the microcantilever was MIMOS Berhad, the design standards of the said foundry were followed. MIMOS CMOS 0.35 μm fabrication technology provides three conducting metal layers, insulation layers, and two polysilicon layers. The metals layers can be connected using vias. Layers consist of Aluminum, Silicon dioxide (SiO_2) and Tungsten which purposely act as conducting, dielectric and via respectively. A three dimensional view of the cantilever designed in CoventorWare software is asserted in Fig. 1.

A coil of 34 turns is employed by metal-2 layer for execution of electromagnetic actuation of the microcantilever. For capacitive sensing of the microcantilever displacement, two sets of capacitive comb fingers containing twenty fingers each have been designed at the free end of the cantilever. The spacing and overlapping length between the moveable and the fixed fingers are 3 μm and 90 μm respectively. The design parameters of the microcantilever sensor are given in Table 1. Silicon substrate of thickness 40 μm is added with the thin film in order to avoid buckling of the structure due to residual stresses. A fully differential Wheatstone bridge in ploy-1 layer has been designed at the maximum stress region; near the anchor for vibration sensing. The dual sensing mechanism has been implemented to study the influence of external parameters such as temperature and humidity on the two sensing mechanisms. The optimized design of the sensor in CoventorWare was later on transferred to Cadence software to ensure the fulfillment of foundry design rules. The final layout of the sensor, drawn in Cadence software and submitted to the foundry for fabrication, is shown in Fig. 2 indicating the metal coil, the capacitive comb fingers and polysilicon layers. Detailed work related to analytical modeling and simulation results of the electromagnetic actuation and capacitive sensing of our proposed sensor have already been reported in [10], while [11] discusses the detailed analysis of the piezoresistive sensing.

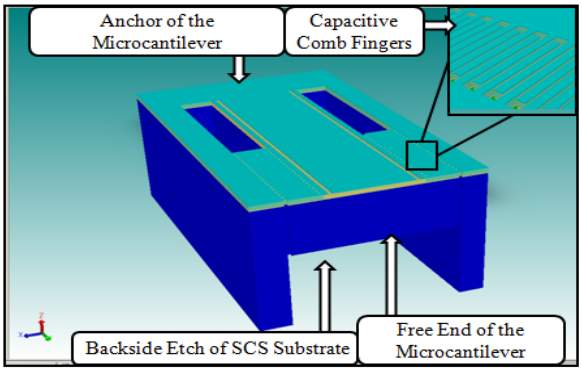

Fig. 1. Solid model of the microcantilever designed in CoventorWare.

Table 1. Device design parameters.

Parameter	Value (µm)
Length of cantilever	1000
Width of cantilever	300
Total thickness of Metal and oxide layers	4.543
Total Thickness of the cantilever	45
Length of the comb finger	100
Overlapping length of the fingers	90
Width of comb finger	6
Spacing between fingers	3

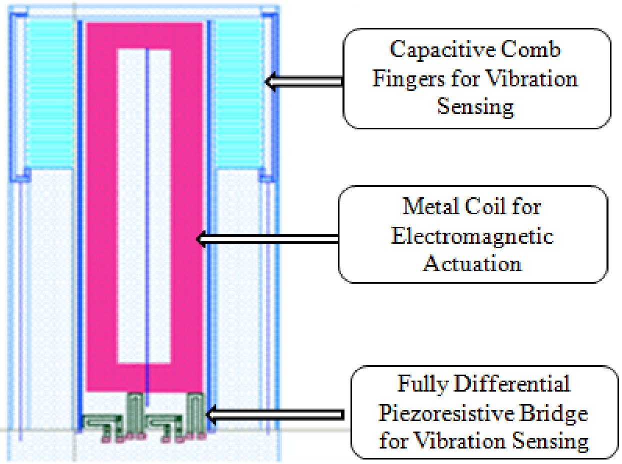

Fig. 2. Inverted color image of layout of the cantilever sensor in Cadence software.

3. Post-CMOS Processing

In the post-CMOS fabrication technique, after the CMOS fabrication step, further treatment is required to release the fabricated microcantilever sensor structure [12, 13]. DRIE process is used to etch the microcantilever using SF_6 and C_4H_8 as pulse gases. C_4H_8 first deposits a polymer film on the structure then SF_6 performs etching to remove the polymer film from the trench bottom by ion assisted etching. During this process, the sidewalls remain protected from ion bombardment. In the next cycle again C_4H_8 deposits a protective polymer film and then SF_6 pulse is fed into the reactor for etching. The process is repeated until desired etch thickness is achieved.

The schematic process flow of the post-CMOS processing of the microcantilever with the cross-section of the CMOS thin films and their spatial locations is illustrated in Fig. 3.

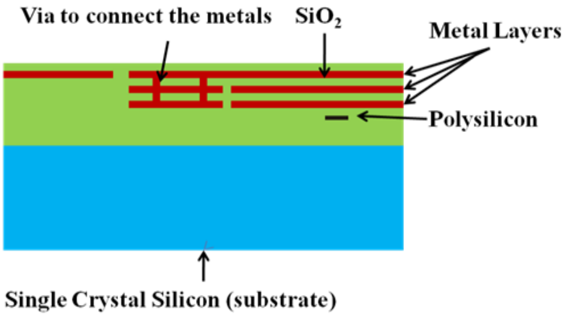

Fig. 3 (a). CMOS fabricated Chip.

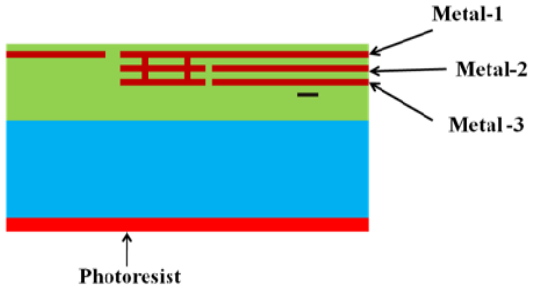

Fig. 3 (b). Photoresist coating on backside of the chip.

Fig. 3 (c). Backside etching by DRIE.

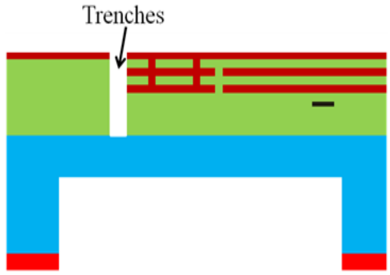

Fig. 3 (d). Anisotropic SiO_2 etching from front side.

Fig. 3 (e). Front side etching of Si by DRIE to release the structure.

The fabricated CMOS chip from foundry is shown in Fig. 3(a). First backside DRIE processing of the chip was completed. For this purpose a photoresist was applied on the backside of the wafer as shown in Fig. 3 (b). The photoresist was selectively patterned to expose sensor region by using the mask and photolithography procedure. In the next step to etch the silicon substrate anisotropically, a backside selective DRIE process was performed by using Tegal plasma etcher. During the etching process an optical microscope was used to monitor the thickness of the substrate. A single crystal Silicon (SCS) membrane of thickness ~40 µm was produced after successful etching process, as illustrated in

Fig. 3(c). To bring the thin film on upside, the die was then flipped and attached with an 8" carrier wafer using Kapton tape as shown in Fig. 4.

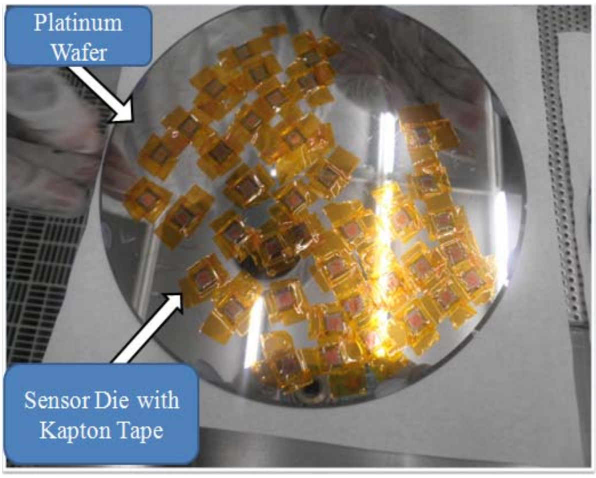

Fig. 4. Dies attached with an eight inch Platinum wafer with Kapton tape.

To process from the front side, first anisotropic SiO_2 reactive ion etching (RIE) was performed to open patterns of the composite beams as shown in Fig. 3(d). After an etching process of 5 minutes, the passivation layer was etched away, and the metal-3 layer was exposed. On vanishing of the passivation layer, its golden color was replaced with the white color of the metal layer as shown in Fig. 5(a) and 5(b). The etching process remained continued for 8 minutes, only then the gray color of silicon appeared in the trenches, which was the indication of the completion of SiO_2 etching. Using the SiO_2 etching rate of test structure, pre-estimated etching time was used to avoid over etching which can cause undesired under cuts. SiO_2 etching rate was found to be 0.56 µm/ min and the trench appearance was up to the SCS surface after the completion of SiO_2 RIE process.

(a) (b)

Fig. 5. Color change during Anisotropic RIE of SiO_2 (a) golden color of the sensor surface before RIE; (b) white color of the sensor surface after RIE.

In the final stage, bulk silicon DRIE process was done at an estimated etching rate of 4.4 µm/ min, obtained during previous back side etching. The sample was processed in the Tegal plasma etcher for 16 minutes. It was observed that, due to narrowness of the trenches, the etching rate for processing front side becomes less than that for backside. As a reference, test structures on the chip were used to monitor the etching process. The schematic cross-section of the sensor after the second silicon DRIE process is shown in Fig. 3(e) with all the trenches etched-through.

4. DC Characterization

DC characterization of the device is very important as an initial test to ensure the connectivity of the electrical connections and wiring, and to measure the values of the parameters of the sensor components. The designed sensor has six ports for biasing and feedback. Among these ports, two are used to energies the pickup coil for electromagnetic actuation, the other two are used to bias the fully differential piezoresistive bridge and the remaining two are used to get feedback from the mentioned bridge. The sensor has four polysilicon resistors, one pickup coil and two sets of capacitive fingers. Careful measurements of the parameters of aforementioned components are essential in order to define allowable biasing conditions for the sensor.

During characterization, for easy handling of the die, it was attached with a 4 inch test wafer. To bond the die with the carrier wafer one drop of SU-8-2000.5 photoresist was put on the carrier wafer and then chip was placed on it. The wafer was heated 8-10 minutes at 90 ^{o}C for soft baking of photoresist. The DC characteristics of the microcantilever sensor were examined by using a PE-4RF type probe station from Ever Being Int'l Corporation as shown in Fig. 6.

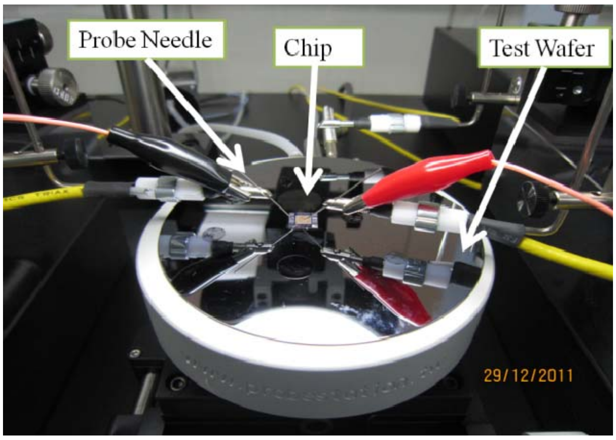

Fig. 6. Die under probe station for DC analysis.

The measured values of the parameters of the sensor were compared with the theoretical estimations carried out during the design stage. Such a comparison is deemed necessary in order to estimate any variation in the sensor parameters, due to manufacturing tolerances, which may influence the operating conditions of the sensor such as biasing voltage. Resistance of the metal coil for actuation and the polysilicon layer were calculated as [14],

$$R = \rho_s \frac{l}{w}, \tag{1}$$

where ρ_s, l and w are the sheet resistance, length and width of the layers respectively. The length of the wire of the coil was calculated as

$$l = N(l_o + l_i + w_o + w_i), \tag{2}$$

where N, l_o, l_i, w_o and w_i are the number of turns, outer length, inner length, outer width and inner width of the coil respectively. Table 2 shows designed values of the parameters of the polysilicon resistor and the coil.

Table 2. Parameter of the polysilicon resistor and actuation coil.

Parameter	Value
Length of the polysilicon resistor	190 µm
Width of the polysilicon resistor	10 µm
Outer length of the coil	900 µm
Inner length of the coil	766 µm
Outer width of the coil	250 µm
Inner width of the coil	118 µm
Sheet resistance of the coil	0.085 Ω/□
Sheet resistance of the polysilicon resistor	87 Ω/□

5. Result and Discussion

Detailed SEM imaging based analysis has been performed in order to observe the structural details and validate the geometrical properties of the cantilever against the designed geometry. Fig. 7 shows zoomed view of the capacitive comb fingers of the cantilever before post-CMOS processing. A well defined geometry can be observed. The two dimensional geometrical parameters were found in agreement with the designed values. A described in Section 2, a backside DRIE was first carried out in order to reduce the thickness of the underneath silicon to ~40 µm. The SEM image of the backside of the cantilever, taken after the aforementioned DRIE, is shown in Fig. 8. As a selective DRIE was carried out using a mask, a higher depth of the etched area with respect to the un-etched surface of the wafer can be observed. From this depth difference, knowing the total thickness of the wafer, one can estimate the remaining silicon thickness underneath the cantilever. The SEM image taken after front side RIE and DRIE is shown in Fig. 9 and a magnified view of the comb fingers is shown in Fig. 10. The cantilever is successfully released. There is no structure breakage and its surface is clean without debris. The features are very well patterned. The dimensions of the fabricated structure were found almost the same as in the design. A small curling can be observed in the comb fingers which has been caused by the stress in-homogeneity along the thickness. In-homogeneous stress is a result of the residual stresses in the stacked layers due to difference in the coefficient of expansion of the materials used. The added silicon layer underneath, has successfully controlled the magnitude of curling and it is much lower as compared to the magnitude one can expect with a finger in CMOS thin film only. There still exists an overlapping area between the static and the moveable fingers. There is no physical interference among the cantilever fingers. Therefore, a successful capacitive sensing is expected.

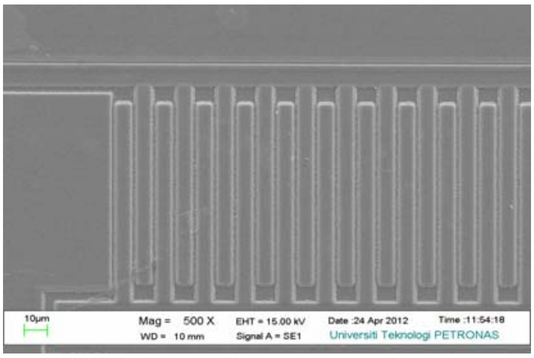

Fig. 7. SEM image of the capacitive comb fingers of the microcantilever before post- CMOS process.

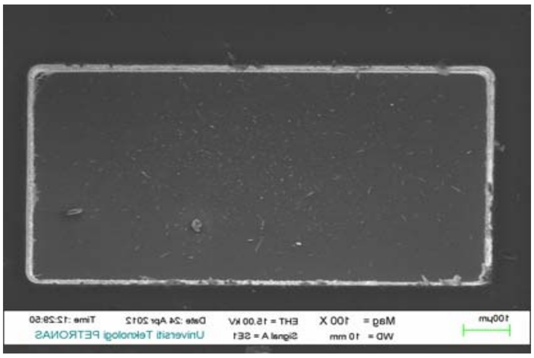

Fig. 8. SEM image of die after backside DRIE.

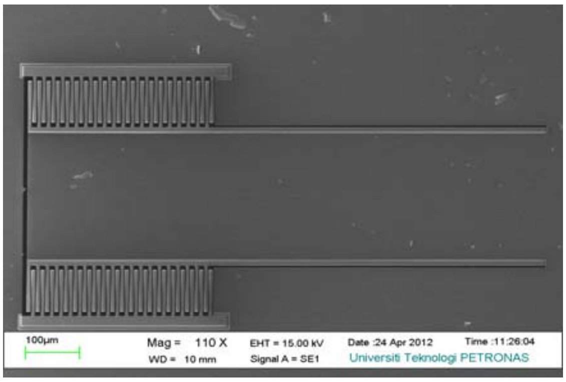

Fig. 9. SEM image of the microcantilever after front side DRIE and RIE.

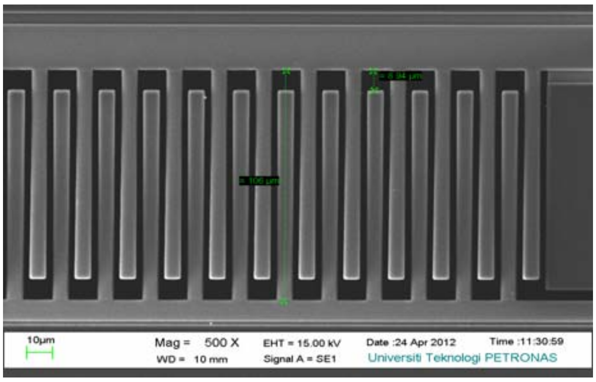

Fig. 10. SEM image of the capacitive combs of the cantilever.

Three dies were investigated for DC characterization of the microcantilever sensor. The experimentally measured resistances of the polysilicon resistors are shown in Table 3. The resistance values of the two ploysilicon resistors agree with each other within an RMS error range of 0.17 %. The average resistance value of the two polysilicon resistors was measured to be 2.15 kΩ. This shows a variation of 23 % with respect to the designed value of 1.65 kΩ. The Table 4 shows comparison of the experimentally measured resistances of the coil with the theoretically predicted resistance. Again, measurements were taken from three different chips. An average resistance of 6.32 kΩ was measured which is in agreement with the theoretically calculated value of 7.34 kΩ within a percentage error range of 16 %. The variation in measured resistances with the calculated resistances is credited to the variation in the sheet resistance of the metal-two layer and polysilicon layer from the typical values given in the design rules and manufacturing tolerance during fabrication process.

Table 3. Comparison of resistances of the polysilicon resistors.

Sample No.	**Resistances of the polysilicon resistor**		**Average Resistance (kΩ)**	**Calculated Resistance (kΩ)**
	R_1 (kΩ)	**R_2 (kΩ)**		
1.	2.15	2.18	2.14	1.65
2.	2.14	2.12		
3.	2.12	2.18		

Table 4. Comparison of the resistances of the coils.

Parameter	**Value**
Sample No.1 (Resistance)	6.01 kΩ
Sample No. 2 (Resistance)	6.88 kΩ
Sample No.3 (Resistance)	6.09 kΩ
Average Resistance	6.32 kΩ
Calculated Resistance	7.35 kΩ
Percentage Error	16 %

6. Conclusion

In conclusion, we reported post-CMOS processing and DC characterization of a cantilever sensor. The sensor was fabricated using 0.35 µm CMOS process at MIMOS Bhd. The SEM images of the released cantilever structure show that addition of the underneath SCS substrate with the thin film, by back side DRIE process, has successfully controlled curling of the structure. Although a small curling was observed in the capacitive comb fingers, there still exists overlapping area between the static and moveable fingers. Therefore, a successful capacitive sensing is expected. During DC characterization, all the electrical connections were found intact. The measured values of the resistances of the polysilicon resistors and pickup coil agree with the designed values within an acceptable error range.

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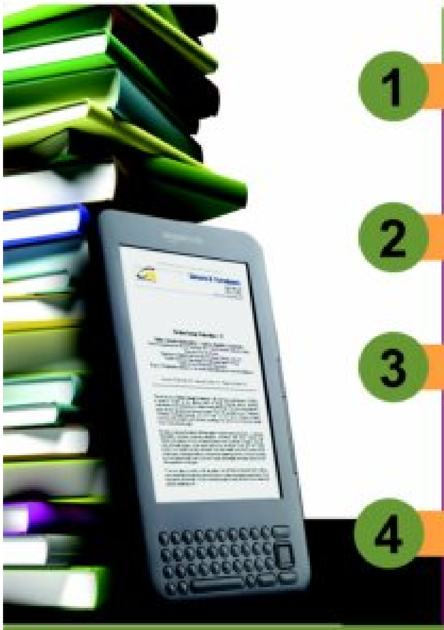

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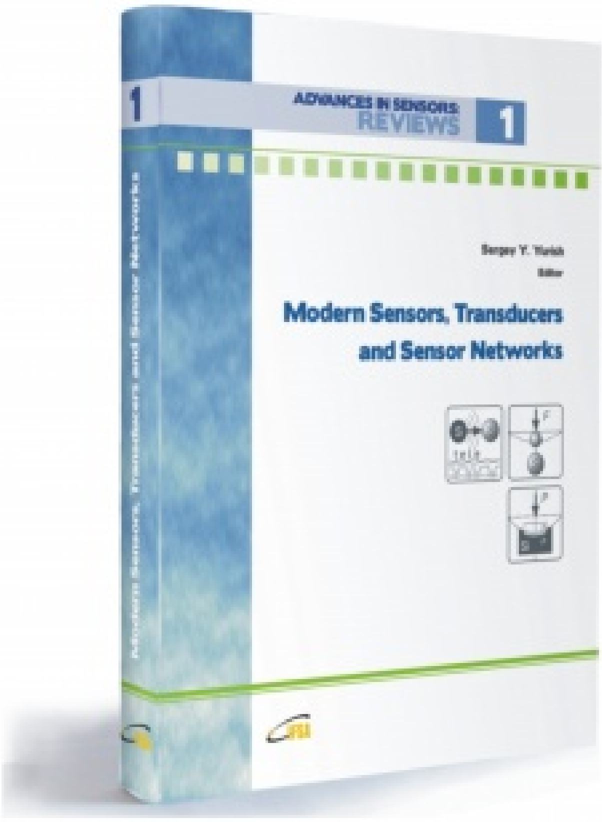

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