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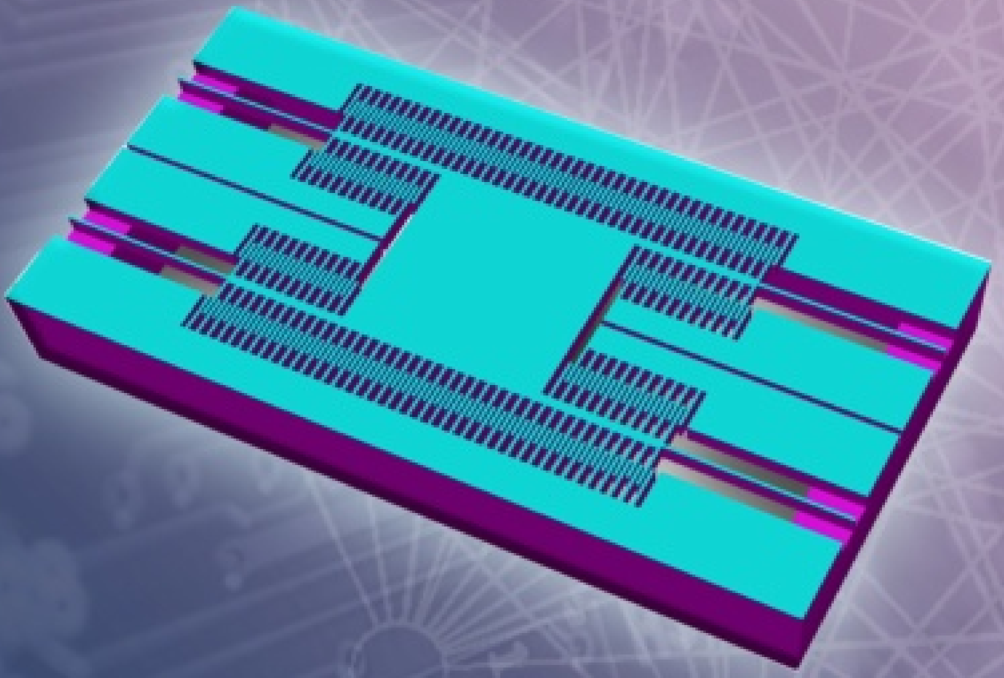

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A Low Ripple Charge Pump Using Low-Voltage CMOS Process

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Abstract: In power supply systems, switching supplies are typically cascaded with low dropout (LDO) regulator to suppress noise and provide low noise output. By providing lower output ripple voltage from charge pump circuit, input noise level (ripple) can be reduced first before it is fed into LDO and hence a more stable supply voltage can be generated from LDO. In this paper, a low voltage CMOS charge pump which offers lower output ripple voltage is proposed. Charge transfer switch (CTS) control scheme is employed inside cross-coupled charge pump in order to suppress backward current leakage path during clock transition. Therefore, proposed charge pump circuit provides lower output ripple voltage and higher voltage pumping efficiency. The proposed circuit has been simulated in 45 nm CMOS process to validate the functionality of the circuit. The measured ripple voltage is less than 60 mV at 10 mA load current with 60 MHz pumping frequency. *Copyright © 2012 IFSA.*

Keywords: Charge pump, Ripple voltage, Low voltage.

1. Introduction

Charge pump circuit is a type of dc-dc converter that can generates dc voltages that are higher than the power supply voltage. Charge pump circuits have been used extensively in the nonvolatile memories, such as EEPROMs and flash memories, which involve in the programming and erase the floating-gate devices [1, 2]. Besides, charge pump circuits are also used in power supplies for liquid-crystal-display (LCD) drivers [3], USB OTG (On-The-Go) applications which require high current drivability [4], and white LED driver IC [5].

As a switching power supply, charge pump circuit introduces systematic noise which causes fatal to state-of-art data converters, radio frequency radios, phase-locked loops, and etc. Hence, low dropout

(LDO) regulator is normally cascaded to the switched supply to suppress noise before it is connected to subsequent sensitive analog circuit blocks [6, 7]. Therefore, allowable noise or output ripple voltage for a power supply is an important element in power supply design. To efficiently suppress the noise at the output of LDO, one cannot solely depend on the LDO but also need to provide a less noise input voltage before it is fed into LDO.

Section 2 reviews the conventional charge pump circuit topologies. Section 3 discusses the new proposed charge pump circuit, including operations and schematics. Section 4 shows the simulations results and comparisons. Finally, conclusions are shown in section 5.

2. Conventional Charge Pump Circuit Topology

2.1. Dickson Charge Pump

Most of the charge pump circuits are designed based on the Dickson charge pump [8]. A conventional four-stage Dickson charge pump circuit is shown in Fig. 1. Basically, this circuit consists of diodes, capacitors and non-overlapping clock generator. Non-overlapping clock generator is used to generate two non-overlapping and out-of-phase clock sources, CLK and CLKB. The voltage of the clock sources is usually same as supply voltage VDD.

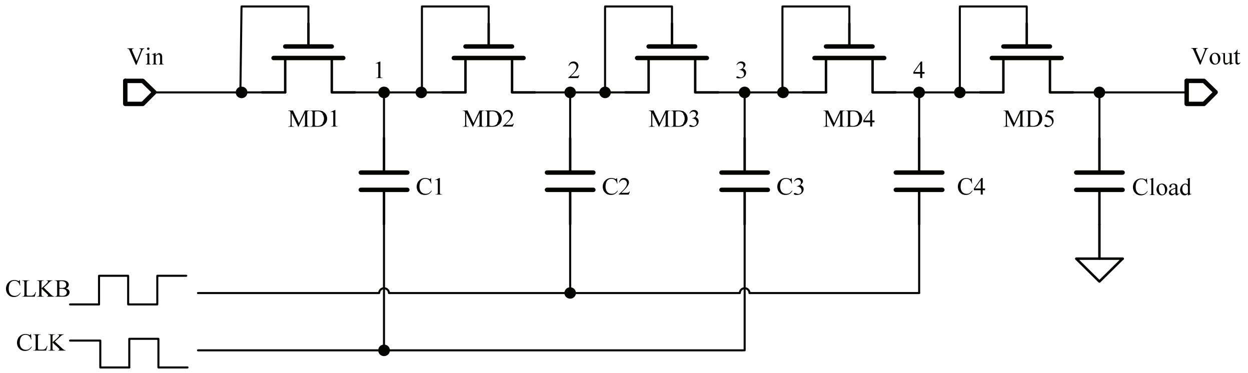


Fig. 1. A conventional Dickson charge pump circuit.

This popular charge pump circuit uses diode-connected MOS as energy-passing elements and capacitors as energy-storing elements. Charges are passed in one direction and stored in the next stage capacitor. Hence, voltage can be pumped high and is proportional to number of stages that are used. The output voltage of Dickson charge pump is therefore given by:

$$V_{out} = VDD + N \times (VDD - V_t) - V_t, \quad (1)$$

where N is the number of stages of the charge pump circuit.

After stray capacitance, C_s and load current, I_{load} take into consideration, the voltage fluctuation at each pumping node can be expressed as:

$$\Delta V = V_{clk} \times \frac{C}{C + C_s} - \frac{I_{load}}{f \times (C + C_s)}, \quad (2)$$

where V_{clk} is the amplitude of the clock, C is the pumping capacitor, Cs is the stray capacitance, f is the clock frequency and I_{load} is the load current. Due to body effect of the MOSFET, threshold voltage increases across the stages. This causes voltage pumping gain is reduced and ends up to be zero when V_t equals to VDD. Hence, Dickson charge pump is not a suitable solution for low voltage operation.

2.2. Dynamic CTS Charge Pump

Dynamic Charge-Transfer-Switch (CTS) charge pump is a variant of Dickson charge pump and it was proposed by Wu and Chang [9]. A four-stage charge pump circuit is shown in Fig. 2. Additional auxiliary CTS switches chain (MS1-MS4) which is controlled by inverter pairs (MN1- MP1 to MN4-MP4) have been added in each stage of the charge pump circuit to eliminate threshold voltage drop at each pumping node. By using this dynamic control circuit, Dynamic CTS charge pump able to transfer charges from current stage to the next stage with improved of voltage gain. However, the output stage of the Dynamic CTS charge pump is still a diode-connected MOSFET and hence it still suffers body effect problem which causes large voltage drop at the output of the circuit. Besides, there is also electrical overstress (EOS) problem occurs in the circuit. One can found out that part of the MOSFET in the circuit having a maximum voltage difference of 2 × VDD which causes these MOSFET suffer the high voltage overstress over the gate oxides.

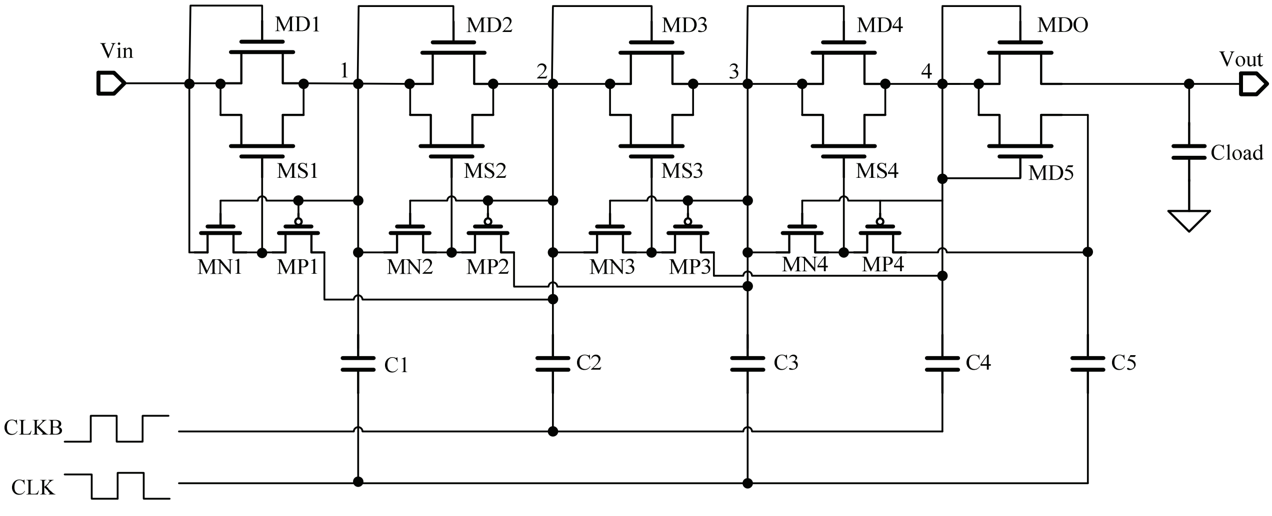


Fig. 2. A four-stage Dynamic CTS charge pump circuit.

2.3. Cross-coupled Charge Pump

To resolve threshold voltage drop and the voltage stress on the gate oxide, cross-coupled charge pump has been proposed [10]. This charge pump circuit successfully gets rid of threshold voltage drop without suffering any voltage stress on the gate oxide.

A four-stage of cross-coupled charge pump is shown in Fig. 3. To eliminate the gate-oxide reliability issue, two branches of similar circuits are cross coupled to ensure the voltage drop between gate-source (V_{gs}) and gate-drain (V_{gd}) does not exceed VDD. Since there are no diode-connected MOSs in the charge feed-forward path, threshold voltage drop is eliminated as well.

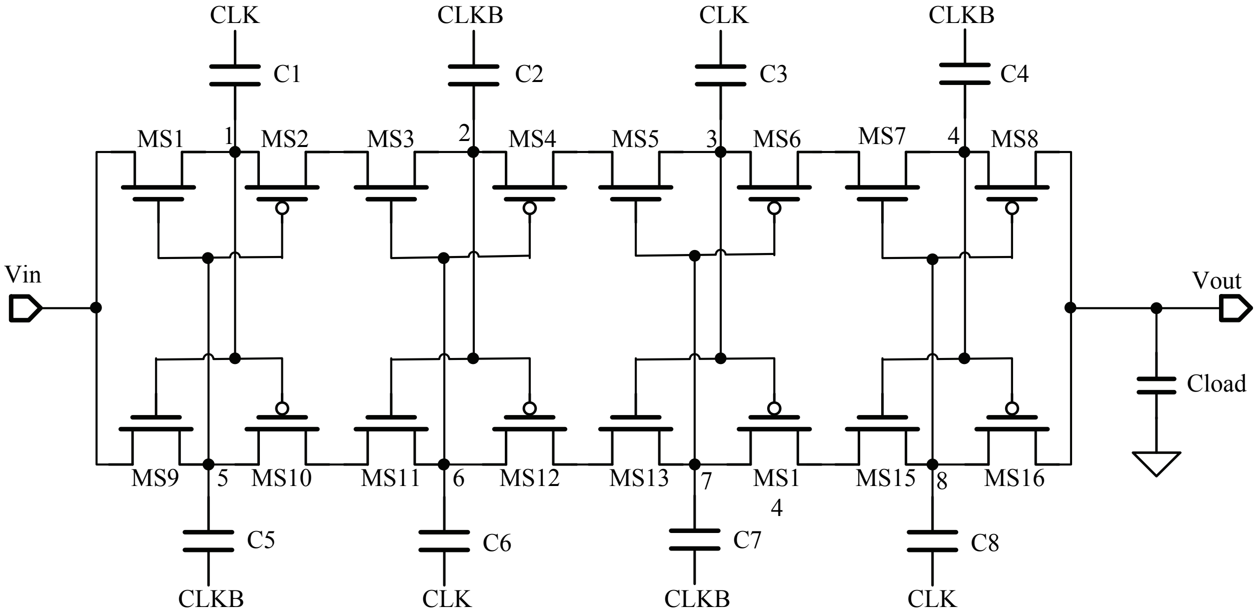


Fig. 3. A four-stage cross-coupled charge pump circuit.

In spite of this cross-coupled charge pump circuit has solved the oxide reliability issue and threshold voltage drop, there is still exist of short period of backward current path during the clock transition interval. Since the generated clock signals are non-overlapping, when CLK is from low to high and CLKB is from high to low, there is a short period where both clock signals are low which account for the backward current path in the circuit. Refer to Fig. 3, when CLK and CLKB are low, voltage at both node 4 and node 8 are 4 × VDD and output voltage is maintained at a level in between $4 \times \mathrm{VDD} < V_{out} < 5 \times \mathrm{VDD}$, which depends on size of transistors, load capacitance and output current loading. This turns on MP4 and MP8 and allows charges flow back from output to node 4 and 8. This causes some degradation to the output voltage level and gives larger ripple voltage at the output voltage.

3. Proposed Charge Pump Circuit Topology

Fig. 4 shows the new proposed charge pump circuit. The proposed charge pump circuit uses cross-coupled charge pump circuit topology [10] as its skeleton and implements CTS control scheme concept from the Dynamic CTS charge pump [9] in order to give a smaller output ripple voltage. Cross-coupled charge pump topology is utilized due to this charge pump topology was designed with the consideration of gate-oxide reliability issue, so that the gate-source voltage (Vgs) and gate-drain voltage (Vgd) of all MOSFETs in the circuit do not exceed VDD [10]. Whereas CTS control scheme is employed in the proposed circuit due to its ability that able to use the already established high voltages from the desired node to control the CTS switch that it is attached with.

As illustrated in Fig. 4, two-phase non overlapping clock signals, CLK and CLKB with amplitude VDD are used in the proposed circuit. This proposed circuit consists of two main charge transfer branches, branch A and branch B. Branch A and branch B are symmetrical to each other, but connected with out-of-phase clock signals, i.e. CLK and CLKB are connected to first and second pumping stage of branch A, respectively. Whereas CLKB and CLK are connected to first and second pumping stage of branch B, respectively. Output nodes of two branches are connected together to give the output voltage. Auxiliary capacitors Ca1, Ca2, Ca3, and Ca4 are added in the first stage to ensure MS2 and MS6 are turned off properly during clock transition period. Detailed circuit operations of each pumping stage in different clock cycles will be explained in the next section.

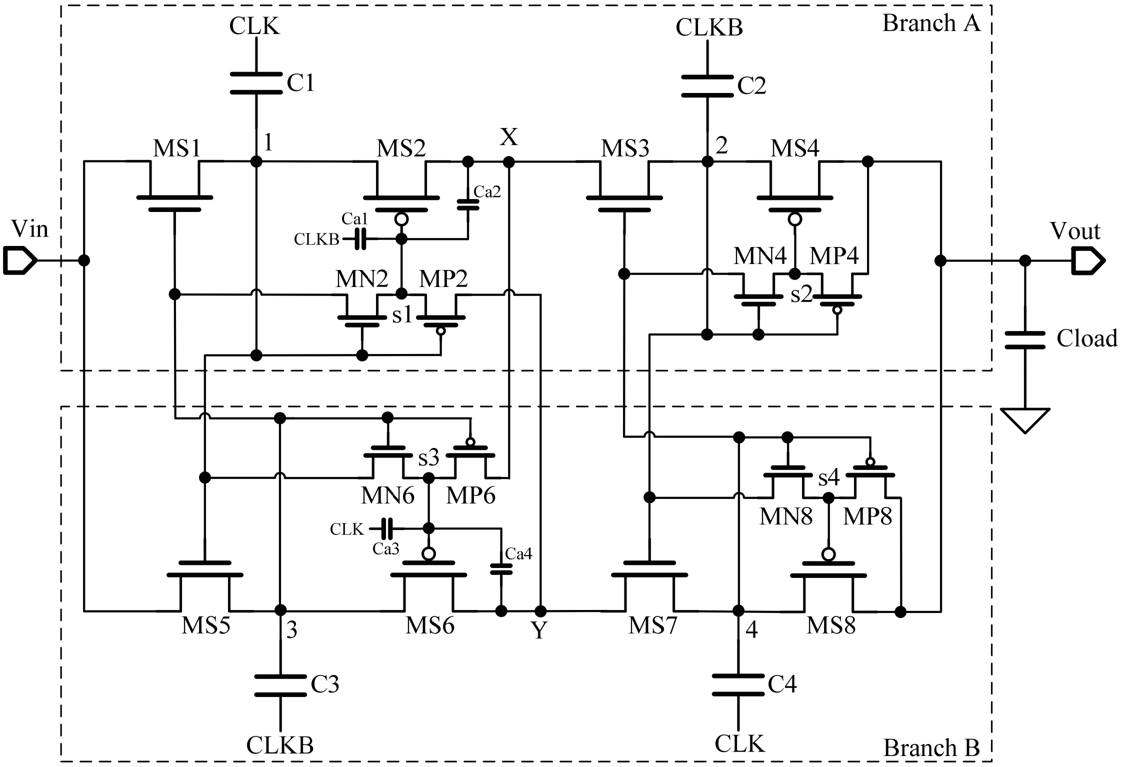


Fig. 4. Proposed small ripple charge pump circuit with two pumping stages.

3.1. Circuit Operation of the First Pumping Stage

Refer to Fig. 4, when the clock signal CLK is low and CLKB is high, voltage at node 3 will be coupled up to 2 × VDD, and hence voltage difference between node 3 and node 1 (V31) is VDD. This turns on transistor MS1 and charges are transferred from power supply Vin to node 1. The transistor MN2 is turned off and MP2 is turned on which makes the inverter MN2-MP2 output equals to 2 × VDD. This turns off transistor MS2 and shut off the current to flow from node 2 to node 1. Whereas in branch B, MS5 is turned off to prevent current to flow back from node 3 to power supply. The transistor MN6 is turned on and MP6 is turned off which makes the inverter MN6-MP6 output equals to VDD. Hence, MS6 is turned on and charges are transferred from node 3 to node 4.

Similarly, during clock signal CLK is high and CLKB is low, voltage at node 1 will be coupled up to 2 × VDD, and hence voltage difference between node 3 and node 1 (V31) is –VDD. Same circuit operations result MS1 is turned off to cutoff current to flow from node 1 to power supply. Transistor MS2 is turned on and let charges to be transferred from node 1 to node 2. Whereas in branch B, MS5 is turned on to let charges to be transferred from power supply to node 3. Transistor MS6 is turned off and shuts off the backward current to flow back from node 4 to node 3.

During clock transition period, i.e. when both CLK and CLKB are low, both node 1 and node 3 are at voltage level of VDD. Due to parasitic capacitive coupling effect, voltage level at node X and node Y are coupled down and hence MP2 and MP6 are turned off as $V_{sg} < |V_t|$. Same reason goes to node s1, where voltage level at node s1 is coupled down and MS2 is turned on as $V_{sg} > |V_t|$. This leads to the formation of backward current path during clock transition period. In order to turn off MS2 and MS6 during clock transition period, V_{sg} for both transistors have to be less than $|V_t|$. To do this, Ca1 and Ca3 are added at node s1 and s3 to maintain the initial voltage level at both nodes. Whereas Ca2 and Ca4 are added to further increase the coupling effect to couple down voltage level at both node X and node Y. With that, backward current of transistor MS2 and MS6 during clock transition period can be suppressed.

3.2. Circuit Operation of the Output Pumping Stage

As shown on Fig. 4, during clock signal CLK is low and CLKB is high, node 2 is coupled up to 3 × VDD and node 4 is equal to 2 × VDD. Voltage difference between node 2 and node 4 (V24) is VDD. Pass transistors MS2 and MS3 are turned off and shut off the backward current path from node 2 to node 1. In branch B, MS7 and MS6 are turned on and charges are transferred from node 3 to node 4. Besides, MN4 is turned on and MP4 is turned off which makes the output of inverter MN4-MP4 equals to 2 × VDD. This turns on transistor MS4 and charges are transferred from node 2 to output. On the other hand, transistor MN8 is turned off and MP8 is turned on which makes the output of inverter MN8-MP8 equals to Vout. This turns off MS8 and shut off the current from Vout to node 4.

In next time interval, i.e. during CLK is high and CLKB is high, where V24 is –VDD. Pass transistors MS2 and MS3 are turned on to transfer charges from node 1 to node 2. In branch B, transistors MS7 and MS6 are turned off and shut off the backward current path from node 4 to node 3. Besides, MN4 is turned off and MP4 is turned on which makes the output of inverter MN4-MP4 equals to Vout. This turns off transistor MS4 and shut off the current to flow from Vout to node 2. On the other hand, transistor MN8 is turned on and MP8 is turned off which makes the output of inverter MN8-MP8 equals to 2 × VDD. This turns on MS8 and charges are transferred from node 4 to output.

During clock transition period, both node 2 and node 4 are 2 × VDD, MP4 is turned on and MN4 is turned off which makes the output shorted to node s2. Same circuit operations apply to transistor MS8 where MN8 is turned off and MP8 is turned on which makes the output shorted to node s4. This turns off MS4 and MS8 where backward current from Vout to node 2 and node 4 can be suppressed.

4. Circuits Simulations and Comparisons

A 45 nm CMOS process model is used to simulate and verify the circuit performance of the proposed charge pump circuit and the prior works [9, 10]. All charge pump circuits are simulated with two-stage basis and can support up to 10 mA of load current. To have a fair comparison, all charge pumps are designed under same conditions, i.e. each circuit consists of 500 pF of load capacitor and same size of pass transistors. Whereas for pumping capacitors, both proposed charge pump circuit and cross-coupled charge pump are set to 400 pF; Dynamic CTS charge pump is set to 533 pF (400 pF × 4/3). For auxiliary capacitors in the proposed charge pump circuit, Ca1 and Ca3 are designed with 200 pF; Ca2 and Ca4 are designed with 50 fF. For all simulations, the non-overlapping clock frequency is set to 60 MHz.

Fig. 5 shows the simulation results of the voltage waveforms at each pumping nodes and at output of the new proposed two-stage charge pump circuit with clock period of 16.667 ns and VDD = 1 V. Ideally, output voltage can be pumped up to 3 V (3 × VDD), but due to the parasitic capacitance at each pumping node, the simulated output voltage is found to be 2.94 V.

Fig. 6 compares the simulated drain current of PMOS MS4 of cross-coupled and proposed charge pump circuit under VDD = 1.0 V and current loading of 10 mA. For PMOS, backward leakage current is positive. Fig. 7 shows that during clock transition period, i.e. when both clocks are low, cross-coupled charge pump circuit has leakage current up to 40 mA whereas the proposed charge pump circuit has nearly zero leakage current.

Fig. 7 compares the output ripple voltages of cross-coupled and new proposed charge pump circuit under different supply voltages when output current loading is 10 mA. From Fig. 6, the new proposed charge pump circuit is verified to have smaller output ripple voltages than the cross-couples charge pump circuit. The proposed charge pump circuit generates as low as 42.8 mV of output ripple voltage while cross-coupled charge pump circuit have 66.8 mV. Regardless of the supply voltages, the new proposed charge pump circuit offers smaller output ripple voltage than cross-coupled charge pump circuit. With smaller output ripple voltage, a more stable supply voltage can be generated from LDO regulator when output voltage of charge pump is fed into LDO regulator.

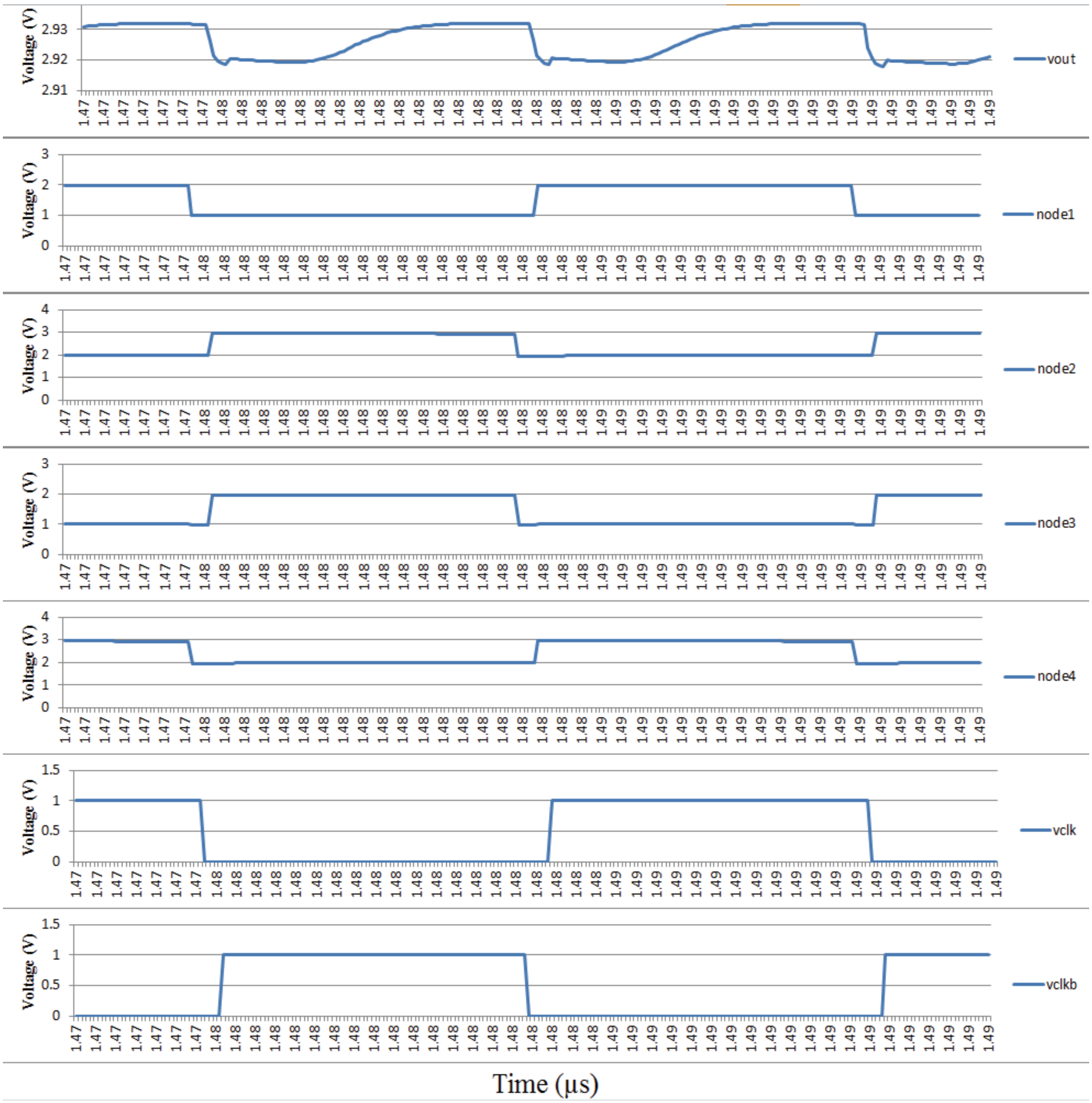
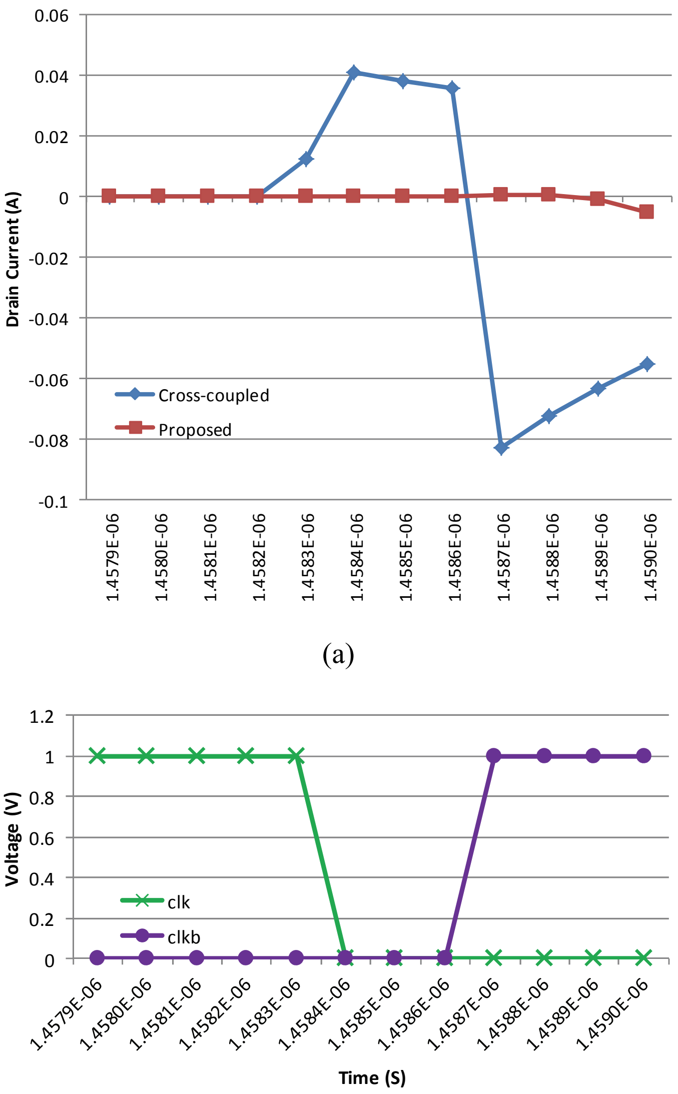


Fig. 5. Simulated voltage waveforms of Vout, node 1-4, CLK and CLKB, in the proposed two-stage charge pump circuit.

Fig. 8 compares the simulated output voltages of Dynamic CTS, cross-coupled and new proposed charge pump circuit under different output current loading. As illustrated in Fig. 7, output voltages of these charge pump circuits are decreases with the increase of load currents.

However, the new proposed charge pump circuit offers better performance over cross-coupled and Dynamic CTS charge pump circuit.

Fig. 9 compares the simulated output voltages of Dynamic CTS, cross-coupled and new proposed charge circuit as a function of the number of the cascaded pumping stages with output current loading of 10 mA. The maximum achievable output voltage of each charge pump circuit is simulated up to 6 stages. The proposed charge pump circuit exhibits better pumping efficiency over cross-coupled and Dynamic CTS charge pump regardless numbers of pumping stages are cascaded together.



(a)

(b)

Fig. 6. (a) Simulation result of PMOS MS4 drain current at output stage of cross-coupled and proposed charge pump circuit during (b) clock transition period (Simulations are done under two-stage charge pump basis with VDD = 1.0 V and load current of 10 mA).

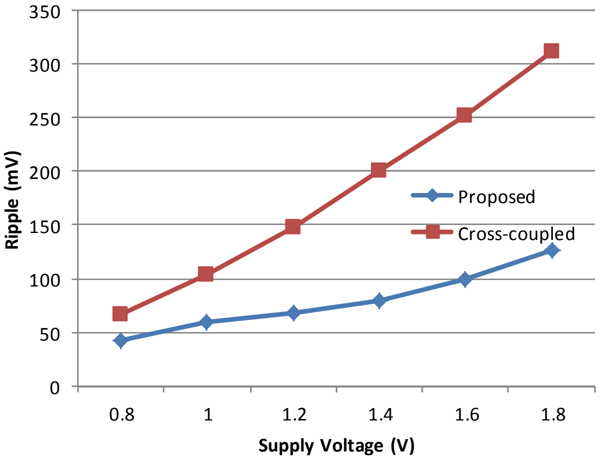


Fig. 7. Simulated output ripple voltages of cross-coupled and proposed charge pump circuit under different supply voltages (VDD) with load current of 10 mA.

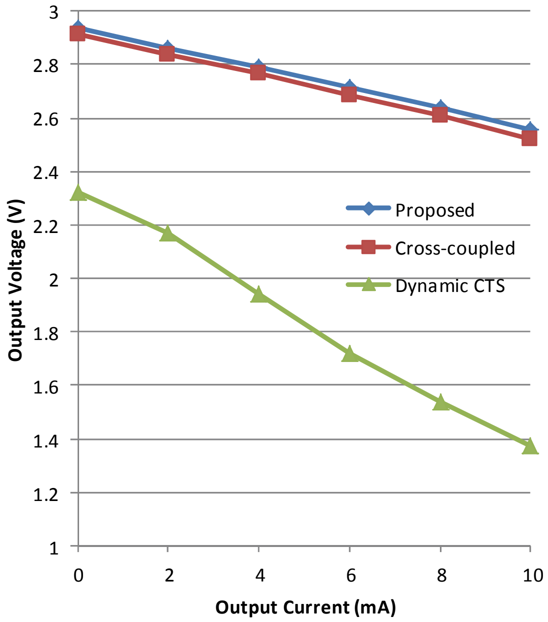


Fig. 8. Simulated output voltages of various charge pump circuit with two stages under different output currents with VDD = 1.0 V.

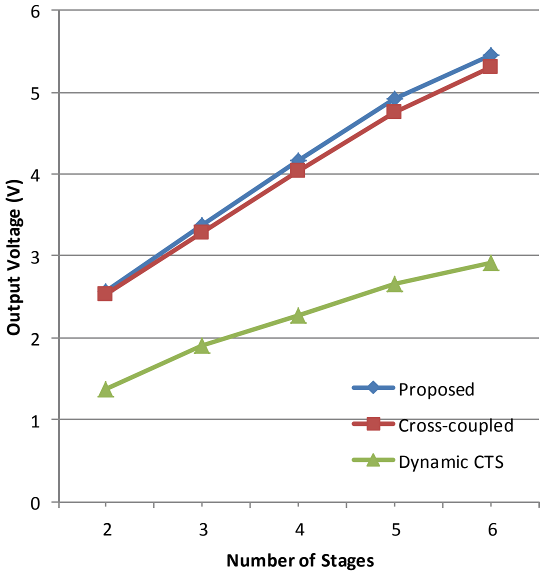


Fig. 9. Simulated output voltages of various charge pump circuits versus number of pumping stages when VDD = 1.0 V and load current = 10 mA.

Fig. 10 compares the simulated output voltages of cross-coupled and new proposed charge pump under different rise and fall time. As the rise / fall time gets bigger, the longer the non-overlapping clock transition time, the output voltage level for both charge pump circuits gets lower. However, cross-coupled charge pump circuit shows a more severe current leakage condition as the circuit cannot well impedes the leakage current flow back into the circuit.

Table 1 summarizes the simulation results of the cross-coupled and proposed charge pump circuits. Results are compiled under conditions of VDD = 1.0 V and loading current of 10 mA with CMOS 45 nm process technology.

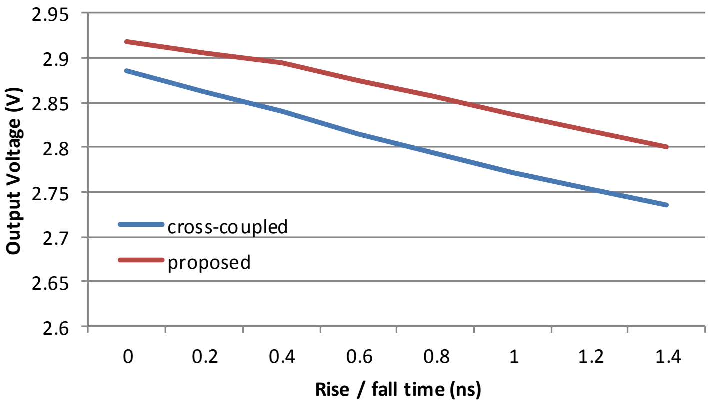


Fig. 10. Simulated output voltages of various charge pump on different clock rise / fall time.

Table 1. Simulation results summary.

	Cross-coupled [10]	**Proposed**
Input voltage	1.0 V	
Size of pumping capacitor	400 pF	
Output load capacitor	500 pF	
Clock frequency	60 MHz	
Average output voltage (When load current = 10 mA)	2.522 V	2.559 V
Output ripple voltage (When load current = 10 mA)	103.3 mV	59.6 mV
Pumping gain (When load current = 10 mA)	84.07 %	85.30 %

5. Conclusions

A new proposed charge pump circuit using 45 nm CMOS process for low voltage operation is proposed. Using the concept from Dynamic CTS and cross-coupled charge pump circuit, the proposed charge pump circuit able to suppress the backward leakage current and does not suffer gate-oxide reliability issue. Therefore, the new proposed charge pump offers smaller output ripple voltage and better pumping efficiency than conventional design. By offering smaller input noise level (ripple) before it is fed into LDO, a more stable supply voltage can be generated from LDO regulator.

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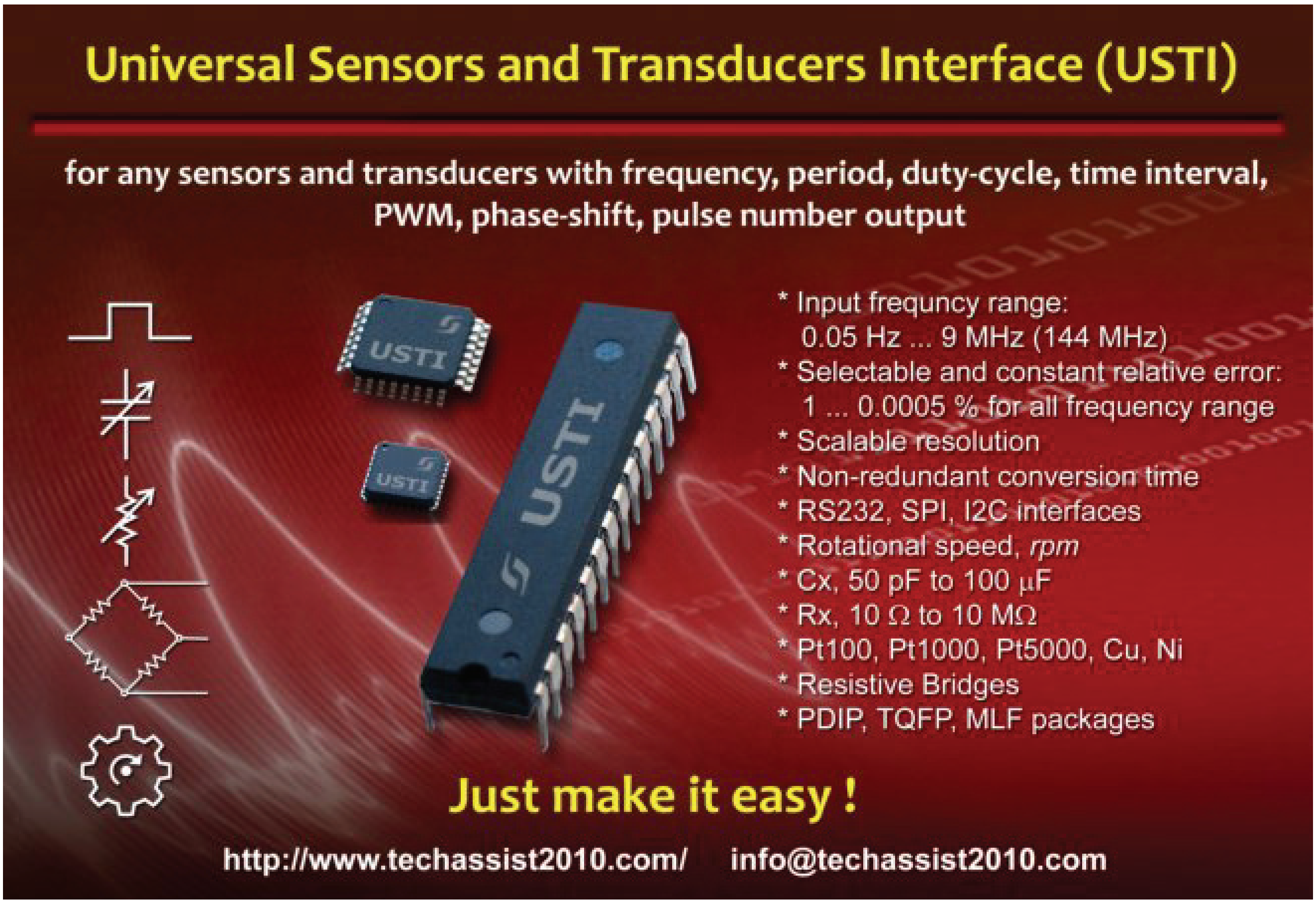

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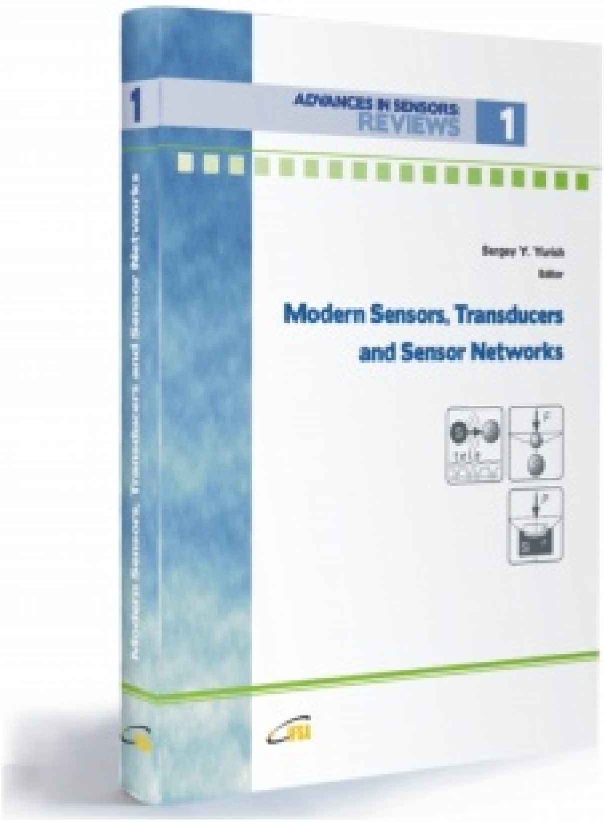

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