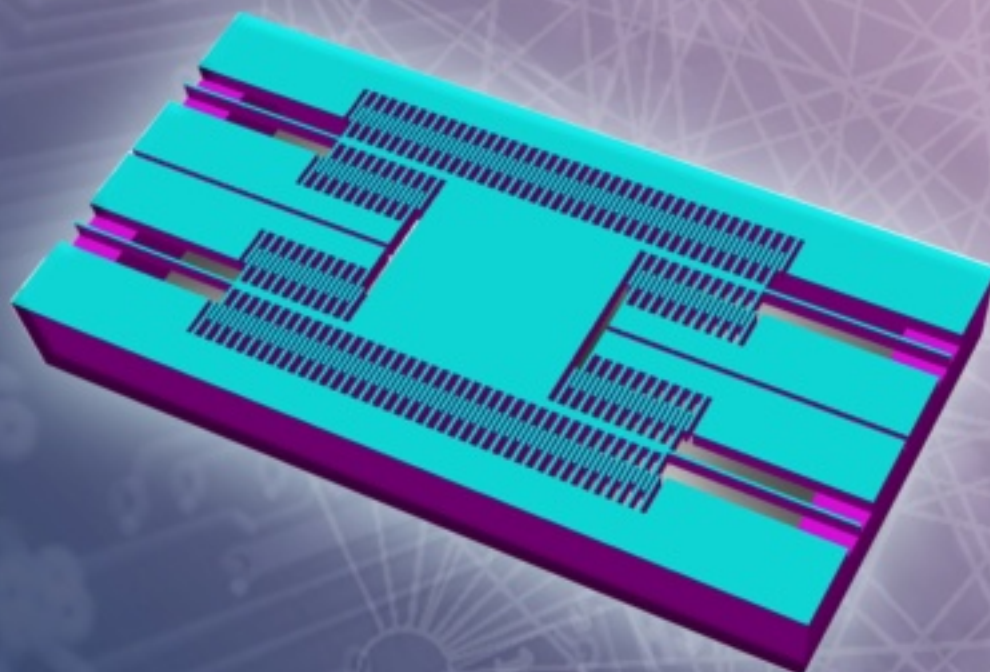


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Contents

Volume 17
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Research Articles

Foreword

Dr. Mohd Haris, Md Khir 1

Modeling and Layout Design of Resonant Lateral Comb Magnetic Sensor

F. Ahmad, J. O. Dennis, M. H. Md Khir and N. H. Hamid 1

DC Characterization and Post-CMOS Processing of a Microcantilever Sensor

A. Mirza, N. H. Hamid, M. H. Md. Khir, J. O. Dennis, K. Ashraf 13

Enhanced Performances of a Wireless System-on-Chip for MEMS Biomedical Plantar Pressure Sensor

Abdul Hadi Abdul Razak and Yufridin Wahab 22

Simulation of Liquid Material for Microfluidic-based Acoustic Sensor

M. F. A. Rahman, M. R. Arshad and A. A. Manaf 30

Design, Simulation and Fabrication of a Mass Sensitive CMOS-MEMS Resonator

A. Y. Ahmed, J. O. Dennis, M. H. Md Khir, M. N. Mohamad Saad and M. R. Buyong 40

Artificial Neural Network-based Electronic Nose for the Detection of Sulfate-reducing Bacteria

Earn Tzeh Tan, Zaini Abdul Halim, Darah Ibrahim, Rashidah Abdul Rahim, Junita Mohamad Saleh, Umadevi Chandaran 50

Microcontroller Based Neural Network for Landmine Detection Using Magnetic Gradient Data

Mohamed Elkattan, Ahmed Salem, Fouad Solima, Aladin Kamel and Hadia El-Hennawy 60

An Intelligent ANN Based Control of A Quasi Six-Phase Voltage Source Inverter

Mohammad Shahid Jamil, Mohammad Ibrahim Al-Naemi, Mohd. Arif Khan, Atif Iqbal, Shaikh Moinuddin 70

Comparative Study and Analysis of Suspension Systems using Adaptive Fuzzy Control

LAIQ Khan and M. Umair Khan 81

Development of NOx Emission Model Using Particle Swarm Optimized Least-Squared SVR (PSO-LSSVR) Hybrid Algorithm

Elangeshwaran Pathmanathan, Rosdiazli Ibrahim, Vijanth Asirvadam 98

Development and Implementation of Hybrid Controllers for Flow Control Application

M. Iqbal Ab Ghafar, R. Ibrahim, Zulfadhli Mazlan 110

Capability of Optical Approach in Condition Based Monitoring of Lubricant Oil

M. F. M. Idros, Hadzli Hashim, Md. Shabiul Islam, Sawal Hamid Ali 125

Extracting Broadband Tissue Optics Parameters from One Source-Detector CW Diffuse Optical Spectroscopy <i>Aulia Nasution</i>	135
A Low Ripple Charge Pump Using Low-Voltage CMOS Process <i>Lee Fu New, Zulfiqar Ali bin Abdul Aziz and Mun Fook Leong</i>	147
Experimental Study on a Directional Cylindrical Dielectric Resonator Antenna (CDRA) At 5 to 6 GHz <i>M. A. Zakariya, Z. Baharudin, M. H. Md Khir, A. J. Jamali, M. F. Ain, Z. A. Ahmad</i>	158
RF Energy Harvester: Harvesting Power from WiFi Signals for Low Power RFID Application <i>S. S. B. Hong, R. Ibrahim, M. H. Md Khir, M. A Zakariya, H. Daud</i>	168
Analytical Investigation of Frequency Dependence of Average Power of a Vibration Energy Harvester <i>K. Ashraf, M. H. Md. Khir, J. O. Dennis</i>	176
Trapezoidal Electrodes Array for Electret-Based Electrostatic Energy Harvester <i>Mohamad Radzi Ahmad and Mohd Haris Md Khir</i>	186
Power Management for USB2.0 5 V Supply Using Load Resistive and Switch Capacitive Detection Approach <i>Tan Thiam Loong, Dr. Anwar Hasni bin Abu Hassan</i>	199
DSP Sensorless Controller of Switched Reluctance Motor-Generator Approaching to AM Modulation <i>A. Moraveji, A. Siadatan, E. Afjei, M. Rafiee and E. Zarei Ali Abadi</i>	208
Optimal Feedforward Zero Phase Error Tracking Control for High Precision X-Y Table <i>Hashimah Ismail, Norlela Ishak, Mazidah Tajjudin, Mohd Hezri Fazalul Rahiman, Ramli Adnan</i>	217
Implementation and Optimization of Human Tracking System Using ARM Embedded Platform <i>Shen Khang Teoh, Vooi Voon Yap, Chit Siang Soh, Patrick Sebastian</i>	226
Effectiveness of the Polymer Electrolyte Membrane Fuel Cell in High Humidity Climate <i>Z. Jalauddin, N. M. Nor, T. Ibrahim, and Y. T. Sin</i>	234
Permittivity and Conductivity Dispersions of Properly and Non-properly Slaughtered Goat Meat <i>Abdullah MOHIRI, Zainal Arif BURHANUDIN and Idris ISMAIL</i>	247
Utilizing Bi₂Te₃ TE Pellet as the Condenser of Thermal Power Plant <i>M. Rafiee, A. Siadatan, E. Zarei Ali Abadi and E. Afjei</i>	257

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Power Management for USB2.0 5 V Supply Using Load Resistive and Switch Capacitive Detection Approach

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Abstract: This paper deals with two proposed power management circuitries for USB 5 V supply are demonstrated by using the current sense amplifier and MOSFET switches architecture. There are some power losses in switched-mode power supply (SMPS) when supplying 5 V to the USB port in board level design. The total amount of losses in reference board for 5 V SMPS is measured which consumes 21 mW. Two proposed detection circuitries which are load resistive and switch capacitive are used to save the power losses in SMPS. The simulation results for the power consumption of load resistive approach consume 2 mW whereas for switch capacitive approach consumes 7.5 mW when the 5 V SMPS is switched off. The load resistive and switch capacitive approaches will save total amount of 19 mW and 13.5 mW respectively in reference board. The load resistive approach has been implemented using breadboard and printed circuit board (PCB) and the total power saving is 18.5 mW. *Copyright © 2012 IFSA.*

Keywords: SMPS, USB2.0.

1. Introduction

The integrated circuit (IC) design world is moving towards the nano-technology nowadays, so that most of the devices can be made in very small size and is more preferable by the consumers. When the technology is moving towards into the smaller feature size, as a result, the power consumption by the devices become one of the critical issues that need to take into account during the design process.

In the conventional USB module or port, it received the power supply from the battery or adapter through a voltage regulator or switched-mode power supply (SMPS) all the time. Proper methods of designing USB peripheral power distribution are crucial to ensure full compliance with the USB specification [3]. As a result, there are some powers wasted when there is no any electronic device is connected to the USB port or when the electronic device is in its idle state. Therefore, some power management circuitries need to be proposed in order to save the total power losses in the design process. For instance, in [1, 2, 5], some USB detection circuits, together with the microprocessor or USB On-The-Go (OTG) has been used in the design and for the purpose of switching off the power supply when there is no device is plugged into the USB port or when the device is in idle state. The ultimate goal in introducing the proposed circuitries is to reduce or minimize the power consumption.

2. Power Consumption of 5 V SMPS

This work is related to the power management issues stated above. By reducing or saving the power at the USB port through the SMPS is the main objective in this research. Most of the SMPS using the PWM controller for its simplicity and good performance [4]. The two main motivations in this project are to save the power when there is no USB attached, and also when the USB devices are in their idle state.

2.1. When no USB Device Attached

The block diagram of 5 V SMPS and controller chip is shown in Fig.1. In the normal mode of operation, the power consumption of the 5V SMPS when there is no USB device attached, P

$$P = [V_{cc}(\text{out5_on}) \times I_{cc}(\text{out5_on}) + V_{smps}(\text{out5_on}) \times I_{smps}(\text{out5_on})] - [V_{cc}(\text{out5_off}) \times I_{cc}(\text{out5_off}) + V_{smps}(\text{out5_off}) \times I_{smps}(\text{out5_off})], \quad (1)$$

where V_{cc} and I_{cc} are the supply voltage and current in controller chip respectively, V_{smps} and I_{smps} are the supply voltage and current of 5V SMPS respectively.

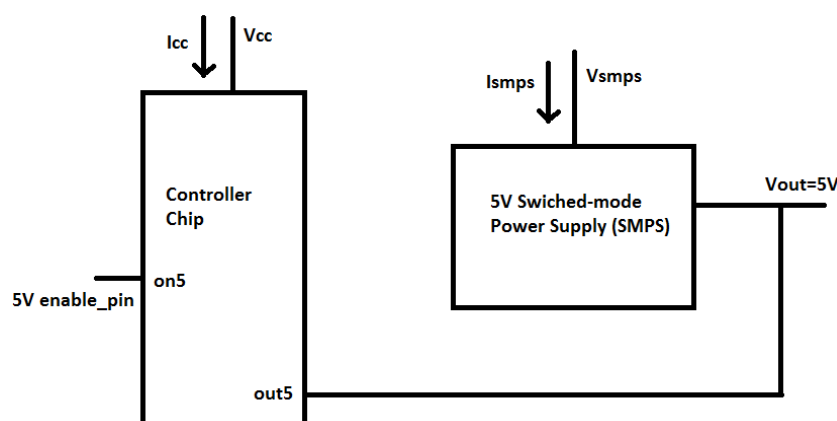


Fig. 1. Block Diagram of 5 V SMPS and Controller Chip.

Based on reference board, the data are obtained and tabulated in Table 1.

Table 1. Data collected based on Cedar Board Design.

Voltage/Current	Values
Vcc(out5_on)	5.106 V
Icc(out5_on)	2.480 mA
Vsmmps(out5_on)	19.50 V
Ismps(out5_on)	0.990 mA
Vcc(out5_off)	4.980 V
Icc(out5_off)	2.070 mA
Vsmmps(out5_off)	19.50 V
Ismps(out5_off)	0.020 mA

The total amount of power saving,

$$P = (5.106)(2.480 \text{ m}) + (19.50)(0.990 \text{ m}) - (4.980)(2.070 \text{ m}) + (19.50)(0.020 \text{ m}) = 21.27 \text{ mW}$$

2.2. When the USB Device is in Idle State

When entering in suspend or sleep mode,

Power Consumption at USB port when there is no USB device attached: $V_{5V} \times I_{\text{SUSPEND}} = 5 \times 0.715 \text{ mA} = 3.575 \text{ mW}$.

Power Consumption at USB port when the USB device in idle state (attached): $V_{5V} \times I_{\text{SUSPEND}} = 5 \times 500 \mu\text{A} = 2.5 \text{ mW}$.

3. Proposed Circuit Design

3.1. Load Resistive Approach

This proposed circuit is based on load resistor concept and is used to send a LOW signal to the controller chip in order to turn off the 5V SMPS when there is no USB device is attached to the USB port and also when the USB device is in its idle state. The Cedar board will be used as reference board throughout this work. The load resistive schematic is shown in Fig. 2.

3.1.1. For Normal Operation

This circuit starts with when there is no USB device is attached to the USB port, the Vbus is continuing supply the 5 V from the SMPS which is contribute to the power losses. The current sense amplifier will then load zero current from Vbus, and it will send a LOW output and compare with the comparator A. The output of comparator A will then compare with reference voltage source, V_A and send a LOW signal as well through the MOSFET switch A which is controlled by the Vbus. This LOW signal will send to the enable pin of controller chip in order to turn off the 5 V SMPS to minimize the losses. After turning off the 5 V SMPS, the Vbus is now at 0 V and MOSFET switch C is also turned off. The load resistor, R_L is playing an important role when there is a USB device is plugged into the USB port. There will be a voltage drop when the USB device is plugged in since the USB device is acting like a load connected to this circuitry. The comparator B is then compare with

the appropriate reference voltage source to send out a HIGH output through MOSFET switch B which controller by Vbus and inverter to the enable pin of controller chip. The Vbus is now turned on by the 5 V SMPS.

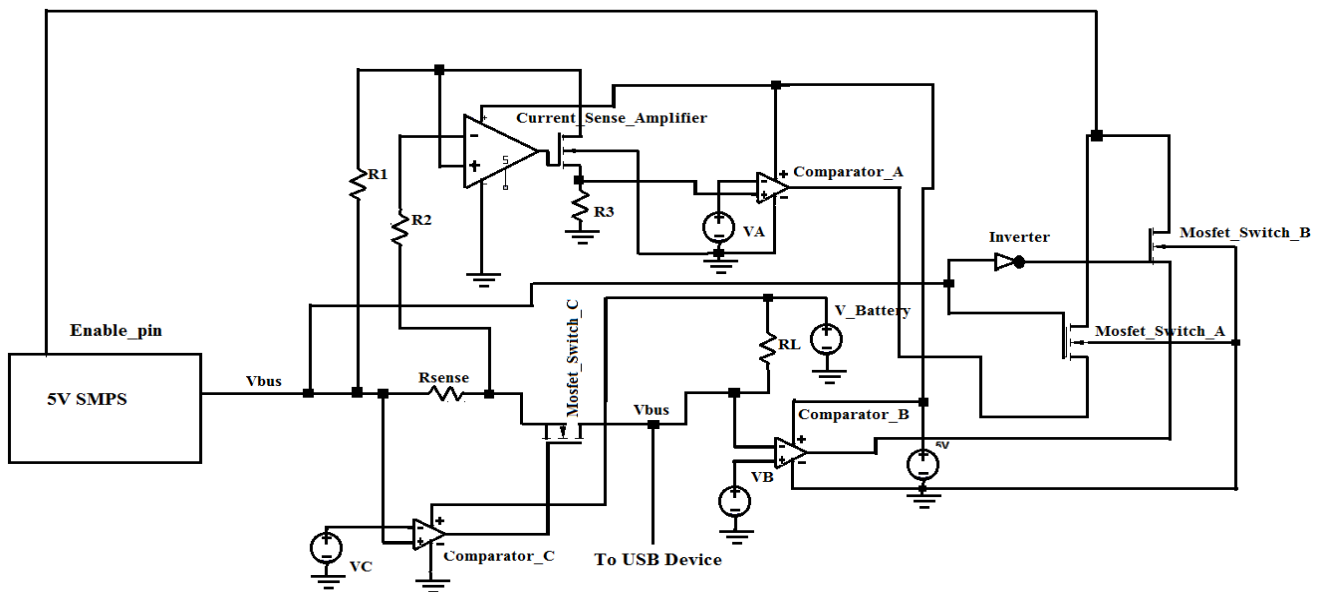


Fig. 2. Load Resistive Schematic Diagram.

3.1.2. For Suspend Mode Operation

When entering into suspend or sleep mode, if the D+/D- pin of USB do not receive any activity signal from the host for more than 3 ms, USB device will in suspend mode. The current draws from Vbus for low and high power device are 500 μ A and 2.5 mA respectively [6]. The Rsense value in current sense amplifier should be chosen as small as possible to avoid power losses. When in suspend mode, both the 5 V SMPS and the load resistive circuit will be turned off to save the power and incapability of the current sense amplifier for sensing the USB suspend low current which is 500 μ A and 2.5 mA respectively. The complete block diagram is shown in Fig. 3 for both normal and suspends mode operation. Note that the load resistive approach consists of current sense block and detection circuitry block. A time delay box from linear technology is used to send HIGH signal after some delay of time which can be adjusted by the resistor and capacitor value in delay box itself. The input of the delay box is connected to the D+/D- of USB device and it will send a shutdown signal through MOSFET switch E to the enable pin of the controller chip to turn off the 5V SMPS. At the same time, the shutdown signal from the load resistive circuit will be disconnected by the shutdown signal from time delay box through MOSFET switch C, and the load resistive circuit will be turned off through an inverter B and MOSFET switch B. Last but not least, the shutdown signal from time delay box will supply an extra 5 V voltage source directly to the USB devices so that the devices can continue to operate in suspend mode through the inverter A and MOSFET switch A, and disconnected the 5 V SMPS supply to the Vbus through MOSFET switch D simultaneously. When resume signal is generated by the host, the extra voltage source will be disconnected while the 5V SMPS and the load resistive circuit will be turned on by the time delay box.

3.2. Switch Capacitive Approach

The second proposed circuit is based on charging capacitor concept and using the charging and

discharging voltages to send a LOW signal to the controller chip in order to turn off the 5 V SMPS when there is no USB device is attached to the USB port and also when the USB device is in its idle state. The switch capacitive schematic is shown in Fig. 4.

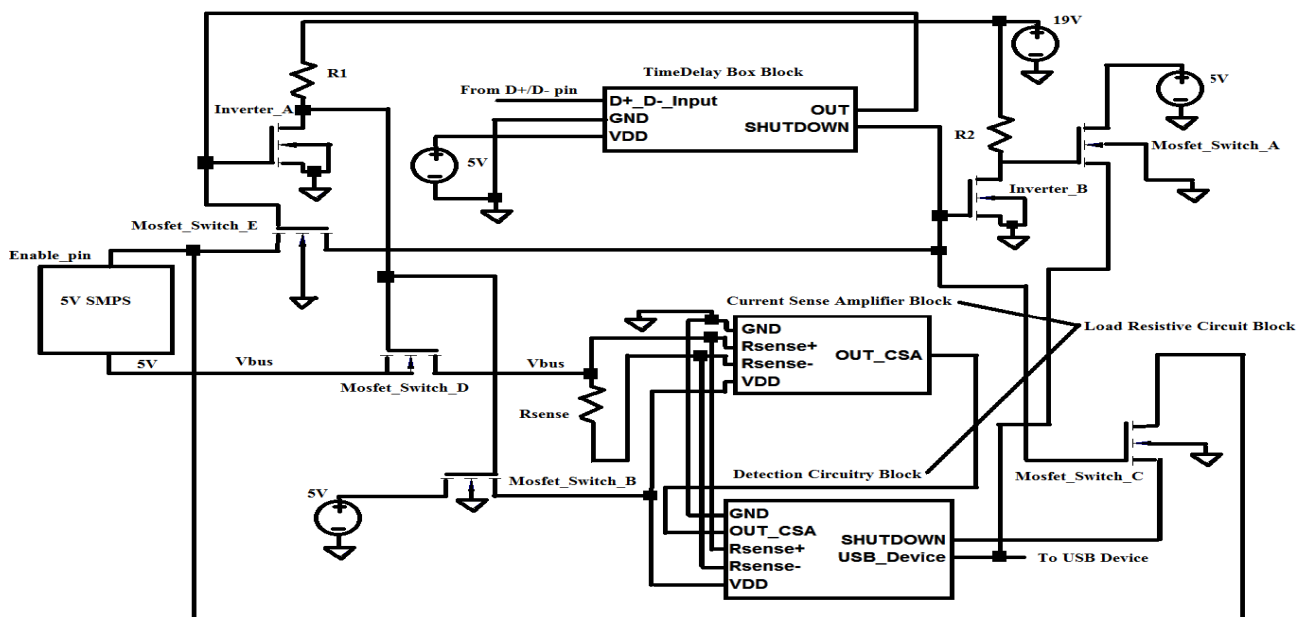


Fig. 3. Load Resistive Complete Block Diagram

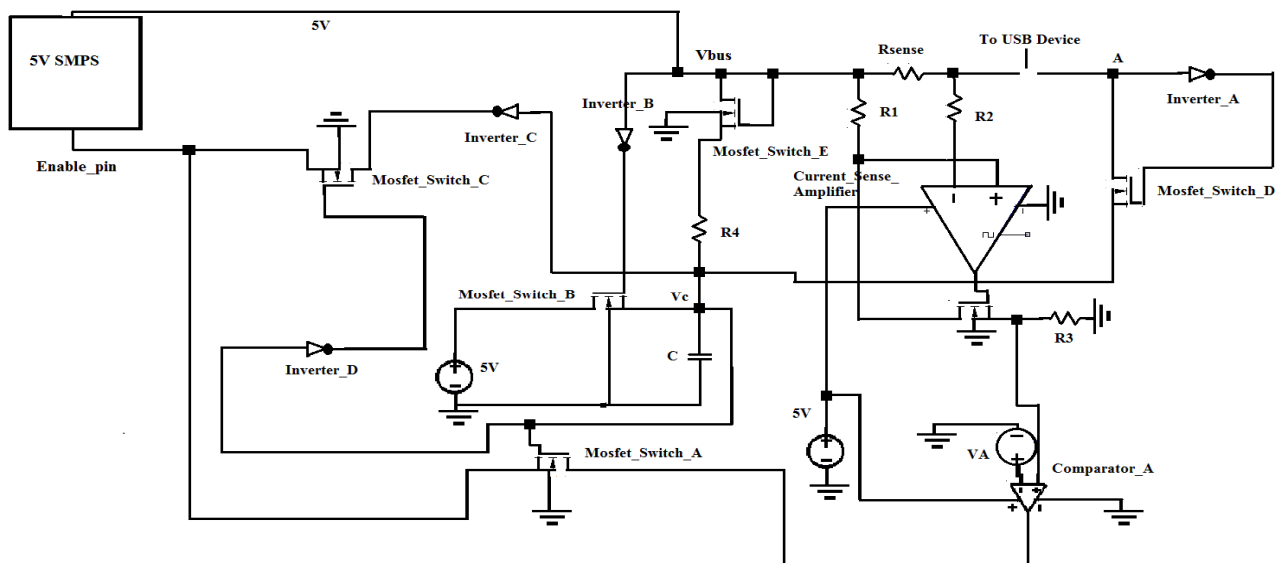


Fig. 4. Switch Capacitive Schematic Diagram.

3.2.1. For Normal Operation

This circuit starts with when there is no USB device is attached to the USB port and Vbus is continuing supply the 5 V from SMPS. The current sense amplifier will load a zero current and send a LOW signal and compare with the comparator A. the output of comparator A will compare with reference voltage, VA and send a LOW signal as well through MOSFET switch A which is controlled by the charging capacitor voltage. This LOW signal will then send to enable pin of controller chip in

order to turn off the 5 V SMPS. An extra 5 V voltage source is turned on through an inverter B and MOSFET switch B in order to continue charging the capacitor and turn the MOSFET switch A on until the USB device is plugged in. Note that the node A will be only connected to Vbus when USB device is plugged in. After turning off the 5V SMPS, the Vbus is at 0 V. When there is a USB device is plugged into the USB port and now the node A is connected to Vbus which is 0 V. The capacitor is now playing an important role and it will discharge to zero and turning off the MOSFET switch A while at the same time turning on the MOSFET switch C through the inverter D since the voltage across capacitor is 0 V. The MOSFET switch C will then pass the HIGH signal through inverter C from the 0 V across the capacitor to the enable pin of controller chip. The Vbus is now turned on by the 5 V SMPS.

3.2.2. For Suspend Mode Operation

The same concept stated in section 3.1.2 will be used in the suspend mode of switch capacitive. Refer to this section for more details. The complete block diagram is shown in Fig. 5. for both the normal and suspend mode operation. Note that the switch circuitry approach consists of current sense amplifier and detection circuitry block.

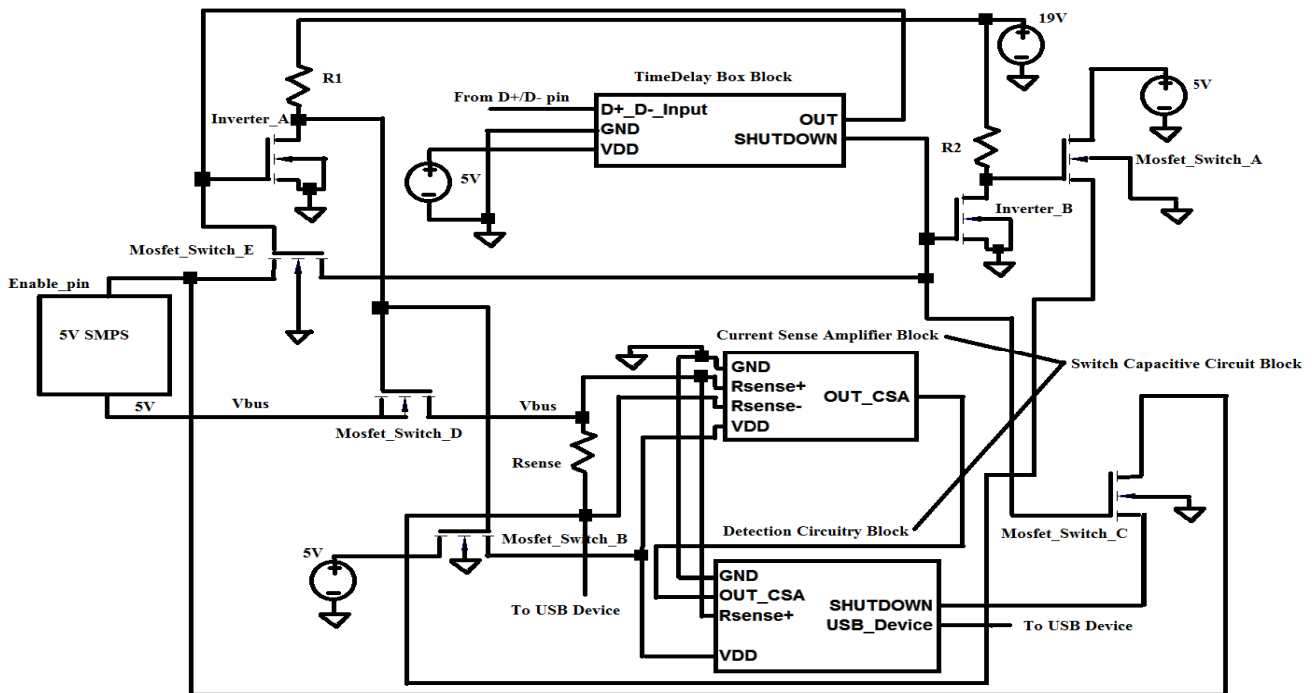


Fig. 5. Switch Capacitive Complete Block Diagram.

4. Simulation Results

4.1. Operation Results for Load Resistive & Switch Capacitive Approaches

The complete simulation results from the schematic in Fig. 3 and Fig. 5 by using the LTspice tool are shown in Fig. 6 and Fig. 7 respectively. The Vctrl signal represents the attachment of the USB device. For instance, logic HIGH for USB device attachment to the USB port whereas logic LOW for USB device detachment from the USB port. The D+/D- input of the time delay box is connected to Vpulse to represents the actual signal from D+/D- pin in USB devices. The time delay box is set to have the

delay of 330 ms for the simulation purpose. The USB current drew by the device in this simulation results is 100 mA.

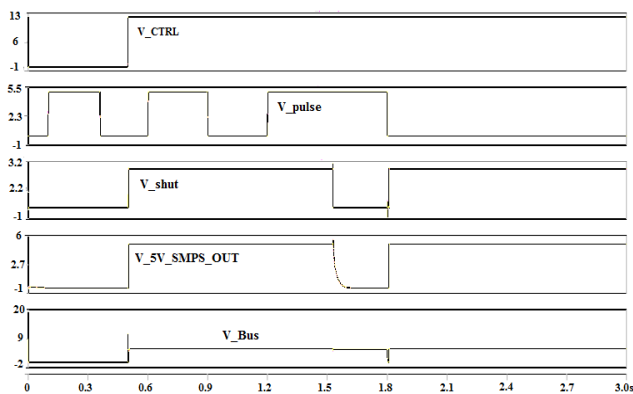


Fig. 6. Load Resistive Operation Results.

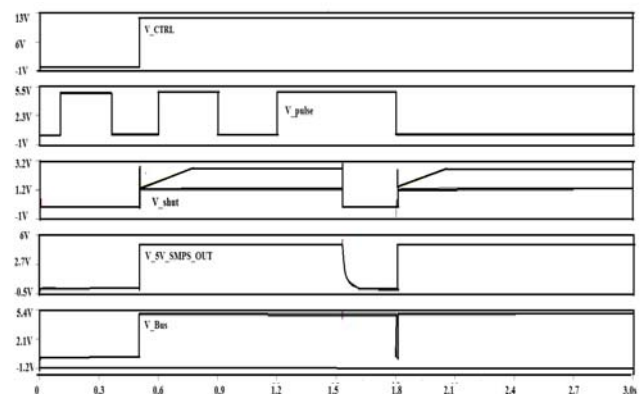


Fig. 7. Switch Capacitive Operation Results.

Firstly, there is no USB device connected to the USB port, i.e. Vctrl is logic LOW for 500 ms. The V_shut signal represents the shutdown signal and it send a logic LOW to the controller chip. Hence, the 5V_SMPS_OUT and VBUS are now turned off, which at 0 V. After that the USB device is connected to the USB port which the Vctrl is now logic HIGH until the end of simulation. The V_shut signal is now logic HIGH to the controller chip and then turning on the 5V_SMPS_OUT and VBUS, which at 5 V.

The idle state of the USB device which represented by Vpulse starts at 1.2 s and there is no any activity from the host more than 3 ms. The time delay box will send a shutdown signal to the controller chip after 330 ms which is at 1.533 ms. The V_shut signal will now at logic LOW and turning off the 5V_SMPS_OUT in order to save the losses in the SMPS itself but at the same time, an extra 5 V voltage source is supplied to the VBUS so that there is still have 5 V supply to the USB device in the suspend mode. Hence, VBUS will at 5 V in the idle state. The suspend state will be ended at 1.8 s which the resume signal is generated by the host to the USB device and the simulation results show the normal operation of the USB device after 1.8 s. The V shut signal is now pull up at logic HIGH to turn on the 5 V SMPS and the extra 5 V supply is now disconnected from the VBUS. The VBUS now obtains the 5V from the SMPS.

The hardware has been built for *Load Resistive* approach. The 5 V Vbus is connected to the 5 V supply instead of SMPS. We only observed for the V_shut when there is no USB device plugged in and when the device is in idle state. The V_shut is LOW when the V_ctrl is LOW and become HIGH when the V_ctrl is HIGH. When in idle state, the V_out, i.e. output from the time delay box will send a HIGH signal. Besides, the 5 V Vbus is observed when in idle state. For this case, the 5 V Vbus is connected to 0 V supply and hence the Vbus in idle can be observed clearly that is at 5 V which is the same result explained in section 4.1. The results shown in Fig. 8 (a) and Fig. 8 (b).

4.2. Power Consumption for Load Resistive & Switch Capacitive Approaches

The power consumption for the *Load Resistive* and *Switch Capacitive* circuitry using the LTspice tools are simulated. The power consumption consumed by each block when there is no USB device is plugged in and when in its idle state at 25 °C are obtained which will tabulate in Table 2. The power consumption of the hardware part for Load Resistive approach is measured using digital multimeter and is also tabulated in Table 2.

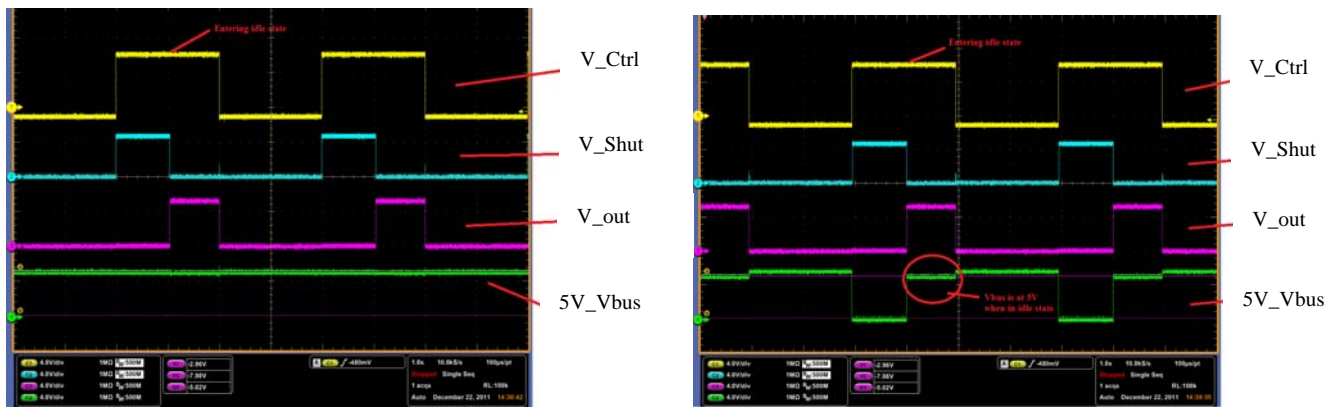


Fig. 8(a). Hardware for Load Resistive (Vbus at 5V). **Fig. 8(b).** Hardware for Load Resistive (Vbus at 0V).

Table 2. Power Consumption Comparison.

Block/ Components	Simulation data						Hardware data	
	SMPS without detection circuit (Watt)		SMPS with Load Resistive (Watt)		SMPS with Switch Capacitive (Watt)		SMPS with Load Resistive (Watt)	
	No USB	IDLE	No USB	IDLE	No USB	IDLE	No USB	IDLE
Current Sense Amplifier	N/A	N/A	1.2 m	217 u	1.2 m	221 u	2.2 m	1.65 m
Detection Circuitry	N/A	N/A	4.1 u	113 u	5.4 m	444 p		
Time Delay Box Block	N/A	N/A	483 u	733 u	483 u	734 u		
Rsense	N/A	N/A	0	0	0	0	0	0
R1	N/A	N/A	0	360 u	0	360 u	0	361 u
R2	N/A	N/A	360 u	0	360 u	0	361 u	0
Total power losses	21 m	3.6 m	2.1 m	1.4 m	7.5 m	1.3	2.5 m	2.0 m
Total power saving			19 m	2.2 m	13.5 m	2.3 m	18.5 m	1.6 m

5. Conclusions

The *Load Resistive* approach consumes 2.1 mW when there is no USB device is plugged in and 1.4 mW in idle state. This proposed method saves total amount of 19 mW in this reference board design. For the hardware part, this approach consumes 2.5 mW when no USB device is plugged in and 2 mW in idle state. Total power saving is 18.5 mW which is slightly lower than the simulation results. The *Switch Capacitive* approach consumes 7.5 mW which is higher than the *Load Resistive* approach when there is no USB device is plugged in and 1.3 mW in idle state. This proposed method saves total amount of 13.5 mW in this reference board design. The *Load Resistive* approach is more preferred because it consumes less power and more suitable in the low power design.

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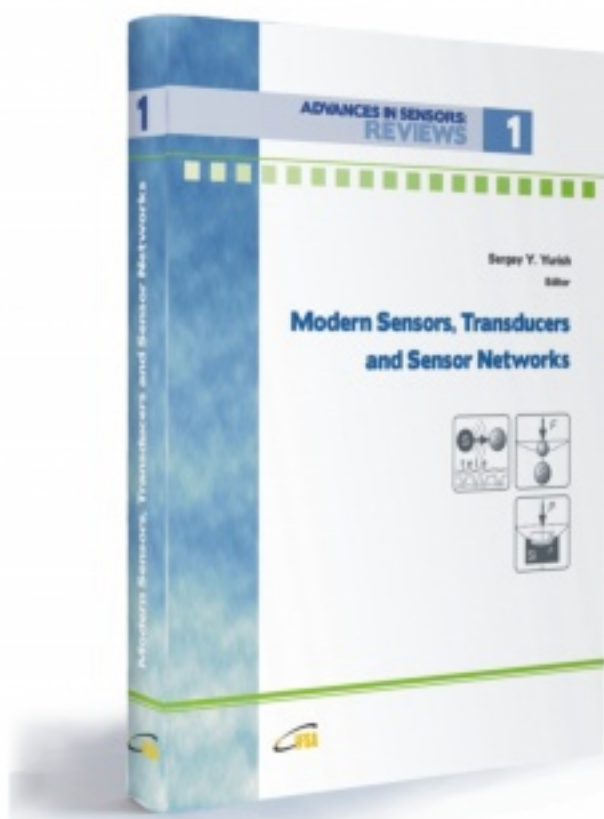
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