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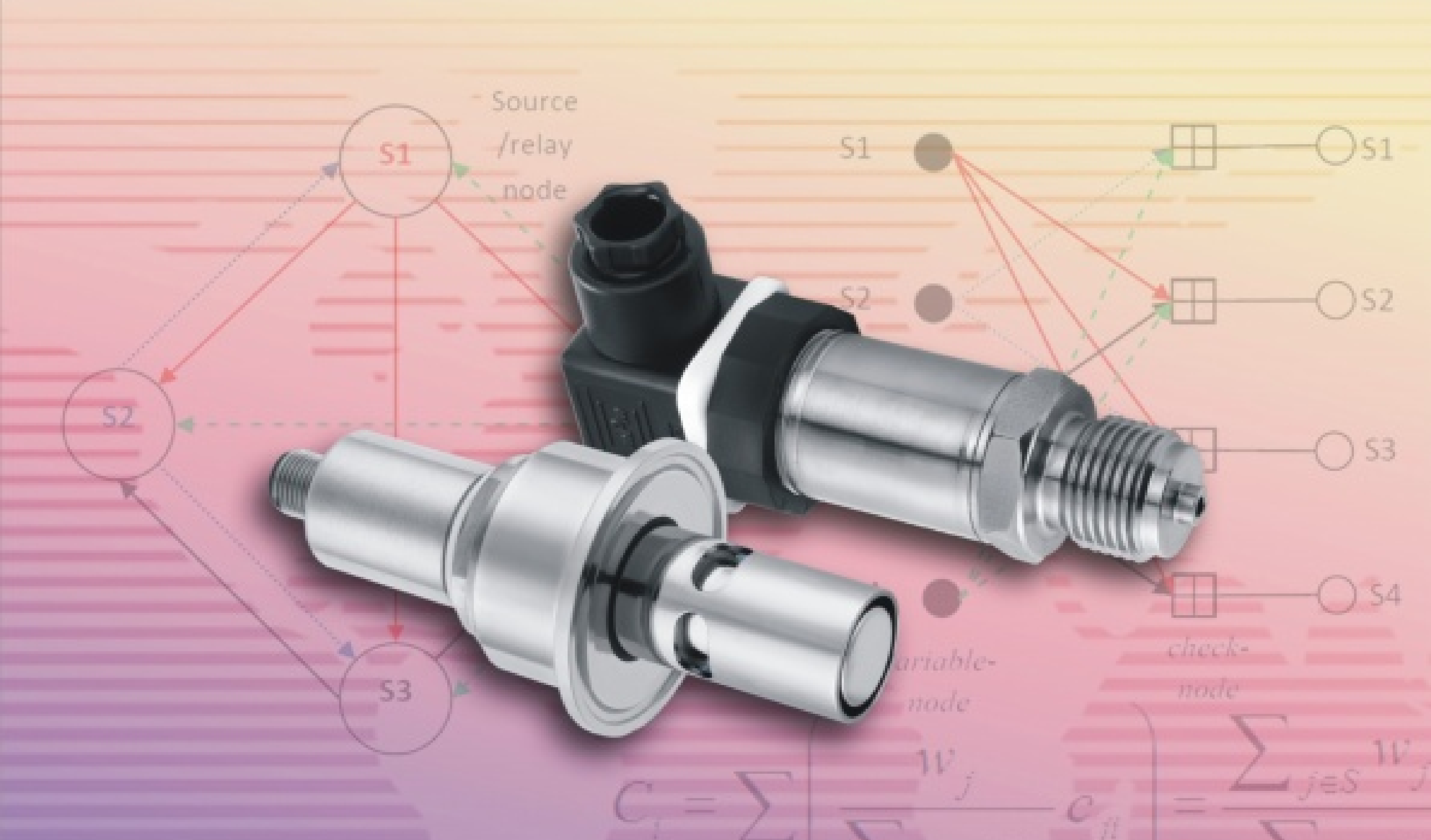

Sensors, Networks, Control Systems and Information Processing

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Volume 20, Special Issue, April 2013

Editor-in-Chief
Sergey Y. YURISH

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Implementation of Closed Loop Control System of FOG Based on FPGA

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Abstract: The stability, reliability and miniaturization of fiber optic gyro (FOG) are always the research focuses and difficulties. This paper presented a design method for the digital closed loop control system of FOG based on FPGA. The proposed twice closed loop technique improved the zero-bias stability of FOG. The using of FPGA brought the digital signal processing by software, the system reliability and agility enhancement as well as the system miniaturization. We also developed some samples of FOG using this design method. The experiments and tests show that the proposed method is efficient and valuable. The zero-bias stabilities of all samples are less than 0.075 deg/h. *Copyright © 2013 IFSA.*

Keywords: Fiber optic gyro, Digital closed loop, Second closed loop, FPGA, Circuit design, Software design.

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1. Introduction

As a novel angular rate sensor, the fiber optic gyro (FOG) has many advantages, such as completed solid state, small size, light weight, long using life, low cost and high anti-impact capability [1]. It has been paid widely attention by the world and increased investment in its research and development annually. It also has been applied to the field of the inertial measurement in the areas of space productions, military productions and civilian productions.

The basic principle of interferential FOG based on the Sagnac effect [2-7] and the reciprocity theorem of its component are introduced in this paper. The work characteristics of the digital closed loop applied to FOG are also analyzed. And the key techniques of signal processing of the digital closed loop are discussed particularly. According to the design requirements, the digital closed loop feedback control system of FOG is implemented. On the basis of the amount of testing, the parameter adjustments of modules in the closed loop control system are summarized, and the relevant circuit is schemed out. At the same time, the software based on FPGA is developed and debugged. Finally, the software and hardware circuit are combined to form an integrated closed loop circuit for detection and control.

2. Digital Closed Loop Technique of FOG

2.1. Main Frame

In passed years, the digital scheme of FOG occupied a dominant position gradually. Its principle can be described by a style, in which the original analog signal should be quantified a digital available measuring range quantity as early as possible and processed in digital field, then the processed digital signal should be converted into an analog signal by D/A convertor to control the system.

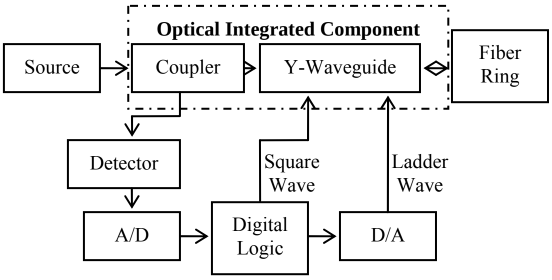

Fig. 1. The frame of closed loop control system of FOG.

The typical system mainly consists of optical source generator, photoelectric detector, A/D convertor, digital logic module, D/A convertor, optical integrated component (coupler, Y-waveguide) and optical fiber ring [8-10]. Its frame is shown as in Fig. 1. In this system, we input the phase modulation signals with the ladder wave and square wave into the interferometer through the optical integrated component. The ladder wave is applied to counteract the Sagnac phase shift through closed loop feedback control. The square wave is as an offset signal to enable that the output signal of the Sagnac interferometer has a linear relationship with the phase shift signal. The step height of the ladder wave is the measured Sagnac phase shift, which is the angular rate signal. In this scheme, besides the output of detector, the drive signals of ladder wave and square wave, the main signal processing is done in the digital field to avoid the circuit noises and to improve the measuring precision [11]. Hence, this scheme is one of the main methods of signal processing system for the medium or high precision FOG.

2.2. Basic Principle

The phase difference of FOG can be obtained through measuring the intensity of the output of the photoelectric detector. The light intensity variable P of the output from the Sagnac interferometer has a relationship with the Sagnac phase shift ΔS as following [11]:

$$P = P_d\left[1 + cos\left(\Delta\phi_S + \Delta\phi_{FB} + \phi_f\right)\right], \qquad (1)$$

where P_d is the amplitude of light intensity, ϕ_f is the phase shift generated by the square wave modulation as shown in Fig. 2, and $\Delta\phi_\text{FB}$ is the phase shift of ladder wave generated by the closed loop control system as shown in Fig. 3. From this equation, we know that the light intensity is a cosine function of phase shift. But, the output light intensity can not reflect the direction of rotation, and the system has a lower sensitivity. Therefore, the system should be added a nonreciprocal ±π/2 phase offset through the square wave modulation. In the light path, we draw two alternative phases with the values of π/2 and -π/2 into two lights in the opposite directions. These two states have their own output light intensities respectively:

$$\begin{aligned} P_2 &= P_d\left[1 + cos\left(\Delta\phi_S + \Delta\phi_{FB} + \pi/2\right)\right] \\ &= P_d\left[1 - sin\left(\Delta\phi_S + \Delta\phi_{FB}\right)\right] \end{aligned}, \qquad (2)$$

$$\begin{aligned} P_1 &= P_d\left[1 + cos\left(\Delta\phi_S + \Delta\phi_{FB} - \pi/2\right)\right] \\ &= P_d\left[1 + sin\left(\Delta\phi_S + \Delta\phi_{FB}\right)\right] \end{aligned}, \qquad (3)$$

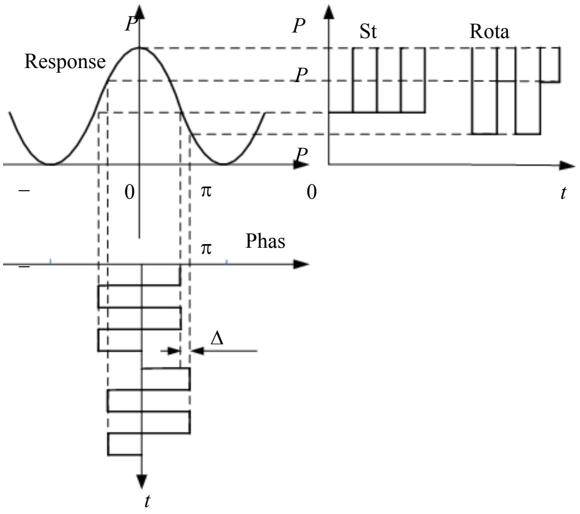

Fig. 2. Schematic diagram of square wave modulation.

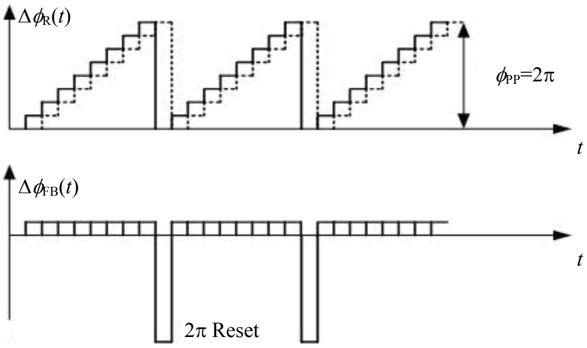

Fig. 3. Schematic diagram of ladder wave modulation.

To do the different demodulation for Eq. 2 and Eq. 3, we obtain

$$\Delta P = P_2 - P_1 = -2P_d sin\left(\Delta\phi_S + \Delta\phi_{FB}\right), \qquad (4)$$

In the Eq. 4, the Sagnac phase shift $\Delta\phi_\text{S}$ is always approximately equal to $\Delta\phi_\text{FB}$ and their signs are opposite, because the added ladder wave is used to counteract $\Delta\phi_\text{S}$. Therefore, $\Delta\phi_\text{S}+\Delta\phi_\text{FB}$ is always approximately equal to 0, then we have

$$\begin{aligned}\Delta P &= -2P_d \sin(\Delta\phi_S + \Delta\phi_{FB}) \\ &= -2P_d \sin(\Delta\phi) \approx -2P_d \Delta\phi\end{aligned}, \qquad (5)$$

Apparently, if $\Delta\phi_{FB}$ can counteract completely $\Delta\phi_S$, that is $\Delta\phi=0$, ΔP should be equal to zero. If $\Delta P\neq 0$, it is said that the nonreciprocal phase shift generated by the ladder wave does not counteracts the nonreciprocal phase shift caused by rotation yet. This time, we can take ΔP as an error control signal to change the step height of ladder wave through the closed loop system to counteract $\Delta\phi$. The additive nonreciprocal phase shift generated by ΔP through the closed loop system is

$$\Delta\phi' = K\Delta P, \qquad (6)$$

where K is the scale coefficient to generate the nonreciprocal phase shift through the closed loop system. Then we have

$$\begin{aligned}\Delta P_1 &= -2P_d(\Delta\phi + \Delta\phi') \\ &= -2P_d(\Delta\phi - 2P_d K\Delta\phi), \\ &= -2P_d\Delta\phi(1 - 2P_d K)\end{aligned} \qquad (7)$$

If $2P_dK=1$, then $\Delta P_1=0$, the control error of the digital closed loop system is zero, it is indicated that the closed loop reaches balance. If $2P_dK\neq 1$, then the closed loop feedback control will be continued. After feedback controlling n times, the system will be in a state as following

$$\Delta P_n = -2P_d\Delta\phi(1 - 2P_d K)^n, \qquad (8)$$

From Eq. 8, we know that when $0< P_dK <1/2$, the closed loop system can be monotonic convergence and will reach the balance gradually. The condition $0< P_dK <1/2$ can be ensured by the system design.

When the closed loop system reached the state of balance, the angular rate of rotation can be calculated by the equation as following and be measured by the FPGA module.

$$\Omega = -\frac{\lambda C}{2\pi LD}\Delta\phi_{FB}, \qquad (9)$$

where λ is the wavelength of the optical source, LD is the product of the length of optical fiber rings and the diameter of optical fiber ring.

3. Implementation of Digital Closed Loop System of FOG

3.1. Hardware Design Based on FPGA

The scheme used in this paper is the continuation of the traditional idea for designing the closed loop control system of FOG, which consists of 6 components such as optical source generator, integrated light path, coupler, optical fiber ring, photoelectric detector and drive control circuit.

Structurally, we choose the integration solution of aluminum alloy material, i.e., the optical source control circuit board and the closed loop control circuit board are fixed in the body of optical fiber rings. We select the super luminiferous diode with a property of wide spectrum as the optical source and do constant power control in whole temperature range (-40~60 °C) using the optical source control circuit board. The used optical fiber is the polarization maintaining fiber and the rings are winded by the quadrupole symmetrical winding pattern [12]. The total length of the fiber coil is about 650 m.

The FPGA based scheme is shown as in Fig. 4. We choose PIN/FET with bandwidth about 7~8 MHz as the photoelectric detector. From the photoelectric detector to the post amplifier, all modules compose the digital closed loop control circuit, and they are integrated into a single PCB as a control circuit board of FOG. In the following sections, we will discuss the implementation of the control circuit board.

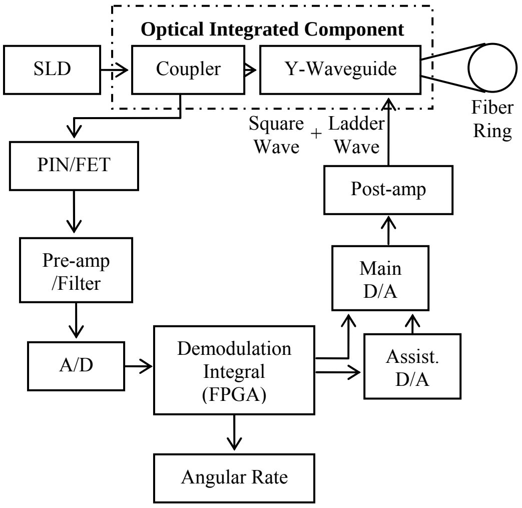

Fig. 4. The frame of closed loop control system of FOG based on FPGA.

3.2. Preamplifier and A/D Module

Since the optical signal is complicated relatively, after photoelectric converted, the electric signal come out from the detector has plentiful noises. As a signal picking up amplifier, the preamplifier needs to suppress the noises as clean as possible but must ensure its effective bandwidth. Therefore, we choose an operational amplifier with high rate, low excursion and low noise as the preamplifier. And we also design a cascaded directly coupled amplifier as shown in Fig. 5 to magnify the signal. Its gain should be adjusted according to the sensitivity of FOG and the precision of the closed loop control.

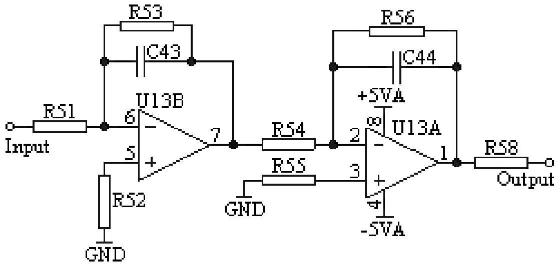

Fig. 5. The circuit of preamplifier.

After amplified, the signal should be converted from analog field into digital field to be processed conveniently. Due to existing of the white noise in the circuit, the A/D convertor should meet some requirements. If the LSB of A/D convertor is smaller than the standard deviation of the noise, then the sampling against the signal will be satisfied. According to the analysis, the ratio of the standard deviation of the noise over π/2 offset power is 2.83×10^{-3}. For this order of magnitude, it is enough to satisfy the requirements of circuit in the whole dynamic range when we just use a 12bit A/D to convert an analog signal to a digital signal. The digital integrator may bring the noise suppression like a low pass analog filter, but there is no long-term drift existing in the electronic circuit generally [9].

Additionally, we should consider the Eigen frequency of system when doing A/D conversion. In our scheme, it is about 158 kHz. In order to reduce the influence from noise to signal, the performance of A/D chip should ensure sampling 32 points at least in a semi-cycle (316 kHz). At the same time, it should keep away from the peak of comb wave in favor of mean treatment. Therefore, the operating frequency of A/D sampling chip is at least 15 MHz.

3.3 FPGA Logic Module

The main functions of FPGA include the integral filtering to the sampling signal, the digital generation of closed loop control, the digital generation of second closed loop control, the digital composition of square wave and ladder wave, the output of closed loop control and the output of angular rate.

Its complete parallel processing enables FPGA to control the event of every time edge and process the relative data on micro point as well as hold the direction of data stream and process the data on macro point. The system connection diagram of FPGA [13] is shown as in Fig. 6. The digital logic in FPGA can be completed by software. Its detail will be described in the section 3.5.

3.4. D/A Module and Post Amplifier

The final part of the digital closed loop control system is the module for phase excursion control from the control voltage output to Y-waveguide. As a vital part of closed loop circuit, it should guarantee the integrality of signal strictly and satisfy the necessary regional linearity.

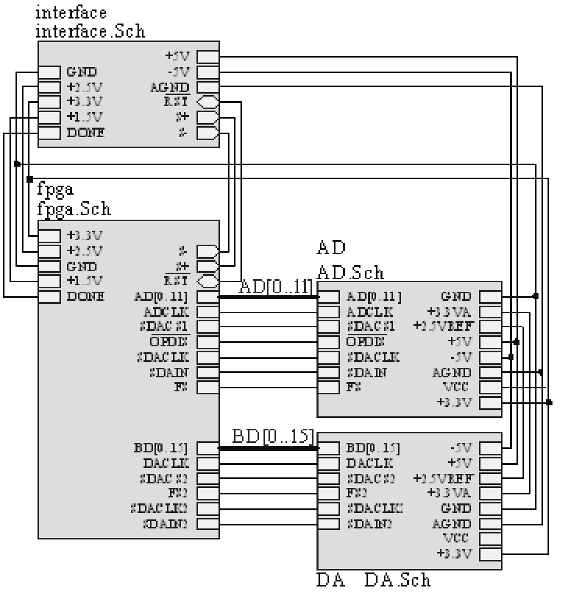

Fig. 6. The connection diagram of FPGA.

On the basis of full considering cost, energy consumption and performance, we select a 16 bit D/A convertor as the main D/A module and a 14 bit one as the assistant D/A module in practice. The main D/A is controlled using parallel interface, while the assistant D/A can only communicate with FPGA using SPI protocol because of the finite pins of FPGA. The two D/A modules are required of having higher establishing times, which are far shorter than the transition time of a light going through the fiber rings.

The basic connection idea is: the FPGA connects with and controls the main D/A and the assistant D/A. then take the output of the assistant D/A as a reference value and input it to the main D/A, form a closed loop circuit to control its gain and also provide a hardware for the second closed loop control. Finally, the output signal of the main D/A is magnified by two cascade operational amplifiers, and the result will be input into Y-waveguide with the difference method. The circuit of post amplifier is shown as in Fig. 7.

3.5. Software Design of FPGA

FPGA is a logic gate array, which is composed of many independent macrocells. These macrocells can be marked out some mutual non-interferential logic unites, which can work in parallel style. The signal exchange between the different logic unites can be realized through simple logical connections or some trigger levels [13]. This digital logic completely fits the demands of the application of the closed loop control system for FOG. The flow chart of works in the FPGA can be described in Fig. 8. Its brief introduction will be presented as follows [14]:

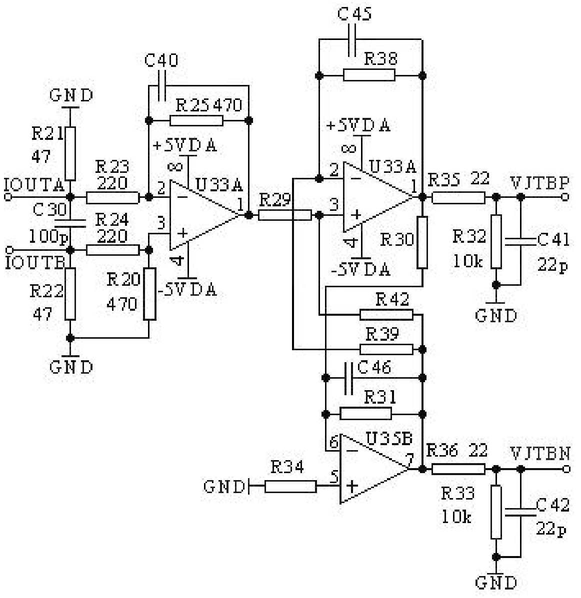

Fig. 7. The circuit of post amplifier.

3.5.1. Sequential Process of the Eigen frequency

The working frequency of the main modules is on the basis of the operating frequency of A/D and depends on the counter to get the working clock of D/A. When the working frequency of A/D is about 20 MHz, the counter stepping on one unit will influence the frequency of D/A about 1 kHz. Certainly, if requiring a higher precision of the frequency of D/A, we can try to use phaselocked loop to improve the input frequency, to apply two cascaded counter to refine the assignment of the frequency points, or to adopt a proper crystal to realize it.

3.5.2. Sequential Process of the First Closed Loop of System

After the clock sequence worked, A/D should do sampling on a more stable wave to keep away from the uncertain points of the comb wave. Now, we select the middle of the comb wave to do sampling and get about 20 points thick and fast. Then, we do integral calculus to them and reckon it in the register of the front semi-cycle. In the same way, we can get the register value of the back semi-cycle. In the late stage of the clock sequence, we can do difference using the values in two registers to obtain the demodulation value. Finally, we do indefinite integral for the demodulated value to do closed loop accumulation and trigger a time edge to do data analysis for the digital closed loop control system.

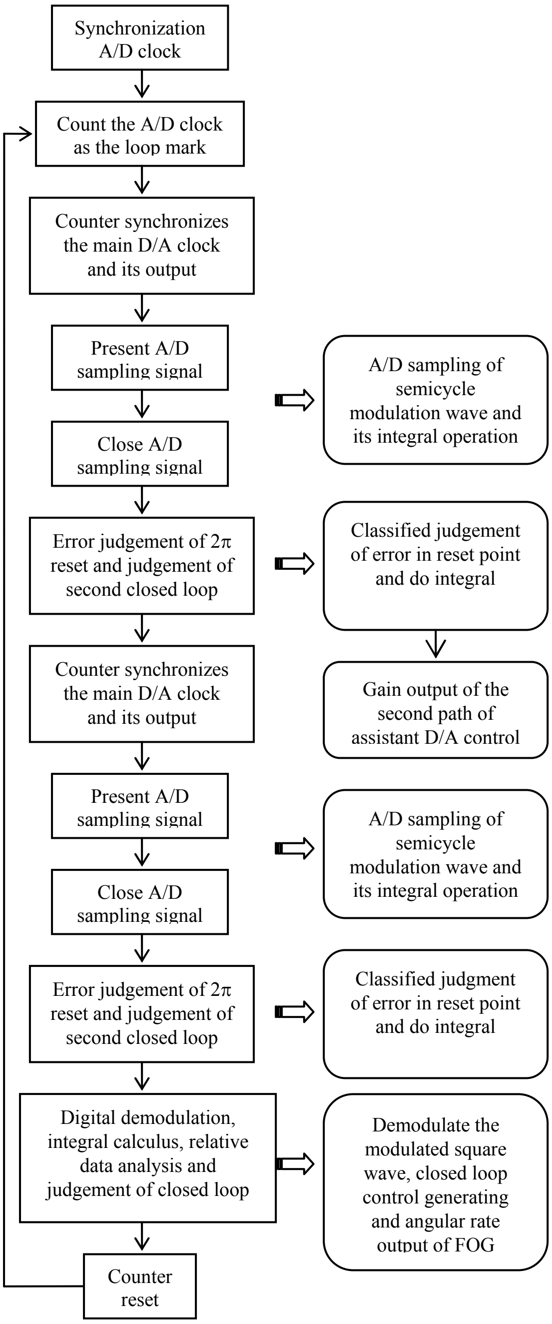

Fig. 8. Flow chart of software working in FPGA.

3.5.3. Sequential Process of the Second Closed Loop of System

The error required by the second closed loop is generated on the time of 2 resetting. Therefore, the record of resetting for the first closed loop should be used as a criterion for the second closed loop. The value accumulation of the second closed loop takes place on the end of twice A/D sampling, its happening precondition is the current signal has been reset. It will trigger a time edge to enable the data analysis module of the second closed loop to go operation.

3.5.4. Sequential Process of the Data Output of System

According to the system design, we know that its output bandwidth is about 400 Hz. In the process of system sequence operation, we use a counter to synchronize the data of each closed loop. When the counter accumulation reaching to 256, it will trigger the output module and generate the output value. In this system, the Eigen frequency is about 158 kHz. Hence, the largest output frequency is 158 k/256 ≈ 617 Hz, which can satisfy the demands of system.

4. Testing Results of Samples

We have developed some samples of FOG using the design method described in above sections and programming in FPGA with relevant algorithms. We also tested them using the performance items of scale factor and zero-bias through the test experiments.

4.1. Scale Factor Testing

The scale factor represents the proportional relation between the change of input rotation rate and the change of output of FOG. According to the measured input data and output data in the whole range of input rotation rates, we can use the least square method to calculate the slope of them. That is the scale factor.

Through the experiment test, we obtained that the scale factor of our samples is about 0.0001154 deg•s/LSB, no matter the rotation direction of FOG.

4.2. Zero-bias Testing

The zero-bias is the output value of FOG when it is at zero input state. It can be expressed by an equivalent input rotation rate, which is converted from the mean of the output values in a considerable long time. Ordinarily, the steady state output in a long time can be described as a stationary random process. It will fluctuate around the zero-bias. Commonly, this fluctuation can be denoted by mean square deviation, which is used to define the stability of zero-bias with a unit of deg/h. It also stands for the precision of FOG.

Through the experiment test, we knew that the zero-bias stabilities of all samples are less than 0.075 deg/h. The experiments and tests show that the proposed method is efficient and valuable.

5. Conclusions

This paper presented a design method for the digital closed loop control system of FOG based on FPGA and developed some samples. Due to apply the twice closed loop technique, the zero-bias stability of FOG had been improved. After the test to the samples, the result data show that their zero-bias stabilities are all less than 0.075 deg/h. Therefore, this method proposed in this paper is efficient and valuable. In addition, the agility of signal input and output interface of FPGA is convenient for hardware design. And, the digital signal processing by software is also convenient for parameter adjustment in experiment. This technique can greatly shorten development period, improve the reliability of system and realize miniaturization of FOG.

Acknowledgements

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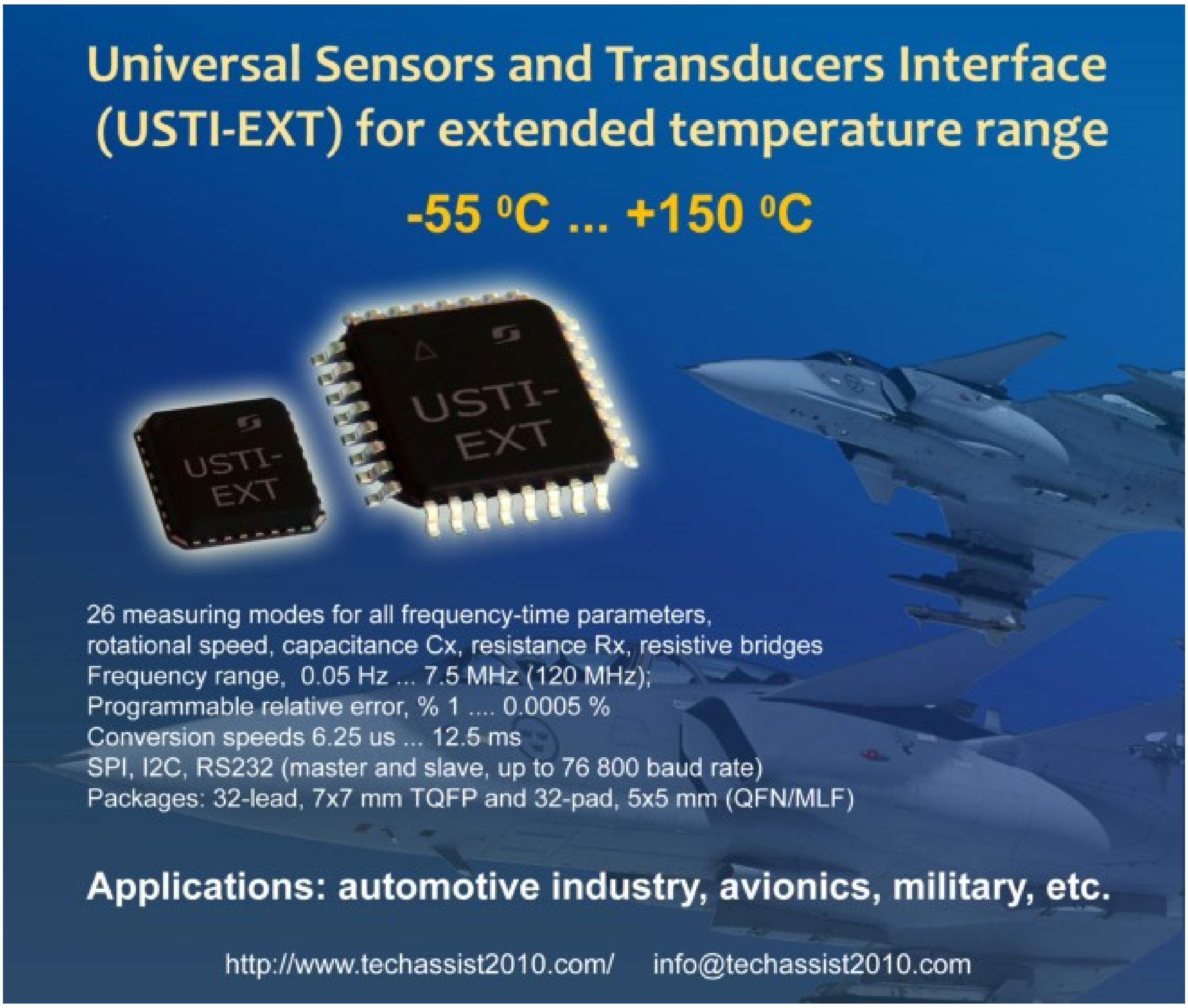

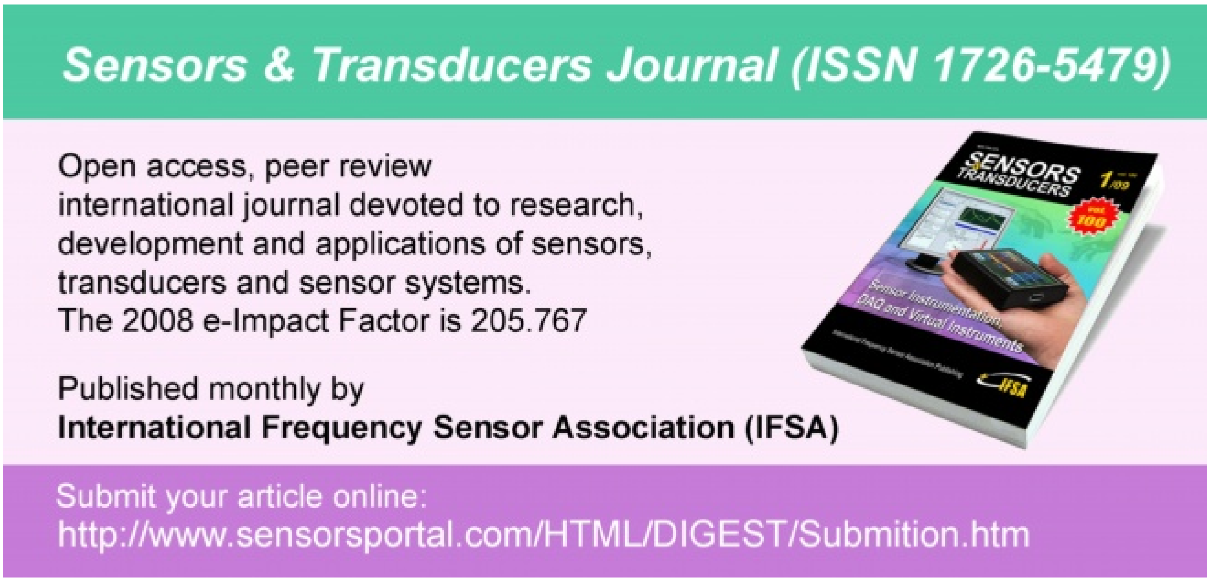

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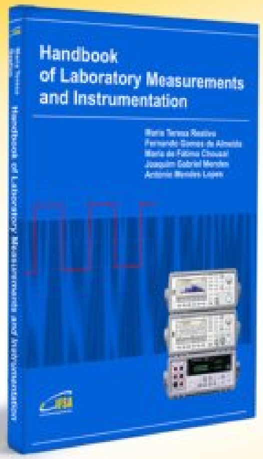

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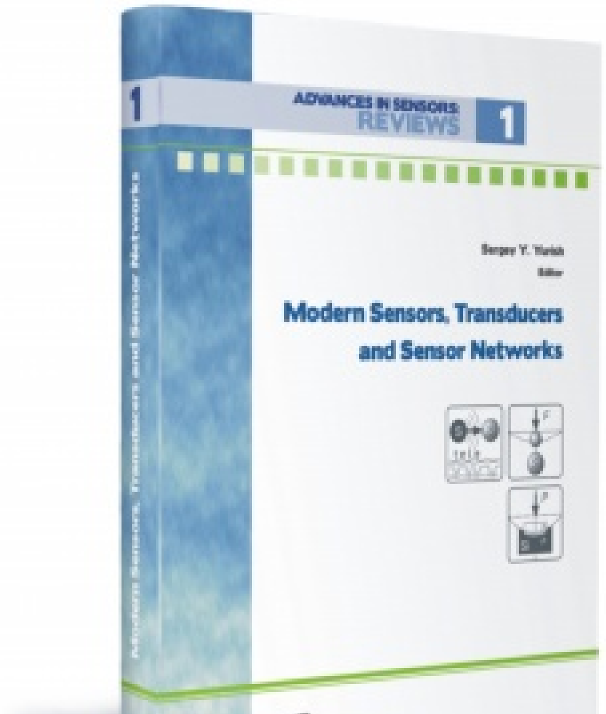

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