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High-precision Position Detection and Real-time Fast Response Designed for Switched Reluctance Motor Drive

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Abstract: It is necessary to detect the high-precision rotor position and control real-time drive for a high-performance switched reluctance motor (SRM) drive. Its optimal control is based on the accurate rotor position information. And the controller processing ability directly influences the effect of control strategy and the motor's real-time response. In terms of the defect that traditional SRM drive can't meet the high-precision requirement and the single processor adopted as controller is limitable to process in real time, this paper puts forward a new control proposal that adopts absolute encoder to produce high-precision SRM rotor position signal, and designs an all-digital controller with digital signal processor (DSP) and complex programmable logic device (CPLD) based on SPI bus communication, which could appropriately combines the fast real-time operation of DSP with the reliability of logic processing of CPLD, achieving SRM high-performance drive. Moreover, the designed system has been applied on the SRM prototype motor and realizes the goal of SRM high-precision rotor position detection and control, thus carries out angle optimal control better, improves the system's real-time response and output torque as well as accelerates its starting process. So the system makes a great progress in the real-time response ability and output performance. *Copyright © 2013 IFSA.*

Keywords: Switched reluctance motor, Rotor position, DSP, CPLD, Absolute encoder.

1. Introduction

SRM performs well as simple structure, strong fault-tolerant ability and high efficiency and wide-speed range [1-2]. And it is widely used in electric vehicle, domestic appliance, aerospace industries and other fields [3-5]. SRM energizes or de-energizes phase windings by position signal produced by position sensor. It utilizes position signal to form speed close-loop and accomplishes self-synchronizing operation. As a result, rotor position detection is an extremely important part. It is quite meaningful to realize SRM commutation and performance optimization [6-8]. Especially for high-performance SRM drive, the real-time accurate feedback of rotor position information is the prerequisite. As a result, the two factors including the accuracy of rotor position signal and the real-time function of controller response influences SRM precise control.

Opto-couplers are low-cost and usually used to provide SRM position information. Taking a three phase 12/8 SRM as an example this paper shows, three opto-couplers generate an opto-couplers edge for every 7.5° mechanical rotation. This position signal can't satisfy the requirement of rotor position resolution for SRM drive variable angle control. Despite the fact that adoption of hardware or software angle subdivision improves resolution in a certain extent, its defects are also obvious [9]. The hardware angle subdivision is easily disturbed by outside, leading to the abnormal phenomenon that the frequency-multiplied output waveform is asymmetric. Adopting phase-locked loop on angle subdivision will create some delay to lock. The software angle subdivision increases calculation tasks and occupies more controller resource, which goes against real-time requirement for high-performance control. In the actual system, owing to that the signals from three-phase position sensors are not totally symmetric, the accuracy based on this kind of angle subdivision is affected. Additionally, traditional SRM drive adopts single processor as controller which is hard to meet the requirement of the real-time drive and high-performance control [10].

In order to achieve high-performance SRM drive, it is necessary to acquire real-time high-precision rotor position information. This paper adopts absolute encoder to produce high-precision SRM rotor position signal and designs a digital controller with DSP and CPLD. The controller takes advantage of digital signal processor (DSP) and its strong ability on computation and fast speed on data processing as well as multifunctional peripherals and additionally equips it with complex programmable logic device (CPLD) that has hardware logic describing and parallel processing abilities to comprise SRM drive central controller. SPI bus communication benefits these two sides and makes them coordinate and realize the optimization and integration of control resource to accomplish SRM detection, optimal control and drive. It has been applied to practical SRM drive successfully and achieves the goal of SRM high-precision rotor position detection and control, thus carries out angle optimal control better, improves the system's real-time response and output torque as well as accelerates its starting process.

2.SRM Drive Framework

The SRM is a single excited machine, which has a simple structure and superior drive performance over a wide speed range. The switched reluctance motor drive consists of SRM, power converter, controller, position detection and other parts [11]. Its principle diagram is shown in Fig. 1. In this paper, motor is three-phase 12/8 pole SRM. Power converter uses asymmetric circuit which has IGBTs as main switching devices as Fig. 2 shows. Controller is the system center, composed of DSP and CPLD, globally handles speed command, speed feedback signal and other detection information from current sensor, position sensor, voltage sensor, etc [12]. It controls the IGBTs to switch on or off in power converter to excite or de-excite SRM phase windings.

The movement of SRM results from the air-gap reluctance change between stator and rotor. It follows the minimum reluctance principle that is the flux always closes along the way of minimum reluctance. In an SRM drive, it is important to synchronize the stator phase excitation with the rotor position; therefore, the information about rotor position is essential for proper switching operation. Torque in the switched reluctance motor is produced by pulses of phase current synchronized with rotor position. According to the SRM model, when rotor position changes, the inductance on motor windings changes periodically between the maximum and minimum value. What's more, in different inductance regions, the current waveform will change if the turn-on angle θ_{on} and turn-off angle θ_{off} change, leading to different control effect. As Fig. 3 shows, when position signal response delays to bring about commuting improperly, the phase current rises slowly and its maximum value decreases. Consequently the torque decreases correspondingly to weaken the loading ability and even produce brake torque when stator phase turns off with delay. Consequently, the synchronization between the time to switch on or off the energizing phase and rotor position is extremely crucial in SRM drive. Thus, the implementation of angle optimization requires high-precision position feedback in position detection and real-time response of drive control system.

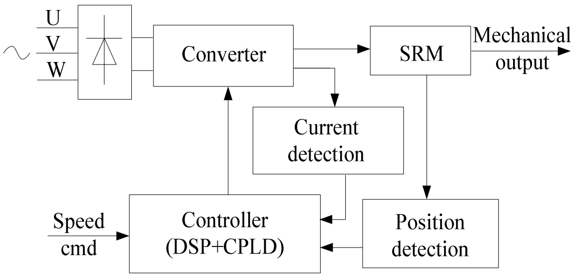

Fig. 1. SRM principle diagram.

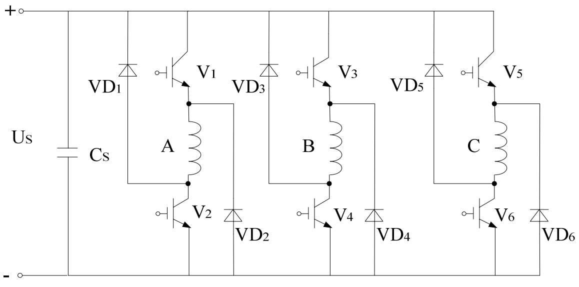

Fig. 2. Asymmetric power converter.

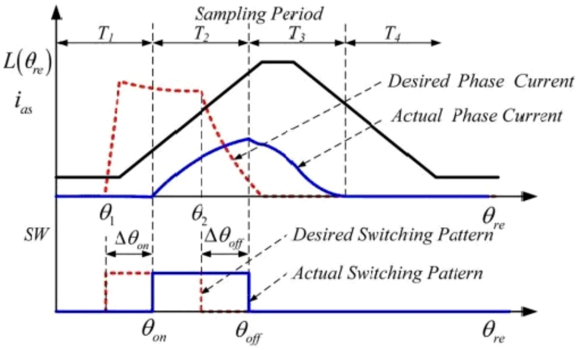

Fig. 3. The delay influence on phase current.

3. Rotor Position Signal Acquirement

Rotary encoder can directly convert angle movement to digital signal. It has two kinds, incremental and absolute encoders. Absolute photoelectric rotary encoder is a sensor which directly outputs digital quantity. It has many advantages including high reliability, power-off memory function, strong anti-interference ability, etc [13]. It is named for the only corresponding relation between every angle position and digital code. Compared with incremental encoder, the advantage of absolute photoelectric axial angle encoder contains fixed zero, output codes with axial angle uniform function, strong anti-interference, dispensability for recalibrating when restarted after power-off, no accumulated errors and so on. As a consequence, it is actually prevalent in many areas [14-15]. According to the diversity of manufacturing process, absolute encoder is divided into binary, binary-decimal, Gray code disc, etc.

The Gray code disc's characteristic is that there is one code change between every two adjacent sectors. When reading, although it changes, there is only one photoelectric tube on the interface, which causes an error on the lowest digit rather than severer error. Thus, this kind encoder has higher accuracy. However, its defect is that it can't directly achieve binary calculation. Before calculating, it is necessary to convert Gray codes to binary codes through logic circuits. The resolution of rotary encoder equals to 360/N, and absolute value code disc $N=2^n$, while n is the digits of output word.

This paper adopts absolute encoder to produce high-precision real-time accurate rotor position signal. The model number of it is EA58C1024G8/28PPX1053PDR with a resolution of 0.35° (360°/1024=0.35°) mechanical angle and the output is Gray code. The resolution can satisfy the requirement of SRM drive sufficiently. The position signal output by absolute encoder, through signal processing and photoelectric isolation, is connected to I/O on CPLD. CPLD converts the Gray code produced by absolute encoder to binary code. Fig. 4 is the connection diagram of acquisition circuit of position encoder signal in one route.

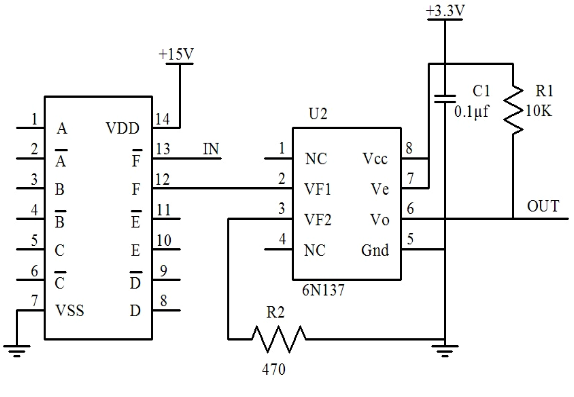

Fig. 4. Position encoding signal capturing circuit.

By experiment, when each stator and rotor's phases are aligned, position encoder's output signal, after CPLD converts, is shown in Table 1 in decimal code.

Table 1. Three-phase (12/8) SRM stator and rotor position alignments in each phase with correspondence to encoder output signals after CPLD converts.

Angle position (mech.) (°)	Aligned position of phase salient pole	Decimal code	Angle position (mech.) (°)	Aligned position of phase salient pole	Decimal code
0	A	1005	180	A	493
15	C	962	195	C	450
30	B	920	210	B	408
45	A	877	225	A	365
60	C	834	240	C	322
75	B	792	255	B	280
90	A	749	270	A	237
105	C	706	285	C	194
120	B	664	300	B	152
135	A	621	315	A	109
150	C	578	330	C	66
165	B	536	345	B	24

4. The Realization of Real-time Controller

In order to improve the response speed of controller, the control device of this system designs digital controller with DSP and CPLD [16]. TMS320F2812 from TI company is selected as DSP which has specialized event manager EVA, EVB blocks, as well as SCI/SPI, 16-route 12 bit high-precision A/D converter and other external interface units. DSP mainly accomplishes close-loop control, control strategy, optimal angle calculation, PWM control output signal, analog signal processing and communication with peripheral devices. The MAX II series low power chip EPM570T100C5 from Altera company is selected as CPLD. It has 570 logic units. The clock frequency that CPLD uses is 10 MHz with less 10 ns gate delay, which satisfies real-time function. In this paper, CPLD is mainly responsible for detecting rotor position signal, chopping current, judging commutation logic, driving power converter, processing fault signal and inputting peripheral digital signal. Compared with single processor mode in traditional SRM drive, CPLD can replace DSP to finish position detection, then reduce the I/O occupation on DSP and relieve its burden. Besides, the method of adopting CPLD to complete commutation control as well as power converter drive improves the system real-time response ability and reliability.

The system principle figure is shown in Fig. 5. CPLD detects SRM rotor position pulse signal output by encoder and converts Gray code into binary code.

In addition, CPLD transmits one position signal to the CAP on DSP. DSP captures this signal and calculates speed in real time. According to the speed, current, voltage and other information, DSP calculates the optimized commutation angle which is sent to CPLD through SPI bus. According to different control methods, CPLD carries on commutation logic control, decides IGBTs in power converter to turn on or off in order to control each phase winding of SRM, keeping motor operating normally.

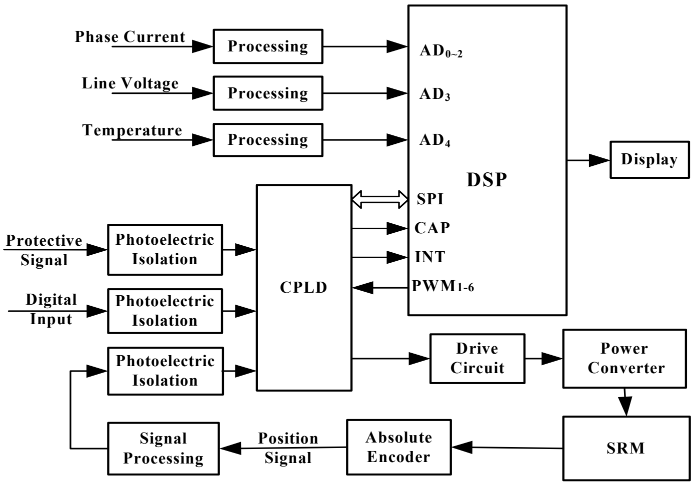

Fig. 5. System control structure.

In this system, one essential task of CPLD is to convert Gray code output by encoder into binary code. Its specific conversion rule is that keep the highest digit of Gray code as the natural binary code, and the second highest binary digit is the exclusive-OR result between the second highest digit of Gray code and the higher digit of binary code. The other digit of binary code is similar with the second highest digit. Taking the ninth digit in binary code as an example, its VHDL decoding program is as follow.

```
B(8)<=G(10) xor G(9) xor G(8)
```

The Fig. 6 is the waveform of Gray code output by position encoder when SRM rotates and binary code through CPLD conversion. The upper half is B10 to B0 from top to bottom, which is the tenth to the zero binary code after converting. The lower half is G10 to G0 from the top to bottom which is the tenth to the zero Gray code before converting.

Besides, CPLD mixes and processes some hardware protective signals and transmits them to the external interrupt pin $\overline{\text{PDPINT}}$ on DSP. When the fault appears, $\overline{\text{PDPINT}}$ is set as low level and the timers inside DSP stop right now and all the outputs are high-impedance state to prevent DSP from sending PWM signals. In the meantime, it produces interrupt signal and judges what happens in the interrupt service routine and displays error code on the upper monitor.

5. The Realization of Communication Blocks

In this paper, the controller adopts DSP and CPLD as control method. In SRM drive, due to the fact that there needs to be real-time data exchange between DSP and CPLD, such as optimized turn-on and turn-off angles in each phase, the fast real-time communication between them, to a great extent, influences the whole system's performance. As a result, this paper proposes SPI communication which is fast synchronizing serial communication bus to achieve data exchange. It can once transmit 1-16 bit serial data whose principle is similar to shift register. To realize SPI communication, it only needs to connect clock line, data transmitting or receiving line. Taking use of SPI communication provides DSP and CPLD with convenience to collaborate rapidly and properly combines the real-time fast computation of DSP with the reliability of logical processing of CPLD.

The SPI bus can be divided into two types as three-line and four-line. Its circuit design is simple and highly reliable. In this paper, SPI chooses four-line mode. DSP is set as master unit and CPLD is taken as slave unit. The clock signal is offered by DSP. Here, there are two questions that are necessary to be concerned about SPI. One is to select clock polarity and phase correctly. The other is to keep dataflow synchronous in communication. The clock set of master and slave unit in the paper is to transmit data at dropping edge and to latch data at rising edge. Therefore, it avoids that controller improperly transmits a wrong datum when electrifying and resetting. In addition, through drawing up reasonable communication protocol, the system solves the problem of synchronizing dataflow. That is to add synchronizing data before data blocks and check word at the end of data blocks to form one frame of data of synchronous communication. The converting waveform of SRM rotor position signals is shown in Fig. 6, and the communicating principle - in Fig. 7.

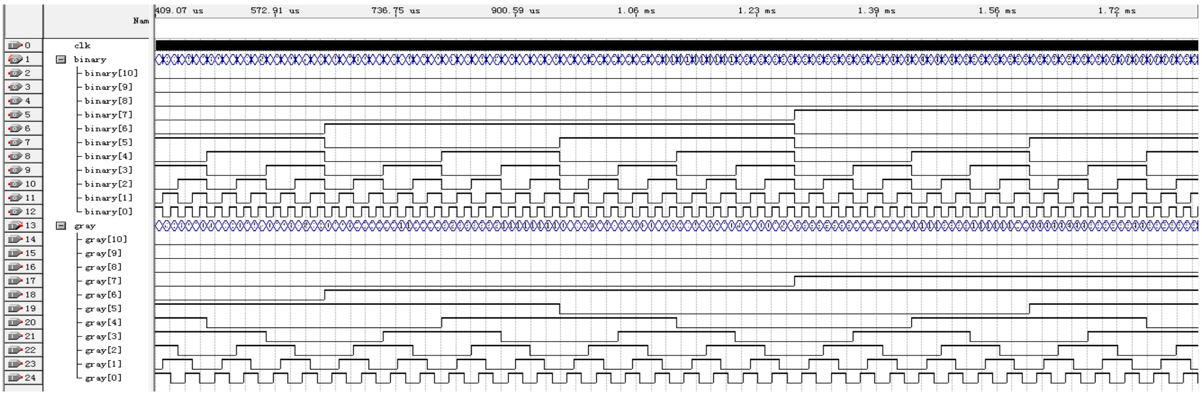

Fig. 6. Converting waveform of SRM rotor position signals.

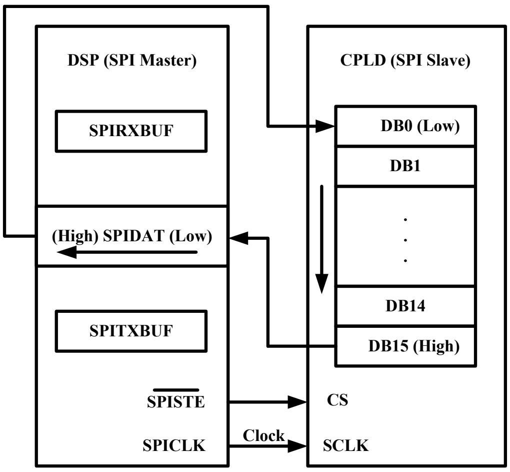

Fig. 7. SPI communication schematic diagram.

SPICLK which is considered as the whole serial network clock is provided by the master unit TMS320F2812’s low speed peripheral clock (LSPCLK). Firstly, SPISTE pin is set low, finishes CPLD chip selection and informs it to prepare communication. Then, write data on SPIDAT (SPI serial data register) or SPITXBUF (SPI transmit buffer register). SPI starts and on the dropping edge of SPICLK through SPISIMO (SPI slave input master output) pin, sends data, to CPLD’s low order DB0 and shift with it. Meanwhile, on the rising edge of SPICLK through SPISOMI (SPI slave output master input) pin, it transmits data to SPIDAT’s lowest effective order. After finishing receiving, data is transferred to SPIRXBUF (SPI receive buffer register) in order to be read by CPU. Finally, SPISTE pin is set high and finishes data exchange and waits for the next communication.

The master unit DSP has specialized SPI communicating interface blocks. Only equipped with relative registers can it operate. The Slave unit CPLD needs corresponding written SPI communicating programs to realize SPI function. As a result of SPI operating principle which is similar to 16 bit shift register, CPLD’s SPI programs are compiled as a 16 bit shift register. Take CPLD receiving DSP data as an example, its partial VHDL code is shown below.

```
  if sclk’event and sclk=’1’ then
                                  –rising edge receives data
    if txcnt=”01111” then
      rxshift<=rxshift(14 downto 0)&din;
      rxcnt<=”10000”;
                                          -- receiving counter
      rec_int<=’0’;
                             -- one time reception finishing sign
    elseif rxcnt=”10000” then
      rxcnt<=”10000”;
      rec_int<=’1’;
    else                                                 -- shift
      rxshift<=rxshift(14 downto 0)&din;
      rxcnt<=rxcnt+”00001”;
end if
```

6. Experimental Results

This experiments uses three-phase 12/8 pole switched reluctance motor with 5.5 kW rated power and a speed range between 100 – 2000 rpm. As this paper states, the Fig. 8 shows one phase current waveform and motor speed waveform when motor starts. During the starting process, according to position encoder signal detected by CPLD, DSP calculates motor speed. According to the principle that is to make output torque maximum, on the base of motor speed and load, DSP also calculates the turn-on and turn-off angle. Then, the optimized angle control information is transmitted by DSP to CPLD which, by comparing optimized turn-on and turn-off angles with the current position, gives the correct time that stator excites or de-excites and achieves SRM angle optimization. High-precision rotor position detection and control makes system carry on angle optimization with very high accuracy and resolution. The control mode that combines DSP and CPLD lays a good foundation for the proposal that starting torque is raised by angle optimization. Consequently, it improves SRM system performance. From the experimental waveform in Fig. 8, with the speed rising, through adjusting control mode and turn-on and turn-off angle, the system has a good effect on quick start.

7. Conclusion

Compared to traditional SRM drive, this paper takes the use of absolute encoder to produce high-resolution-ratio SRM rotor position signal and improves the accuracy and precision of system rotor position signal. On this base, the digital controller with DSP and CPLD is designed. It utilizes their digital processing and hardware logic description abilities which makes the control system more real-time and reliable so that optimization and integration of control resources are both achieved. It also ensures real-time function of controller's response. More importantly, it is successfully applied to practical SRM drive. The experimental results indicate that this method is reliable and effective and able to obtain SRM current rotor position information accurately and timely, and then controls turn-on and turn-off angles, which realizes the goal of SRM high-precision rotor position detection and control, thus carries out angle optimal control better, improves the system's real-time response and output torque as well as accelerates its starting process.

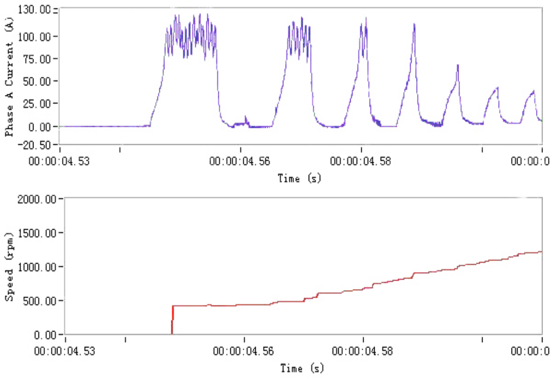

Fig. 8. SRM starting phase current and speed waveform.

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