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Neural Circuitry Based on Single Electron Transistors and Single Electron Memories

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Abstract: In this paper, we propose and explain a neural circuitry based on single electron transistors 'SET' which can be used in classification and recognition. We implement, after that, a Winner-Take-All 'WTA' neural network with lateral inhibition architecture. The original idea of this work is reflected, first, in the proposed new single electron memory 'SEM' design by hybridising two promising Single Electron Memory 'SEM' and the MTJ/Ring memory and second, in modeling and simulation results of neural memory based on SET. We prove the charge storage in quantum dot in two types of memories. *Copyright © 2014 IFSA Publishing, S. L.*

Keywords: Neural circuitry, Single Electron Transistor, Winner-Take-All, Single Electron Memory.

1. Introduction

The SET transistors were introduced by Likharev in 1987 [1]. Single-electron transistors hold great promise for future nanoelectronic circuits due to their small size, low power consumption and ability to perform fast and sensitive charge measurements [2]. Several single electron memory cells have been proposed in the literature such as the single electron FlipFlop, the electron trap proposed by Nakazato and Ahmed [3] ,based on a dynamic memory cell and the single electron ring memory which is "similar" to the electron trap memory because it is a trap connected to a ring and SET/SEM structure [4]. However, the operation is different. Another type of a single electron memory is called 'the Q_0-independent memory', where Q_0 is the background charge. In this memory electrons, which tunnel to the floating quantum dot due to an appropriate voltage on the gate electrode, change the threshold voltage of the narrow channel. The quantum dot stores charge even after reducing the gate voltage and the multiple island memory [5]. It is possible to make a neuron, which its role is to map the information presented at its inputs by synapses onto its input space by means of an activation function, in a several ways using SET transistor. It is possible to generate an activation function similar to the standard sigmoid function using two SET transistors. Two others neuron designs, both based on the SET inverter with two SET transistors are known in the literature [6].

An artificial neural network is a machine composed of a large number of similar and interconnected cells consisting of a small set of mostly non-linear and adaptable building blocks. Neural networks are suitable to help us solve certain types of problems such as the recognition of patterns, and could become of increasing importance if an efficient way of manufacturing them becomes available.

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Two types of neural primitive function are distinguished: evaluation functions which are contained in two types of building blocks (neuron and synapses) and learning function. Competitive nets, like winner-take-all (WTA), provide easiness of operation due to their non-supervised training [7]. In addition, WTA has a relatively reduced number of control signals, self-organization, local memory and low connectivity when adopting a lateral inhibition configuration [8]. WTA nets are used for decision making, pattern recognition and image feature extraction.

In the first section, we describe a schematic SET model and present a Coulomb oscillations using SIMON (Simulation of Nano-structures) software [9]. Then, we simulate and model neural network based on SET device after presenting an electrical model of one neuron and the Transfer function of the SET inverter structure based neuron. In the second section, SET WTA architecture with 2 neurons is presented and the confrontation between MATLAB and SIMON simulations are realized. Section 3 explains the process storage of the proposed hybrid MTJ/Ring memory and neural memory based on SET can store electrons in the quantum dots.

2. Neural Circuitry Based on SET

The single Electron Transistor is the simplest known device that can be constructed with SET junctions. It consists of two tunnel junctions connected in series, and a gate electrode which is either capacitively or resistively connected to the island formed by the node connecting the two junctions [9].

As showed in Fig. 1, SET can be simply treated as 3-teminals (gate, source and drain) device, and, there is a so called Coulomb island between source and drain, where only one or several electrons are permitted to pass over at the same time. As the special nature of SET, Coulomb Oscillation is that with the gate voltage changing linearly, the current between source and drain exhibits periodic changes. In other words, the source-drain current is the periodic function of the gate voltage. In fact, Coulomb Oscillation can be considered as current pulses under the gate's voltage.

The current flow through the SET consists of individual electrons tunneling through the source to the island and the island to the drain. Whet her electrons tunnel, depends on the charge present on the island enclosed by the dotted box. This charge changes discretely with the elementary charge e when electrons tunnel through the junctions and can be modified continuously with charge q by a voltage over gate capacitor.

The tunnel current for single electrons through the junction is:

$$I = \frac{\Delta Q}{\Delta t} = \bar{e}.\Gamma, \tag{1}$$

where Γ is the tunneling rate, and ΔQ is the difference of charge. [11]

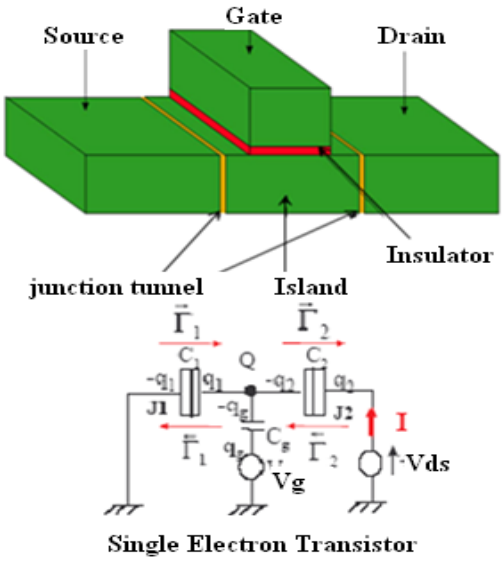

Fig. 1. SET structure and its equivalent circuit.

The rate of tunneling events is given by the orthodox theory

$$\Gamma = \frac{\Delta W}{e^2 Rt\left(1 - \exp(\frac{-\Delta W}{KT})\right)},$$

and

$$\Delta W = e\left(U_c - \frac{e}{2C_\Sigma}\right), \tag{2}$$

where ΔW is the drop of electrostatic energy.

Because of current conservation, $I(V)$ can be calculated on any junction according to the following equation [10].

$$I(V) = e\left(\sum_{n=-\infty}^{+\infty} p_n\left(\vec{\Gamma}1(n) - \overleftarrow{\Gamma}1(n)\right)\right) = e\left(\sum_{n=-\infty}^{+\infty} p_n\left(\vec{\Gamma}2(n) - \overleftarrow{\Gamma}2(n)\right)\right), \tag{3}$$

which

$$p_n = p_0 \prod_{m=0}^{n-1} \frac{\Gamma_{m+1,m}}{\Gamma_{m,m+1}}, \tag{4}$$

SET transistor is capable of performing more advanced functions than simple current switching. The device can calculate a weighted sum of multiple

input signals at the gate level. The result of the sum operation determines the output state of the transistor.

There are two fundamental elements used to compose a neural network: the synapse and the neuron. The complete structure of the neuron is presented in Fig. 2. It acts as an adder, and provides the output nonlinearity and the required gain. It is quite a standard approach to the activation function generation. The novelty lies in the synapse circuitry [11].

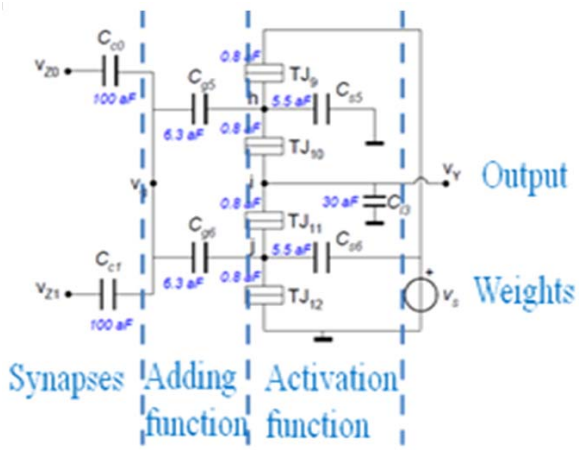

Fig. 2. Two input SET inverter based on neuron.

Fig. 2 presents an electrical model of one neuron SET with three islands where C_{g5} and C_{g6} are the addition capacitors, C_{c6} and C_{s6} are the coupling capacitors, V_{Z0} and V_{Z1} are the inputs voltages and V_Y is the output voltage. This kind of neural circuitry can be considered as a single-electron memory "SEM" with four voltages inputs and capacitors connected to a three-island structure extended with an extra junction. The weight is represented as a voltage at the drain of the 3 islands structure. This neural is composed of a multiplication, an adding and an activation function. The adder is obtained by capacitive coupling, the activation function by cascading two C-SET transistors and the weight is represented as a voltage at the drain of the 3 islands. The circuit receives a voltage input (V_{Z0}, V_{ZN}) from a sum-of-product unit to generate its internal state and produces the corresponding voltage output.

Before this perceptron can be simulated, the desired output has to be defined. In order to check if the output signal is the desired signal, a good test-set of input signals has to be created. In Fig. 3, the transfer function of the SET inverter structure based on neurons is shown. The possible output values are plotted in red.

As it can be seen in this transfer function, we can notice that the input voltage vg for which the output voltage changes, is set to 3.3 mV approximately in this configuration.

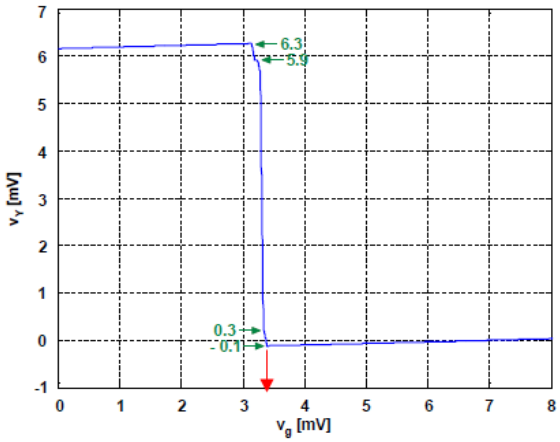

Fig. 3. Transfer function of the SET inverter structure based neuron.

A two-neuron SET-Winner-Take-All (SET-WTA) circuit is shown in Fig. 4. Each neuron has a primary current input unit Ii which brings the data information to the network, and secondary voltage input units (vi−1(t) and vi+1 (t)) which come from the nearest neighbors, as illustrated in Fig. 4. These secondary connections provide the stimulation or inhibition features which are characteristic of WTA networks. Neuron 1 receives as inputs the current I1 and the output voltage v2 (t) from neuron 2. Its single output voltage is v1 (t). The bias voltage V_{bias} has a fixed value [11]. Resistor R_t and capacitor C_t are responsible for the time constant of the circuit, determining the output convergence time.

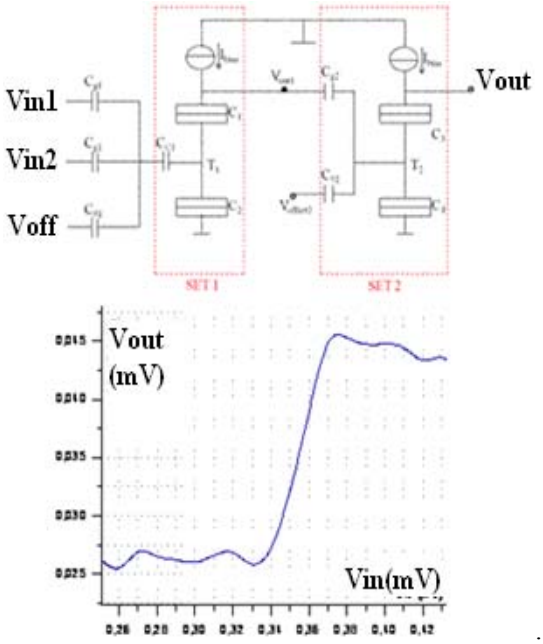

Fig. 4. SET WTA network structure with two neurons and its transfer function.

The SET-WTA network provides the winner output. The SET transistors, connected to the output

of each neuron are used to normalize its value. From their Coulomb Blockade characteristics, it is possible to have a positive value voltage in the winner output only. This value will be taken as a logic "1". All other outputs will be taken as logic "0". The SET WTA network can be used in classification and recognition.

3. MTJ/Ring Memory and Neural Memory Based on SET

3.1. Hybrid MTJ/Ring Memory

In order to prevent the MTJ memory cell, a new single electron memory 'SEM' design by hybridising two promising SEM is proposed. The MTJ/Ring memory, shown in Fig. 5, consists of two key blocs: The MTJ memory cell which is connected to the second bloc: ring memory. The electrons pumped by two inputs voltages will repel each other thanks to Coulomb interaction and, thus, can form two stable configurations represented in red and green in right of Fig. 5. The first configuration is associated to logical '0' having an electron in the islands *N1, N3* and *N5*. The second one designates the writing of logical '1' when the complementary islands trap electrons. The bias variation of two inputs switches the state of the ring to another one of the stable configuration. This is the better advantage of the ring memory. Furthermore, the pure capacitance in this bloc must be small to accentuate the influence of electrons on their neighbours. To reach this hypothesis, great technological difficulties might be confronted. Fig. 5 shows the combination of MTJ and ring memory.

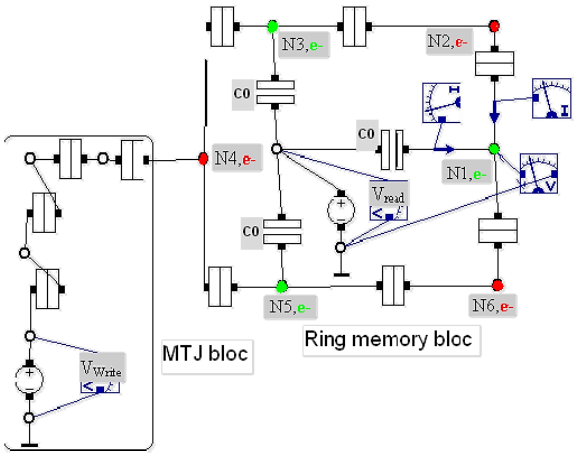

Fig. 5. Schematic circuit of MTJ/ring memory structure. The green points are representing binary information '1' and red points are representing '0'.

The purpose of combining the multi tunnel junction to the ring memory is to load and empty the ring memory. The two stable configurations of the ring memory are used to move the trapped charges around to distinguish between logical zero and logical one. By applying a negative input voltage to V_{write}, the ring memory will produce a coulomb oscillation. If no electrons are trapped in the ring memory, no current will be induced in the single-electron transistor and the presence and absence of coulomb oscillations distinguishes between logic zero and logic one.

The combination of multi-tunnel junction and the ring memory can prevent from random background charge. Fig. 6 shows only the result of the charge q1 (t): the odd charges *q3* and *q5* have the same simulation results. When there is an electron in the quantum dot *N1, N2 and N3*, there is a hole in *N2, N4* and *N6*. When V_{read}=0.65 V, there is not any electron stored in the ring memory after the reset of V_{write}.

By increasing V_{read} to 1V, the number of stored electrons also increases (From 0 to one). In fact, as the gate voltage reduces to 0V, the number of electrons in the quantum dot also reduces, but not to zero (from 3 electrons to one). This situation happens because as V_{read}=1V, the energy that attracts the electrons to the quantum dot is larger than the repulsion of the other electrons. Fig. 6 shows the storage of one electron in the MTJ/Ring memory.

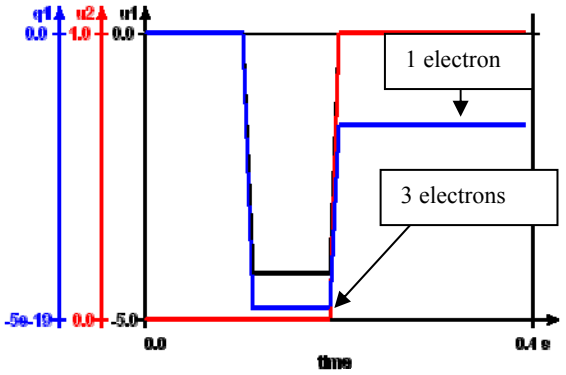

Fig. 6. Storage of one electron in the MTJ/Ring memory.

3.2. Neural Memory Based on SET

Each SEM proposed in the literature differs from the other by such properties as the complexity of the architecture, the dependence of background charges and the operating temperature. One of the most promising applications of single electronics is the single-electron memory named SET/SEM, proposed by A. Boubaker et al [2] who have explained the operating principle and the electrical model of a new SET/SEM device and presented the simulation results, obtained with SIMON Simulator, in Write/Read/Erase cycles. Fig. 7 shows a schematic circuit of neural memory where the summed output is used by the source of a SET transistor as an

illustration of how the summed charge is used. The outputs of SET1 are considered as the input of SET2. This structure is made of three key blocs: a bloc of memory(Write/Erase) with a voltage drain 'V_{Write}', a second bloc of reading with voltages 'V_{Read1}' and'V_{Read2}' and a third bloc of Weight with voltages 'V_{W1}' and'V_{W2}'.

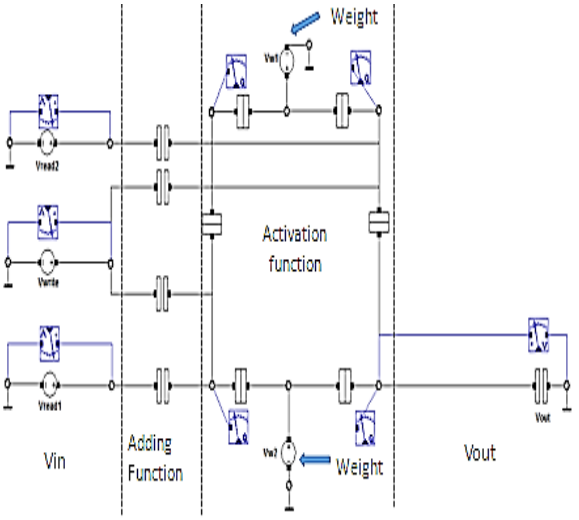

Fig. 7. A schematic circuit of new neural memory based on SET modeling write/Erase/ Read states.

The shape of control signals (*u1(t)* and *u3(t)*) is very important to observe the charge evolution 'Q' versus time. In order to break this lock, different potential signals were applied but it has retained for writing a starting ramp of 0 s and for reading a ramp which starts just after writing.

At first, the voltage 'V_{read} 'is zero and there is no electron at the quantum dot. As 'V_{read}' increases to 0.1 V, electrons are transported to the output. If the slope of V_{read} after writing is kept at 0.1 V for some time, electrons are stored inside the quantum dot and no more electrons will be transported to the quantum dot. Because of the Coulomb blockade effect and the potential barrier, the electron cannot flow back to the ground. When the value of 'V_{read} '=0.3 V, there are 2 electrons in the output island. Finally, Fig. 8 shows the charge, the writing and the reading bias characteristics as a function of the time where V_{read}*>=0.5 V*. It is found out that the portion of the curve, representing the reading of the state, has shifted compared to that of the writing state. In fact, the reading voltage after 1.2 second until 1.5 second with a 0.5 V as maximum of ramp is applied. In this case, the memory stores 2 electrons then 3 electrons. This situation is due to the energy that attracts the electrons to the quantum dot and those are extremely larger than the repulsion of the other electrons. As a result, the number of stored electrons increases from one to three.

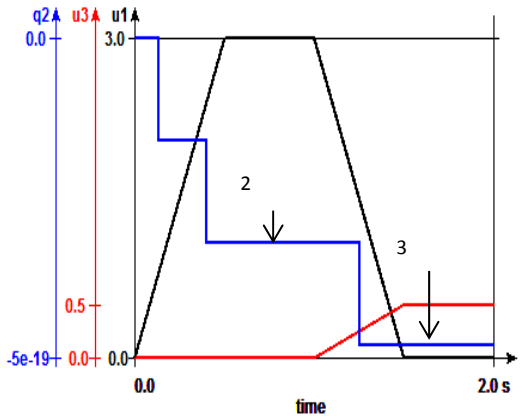

Fig. 8. The timing diagram of the write voltage "V_{Write}=u1(t)" applied to the programming bloc and the reading voltage " V_{Read}=u3(t)" when 3 electrons are stored.

4. Conclusion

Various research groups suggested neural network nodes based on SET devices. This work proposes a new neural node, study and neural network model based on SEM device after presenting synapse and neuron. Thanks to the simulation results, we have illustrated how the MTJ/Ring and our proposal memory neural cell store, erase and read data information. Finally, the double functionality of neuron and memorization cell is explained in order to write and erase electrons. The most promising applications for new neural memory based on SET are in pattern recognition such as speech, handwriting or the recognition of a human face.

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