Sensors & Transducers, Vol. 27, Special Issue, May 2014, pp. 151-155

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Sensors & Transducers

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Interface States Densities Effect at SiO_2/ Polysilicon and SiO_2/ Monosilicon Surfaces on N-polysilicon /Oxide/ P-Monosilicon Capacitance

H. Dib, Z. Benamara, Z. Kari

LTTNS, Université Djillali Liabes Sidi Bel Abbès (22000), Algerie

E-mail: hh_dib@yahoo.fr

Received: 31 December 2012 /Accepted: 10 August 2013 /Published: 26 May 2014

Abstract: the interface states have a very significant role in the components containing MOS structures. In this paper we study the interface states densities effect at SiO_2/ N-polysilicon and SiO_2/ P-monosilicon surfaces on metal/polysilicon /oxide/ monosilicon capacitance. The numerical solution of poisson's equation and the determination of the charge variation in the structure induced by application of external bias (V_g) allow simulating the capacitance-voltage MS^POS characteristics. The results show that the interface states at SiO2/ polysilicon and SiO2/ monosilicon surfaces translate the CT (V) curve about positive voltage and cause the increase of the minimum value of capacitance. The effect of interface states on C (V) curves is neglected for the polysilicon doping concentration in order to 1019 cm^{-3}. For this doping level, the C (V) curves are identical to the C (V) of the monocristalline MOS structure. *Copyright © 2014 IFSA Publishing, S. L.*

Keywords: MS^POS structure, Interface states densities.

1. Introduction

In this document we study the effect of interfacing states on the capacitance voltage characteristics. At the first time, we introduce the traps states density at oxide/mono-Si interface. At the second time, we introduce the interface states at polysilicon/oxide interface. The numerical simulation model of the C_T (V) characteristics versus bias voltage of MS^POS realized on the polysilcon was presented, neglecting the charge density in the oxide. Using a numerical resolution of Poisson's equation and a calculation of the charge variation induced by the application of an external bias, a simulation program of the quasi-static C (V) characteristics of MS^POS has been developed. In our simulation the polycristalline silicon layer is modelized by a series of rectangular crystallites of monocrystalline silicon separated by identical grain boundaries, parallel to the SiO_2/polycristalline Silicon interface. We have analyzed capacitance voltage C_T (V) characteristics of metal /N-polysilicon /oxide/P-silicon structure as function of the interface states density.

2. The Model

The problem is treated one-dimensionally in this paper. We consider a metal/polysilicon /oxide/silicon structure. The silicon substrate is P doped and the polysilicon is N doped. The interfaces polysilicon/oxide and oxide/silicon are located at x=int1 and int2 respectively. It is assumed that the doping concentrations N_D and N_A of the N-polysilicon and P-silicon regions respectively are uniform and entirely ionized at room temperature. In

this computation, we have considered that the N-polysilicon region is composed of five crystallites separated by lateral grain boundaries which are parallel to the polysilicon/ oxide interface. (See Fig. 1). Monoenergetic traps are assumed to be uniformly distributed at the grain boundary of a thickness equal to 1 nm. Traps can be acceptors, donors (N_{TA}=N_{TD}=N_T) when the energetic levels E_{TA} and E_{TD} are symmetrically located in reference to the midgap. To describe these structures, the following physical equations are considered:

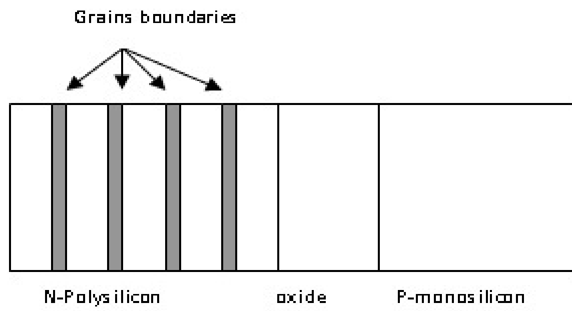

Fig. 1. Geometrical model for the studied Poly-Si/SiO2/Si capacitance.

3. The Basic Equations

The MS^{P}OS was analyzed using the simple energy band diagram of the N-polysilicon/ SiO_2/ P-silicon structure shown in Fig. 2.

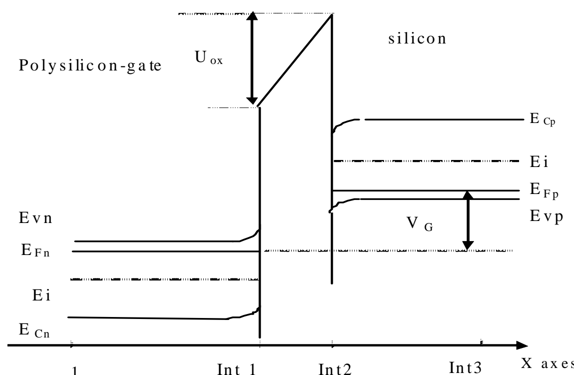

Fig. 2. Band diagram at positive bias.

3.1. Poisson Equation

The Poisson equation can be definite by:

$$\varepsilon\frac{d^2\varphi}{dx^2}=-q(p-n+N_A^- - N_D^+ + N_{TA}^- - N_{TD}^+), \qquad (1)$$

where φ is the electrostatic potential; n, p are the free carriers concentration; N_D^+ and N_A^- are the concentrations of the ionized doping atoms, N_{TA}^- and N_{TD}^+ are the concentrations of the ionized traps; ε is the dielectric constant.

At ohmic contacts, two types of boundary conditions are implanted in this analysis:

$$\varphi(1) = V_G + \left[\frac{kT}{q}\times\ln\left(\frac{N_A\times N_D}{n_{in}^2}\right)\right], \qquad (2)$$

$$\varphi(\text{int}\,3) = \varphi(\text{int}\,3-1), \qquad (3)$$

where (l) and (int3) are the contact positions in the polysilicon and silicon regions respectively. These contacts are considered to be far away from the potential variations. n_{in} is the intrinsic concentration, V_G is the applied voltage.

We used Maxwell-Boltzmann statistics, for the electron and hole free carriers concentration expressions. The ionized traps densities are given by the Shokley-Read-Hall model [2].

3.2. Quasi-static Capacitance Formulation

The total capacitance of the polysilicon-oxide-silicon structure C_T is defined by [3]:

$$C_T = \frac{dQ_G}{dV_G} = -\frac{dQ_s}{dV_G}, \qquad (4)$$

where Q_S, Q_G are the electrical charges in the monosilicon and in polysilicon-gate respectively. Using Q_S= $-\varepsilon_S\times E_S(\text{int}1)$, the capacitance is given by following expression:

$$C_T = \varepsilon_s\frac{dE_s(x_1)}{dV_G} = \varepsilon_s\frac{d}{dV_G}\left[\frac{d\varphi}{dx}\Big|_{x=\text{int}\,1}\right], \qquad (5)$$

where E_S is the field of the polysilicon-oxide interface; ε_S is the silicon dielectric constant.

4. Numerical Solution

The discretization of the studied domain is based on the finite difference method [4], with the use of a sufficiently sharp variable mesh to allow an accurate simulation along the discritized structure. After linearization of Poisson's equation, and at each node, the discritized expression of this equation becomes [5]:

$$A_i\delta\varphi_{i-1} - T_i\delta\varphi_i + B_i\delta\varphi_{i+1} = V_i, \qquad (6)$$

where

$$A_i = 2(\varepsilon_i-\varepsilon_{i-1})/h_{i-1}/(h_i+h_{i-1}) \qquad (7)$$

$$B_i = 2(\varepsilon_i-\varepsilon_{i+1})/h_i/(h_i+h_{i-1}) \qquad (8)$$

$$Ti = A_i + B_i - \frac{\partial \rho}{\partial \varphi}\Big|_{i} \quad (9)$$

$$V_i = A_i(\varphi_{i-1}-\varphi_i) + B_i(\varphi_i-\varphi_{i+1}) - \rho_{I,} \quad (10)$$

where h_i is the distance between the neighboring points in the grid.

At each iteration k the obtained system is solved by the Gauss elimination method to produce the correction $\delta\varphi_i$ of the potential vector φ (Fig. 3). A damping method can be applied to activate the convergence, and the potential φ is given by a difference update:

$$\delta\varphi_i^k = \varphi_i^k - \varphi_i^{k-1} \quad (11)$$

After the convergence, the values of the solution vector φ are used to determine the free carriers concentrations n, p. At the end, the capacitance is calculated by expression (5).

5. Results and Discussion

In this work, we have analyzed the effect of the interface states charges on the quasi-static capacitance-voltage (C_T (V)) of the MS^POS structure. For that the characteristics C_T (V) are simulated with and without interface states.

The physical and technological parameters used in the calculation procedure to simulate the C_T (V) characteristic of the MS^POS structure are reported in Table 1.

Table 1. The physical and technological parameters used in simulation.

Parameters	Sizes
Oxide thickness	100 nm
Polysilicon thickness	300 nm
Monosilicon thickness	1 µm
Doping of monosilicon	$N_{DA}=10^{17}$ cm^{-3}
Doping of polysilicon	$N_{DP}=10^{17}$ cm^{-3}
Band gap energy E_G	1.12 eV

The Fig. 3 shows the effect of interface states densities at monosilicon/SiO_2 on C (V) characteristics. We have considered the surface state charges at the monosilicon-oxide interfaces, $N_{TS}= 10^{12}$ cm^{-2}.

Fig. 4 shows the result of the simulation with an interface state density of 10^{12} cm^{-2} introduced at the polysilicon/oxide interface.

The shape of curves C (V) is extremely dependent on interface states to the interfaces SiO_2 / Si-poly and SiO_2 / Si-mono.

The interface states charges density causes a distortion and a translation toward positive voltage of the C_T (V) curve. To obtain the same desertion region that the one of the curve with $N_{TS}= 0$ corresponding curve, it is necessary to applied a strong bias voltage. The working of the component is degraded.

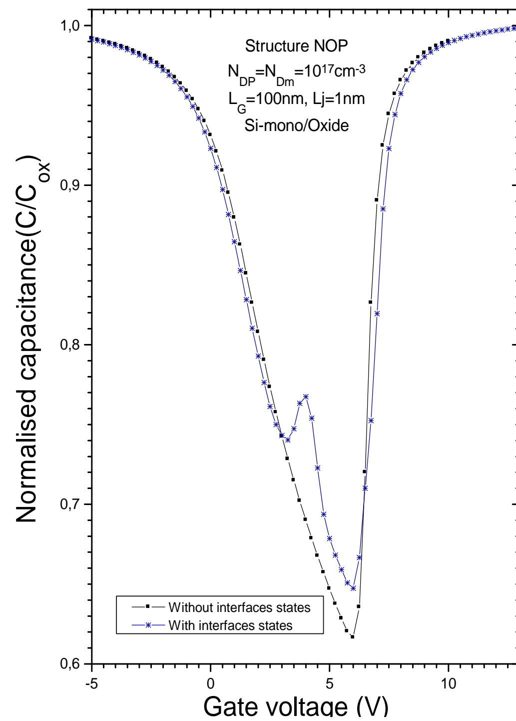

Fig. 3. Interface states at monosilicon/SiO_2 effect on Quasi-static capacitance.

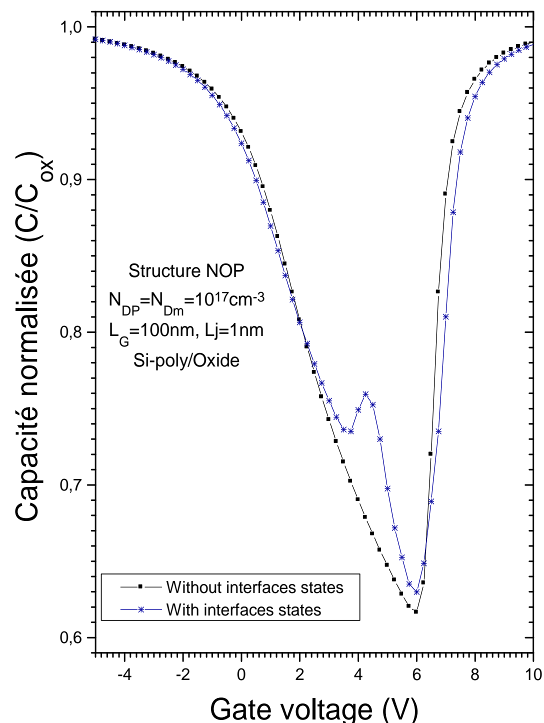

Fig. 4. Interface states at polysilicon/SiO_2 effect on Quasi-static capacitance.

The peaks correspond to the interface states density at the monosilicon/oxide and polysilicon/oxide interfaces appears in positive voltage. In this case, polysilicon and monosilicon layers are depleted or inverted. The second peak depth is lower for the state of interface Si-mono/SiO_2 If the Polysilicon doping concentration is 10^{19} cm^{-3} the effect of the interface states disappears. What is confirmed by Fig. 5. In this case the density of traps is neglected compared to the polysilicon doping concentration.

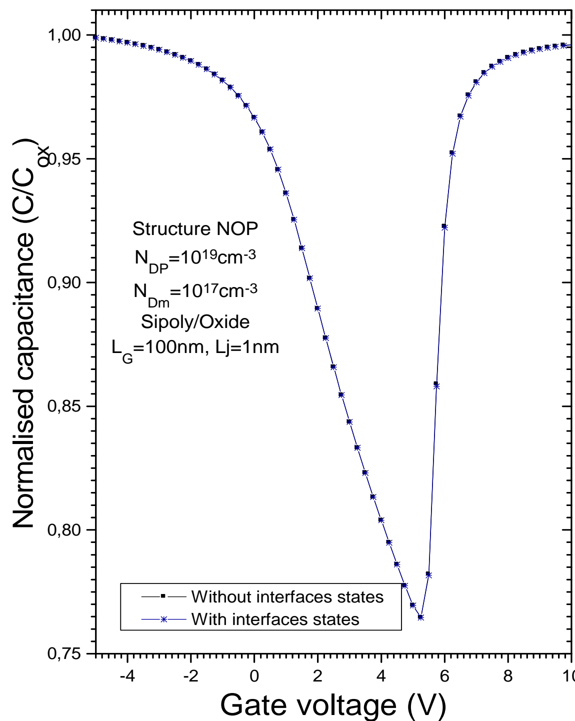

Fig. 5. Interface states at polysilicon/SiO_2 effect on Quasi-static capacitance for Polysilicon doping= 10^{19} cm^{-3}.

Our results are in a good agreement with the results given by C. Leveugle on capacitances polysilicon/SiO_2 / monosilicon [6].

In the case if the silicon substrate is N doped. The peaks correspond to the interface states density at the monosilicon/oxide and polysilicon/oxide interfaces appears in negative and positive voltage respectively (Figs. 6, 7). What confirms that when V_G<0, the polysilicon region is accumulated and the monosilicon region is depleted or inverted. In the same way when, at V_G>0, the monosilicon substrate can be accumulated and the polysilicon region is depleted or inverted. The traps states density at the interfaces SiO_2/polysilicon and SiO_2/polysilicon values decrease when the samples are annealed. The quality of structure MS^{P}OS will be improved. These results are obtained in our work study on the MS^{P}OS capacitance [7].

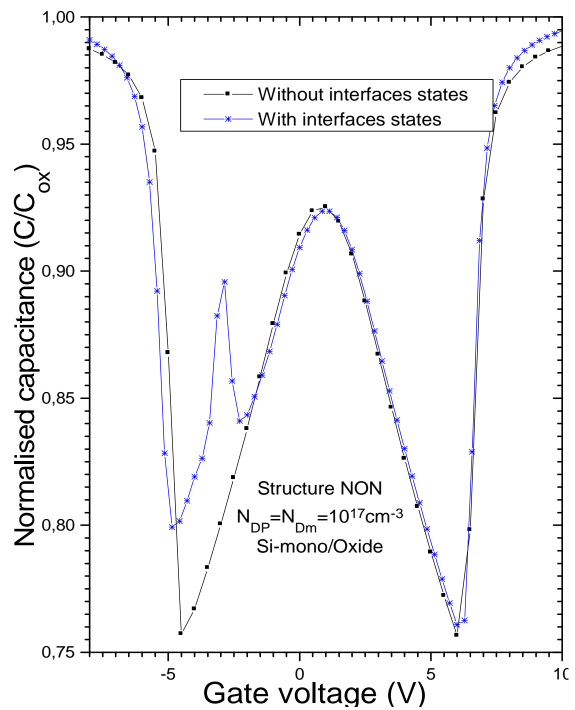

Fig. 6. Interface states at monosilicon/SiO_2 effect on Quasi-static capacitance for N doped type substrate.

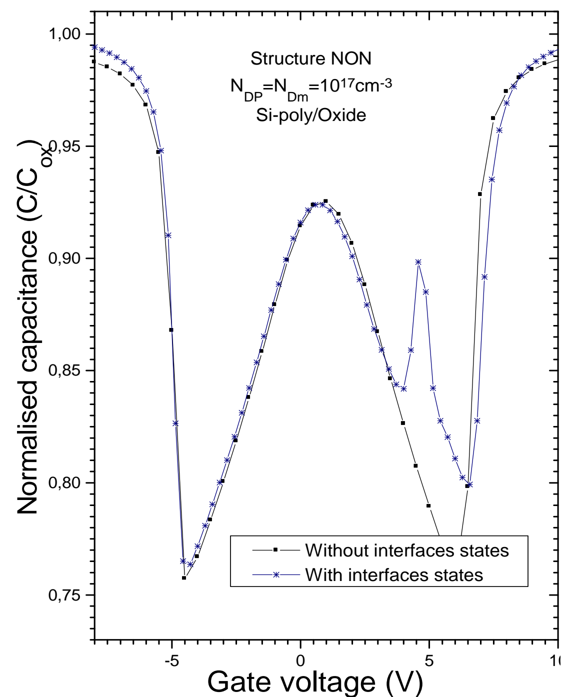

Fig. 7. Interface states at polysilicon/SiO_2 effect on Quasi-static capacitance for N doped type substrate.

6. Conclusions

The C (V) characteristics are presented in this work, the effect of the interface states is analyzed. The peaks correspond to the interface states density at the monosilicon/oxide and polysilicon/oxide interfaces appears in positive voltage. What confirms

that when VG>0, the polysilicon and the monosilicon regions are depleted or inverted. The interface states translate the C_T (V) curve and cause the increase of the minimum value of capacitance. The effect of interface states on C (V) curves is neglected for the polysilicon doping concentration in order to 10^{19} cm^{-3}. The simulated curves can be exploited in order to compare them with the experimental curves realized on the MS^POS structures. This comparison allows the determination of the interface state density.

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