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Electrical Characteristics and Sensitivity Performance Analysis from Planar MOSFETs to FinFETs in III-V Semiconductor Technology

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Abstract. With rapidly approaching limits of scale for silicon planar MOSFETs, new device designs have begun to appear as replacements for the present planar technology. The potential new device designs include Double Gate (DG) FETs, FinFETs, Tri-Gate FETs, and Omega-Gate FETs. The motivation for moving from a single-gate MOSFET to the gate-all-around transistor has been the minimisation of short-channel effects and more efficient transfer characteristics through a more intimate control of the conduction channel. However, in the drive for minimisation, along with short- channel effects, another major challenge for the process engineer has been the issue of variability. While the effect of increased gate control and variability has been studied exhaustively, there has been relatively less focus on the effect on variability as we move from a 1-D to a 3-D gate architecture. This paper aims to explore the impact of gate architecture on parametric sensitivity. A comparative analysis of performance parameters such as threshold voltage, sub-threshold slope, I_{ON}/I_{OFF} ratio, and ON current across different structural parameters, including gate length, oxide thickness, and dielectric materials, is conducted in this proposed work.

Keyword: Planar MOSFET, JLT, TG-FinFET, DIBL, Subthreshold swing, Switching ratio.

1. Introduction

Silicon has dominated semiconductor fabrication for decades. Silicon devices' scalability, availability, and oxide properties are key. Due to their near-attainable upper theoretical limit of operation, Si-based devices cannot meet future RF and microwave performance demands. The continuous drive for minimalism faces two bottlenecks: process-induced variability due to minor structural parameter fluctuations and an almost exponential increase in power density due to the quest for more transistors per IC chip. Nano-scale devices also have short-channel effects and leakage. Device engineers have tried many gate topologies to regulate the conduction channel and prevent short channel effects, but Si-Ge and GaN are fascinating.

Different GaN gate designs influence variability, this study finds. III-V FinFET subthreshold drain current is calculated using the analytical model [1-4]. This work investigates the DIBL effect [5], leakage current [6], subthreshold slope [7], and switching ratio for model improvement.

2. Materials and Methods

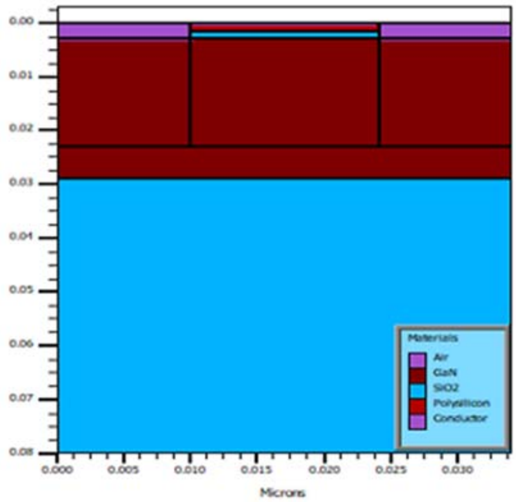
2.1. Beyond Silicon-GaN as a Substrate Material

Silicon (Si) is the chosen electronic semiconductor material due to its well-established technology and distinctive native oxide. Si electrical devices typically have a 150 °C junction temperature limit. Si chips and power devices must not exceed this temperature. Modern devices cannot use Si due to its low charge transfer and maximum velocity. The pursuit of smaller components has enhanced the power density of semiconductor circuits during the past decade. Device mean operational temperatures have increased due to short-channel effects, tunnelling-induced leakage current, high-frequency switching, and smaller device surface areas. High-bandgap alloys might replace silicon. Thus, device scientists target novel materials like SiGe, SiC, and group III–V semiconductors. Group III nitride semiconductors, especially gallium nitride (GaN) and associated alloys, have drawn attention for their unique properties for 20 years. GaN offers enormous potential in optoelectronic and high-power device development. GaN has a breakdown field strength of 20 MV/cm [8], stronger than GaAs (4 MV/cm) and Si (3 MV/cm). Additionally, its electron velocity is 3×107 cm/s [9], exceeding GaAs and Si (2×107 cm/s). The military and commercial application of GaN technology is due to its enhanced electron transport [10-12]. At 14 nm, high-k dielectric [13-18] replaces SiO_2 to limit short channel effects.

2.2. Evolution of a Gate Structure

Channel management becomes crucial in DSM. Because of strong short-channel effects, the International Technology Roadmap for Semiconductors (ITRS) recommends using multi-gate transistors for sizes larger than 32 nm to meet strict leakage standards. Scaling standard MOS transistor channel length below 30 nm causes acute source/drain junction issues. To prevent impurities from moving from source to drain to channel, doping concentrations must vary by many orders of magnitude within nanometres. A second ultra-thin layer with high dopant concentration in the "junction-less (JLT) transistor" [19-22] solves the problem. No source-drain connections or doping concentration fluctuations occur in this layer. Channel-end gates govern conduction status. Not having enough S/D depletion charge spread out in the channel area leads to short-channel effects like DIBL and a worsening subthreshold slope in junctionless transistors (JLTs). Gate capacitance alone does not drive current; doping concentration does [21-23]. Zero doping gradient prevents source-to-drain diffusion. The junction-less device helps maintain better mobility by using bulk conduction instead of relying on conduction through the surface, which can be affected by surface scattering from high-k dielectrics. FinFET transistors might be utilised for ULSI below 20 nm. Effectively expanding inversion layer gates improves channel control. FinFETs outperform CMOS due to their high transconductance, low subthreshold swing, and gate-spanning channel to reduce SCE [24]. FinFETs can serve as switching power supplies, amplifiers, frequency converters, and miniaturised electronics and sensors due to their low energy consumption [25-29].

Medical surgical equipment uses switching generators and modulators for ultrasonic and high-frequency tissue welding. Fix drain current collapses and other reliability issues to boost device efficiency. This study's 1D to 3D gate architecture simulated device architectures are illustrated in Fig. 1(a), (b), and (c).



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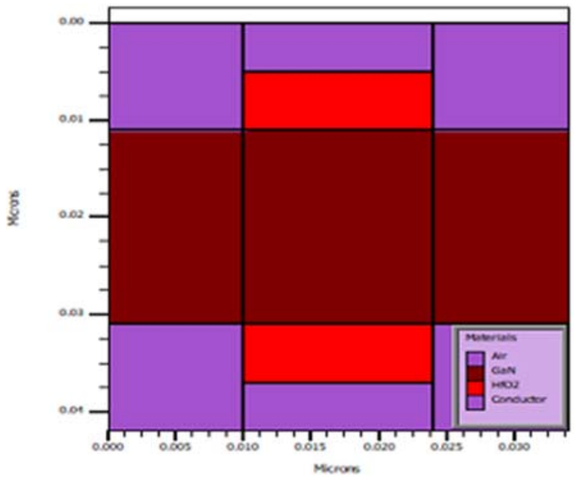

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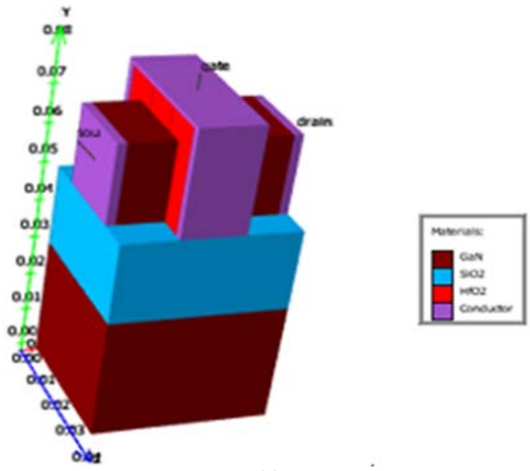


(c)

Fig. 1. Construction of (a) Planer MOSFET (b) JLT (c) TG-FinFET structure using Silvaco TCAD.

2.3. Simulation Method

The simulations for this study were conducted only using ATLAS SILVACO TCAD, which supports both 2D and 3D simulations. Table 1 presents the fundamental characteristics of this n-channel TG FinFET structure.

Table 1. Basic parameters used for all above said gate architecture.

Device Parameter	Value	Unit
L	14	nm
W	20	nm
Source/drain height	20	nm
Source/drain width	20	nm
Channel Doping	1×10^{15} (p-type)	Atoms/cc
T_{BOX}	50	Nm
T_{sub}	30	Nm
T_{OX}	2	Nm

This calculation uses 4.6 electron volts for the gate electrode's work function. The Gummel-Newton method solves it. Fermi statistics replaced Boltzmann statistics in severely doped locations with low carrier concentrations.

This work examines how heating and generation-recombination affect energy transfer between carriers and the lattice environment at high temperatures. The Shockley-Read-Hall (SRH) model predicts heat-induced leakage and recombination. Auger generates high-current density recombination and high-level injection effects. Inter-carrier interactions reduce Auger recombination as carrier concentrations rise. Studies show heavily doped MOSFETs act like bipolar transistors. Doping has an impact on both the pn product and bandgap narrowing. Bandgap narrowing. The quantum mechanics-based HANSCHQM model confines MOSFET carriers at the gate oxide contact.

3. Results and Discussion

This section provides a detailed analysis and discussion of the simulated results for GaN-based single-gate MOSFET, double-gate MOSFET (JLT), and TG-FinFET. The analysis focuses on the effects of temperature, oxide thickness, channel doping, oxide material, and changes in threshold voltage, DIBL, and SS.

In this work, at first performance of the GaN-based TG-FinFET device with Al_2O_3 as the gate dielectric is compared with a single fin FinFET (AlGaN/GaN) device with Al_2O_3 as the gate dielectric as reported by Ki-Sik IM et al. (2014) [30] at 300 K. Fig. 2 shows the comparison of I_D-V_G for $V_D = 0.1$ volt and clearly shows in Table 2 that GaN-based TG-FinFET has produced greater on-current and lower threshold voltage.

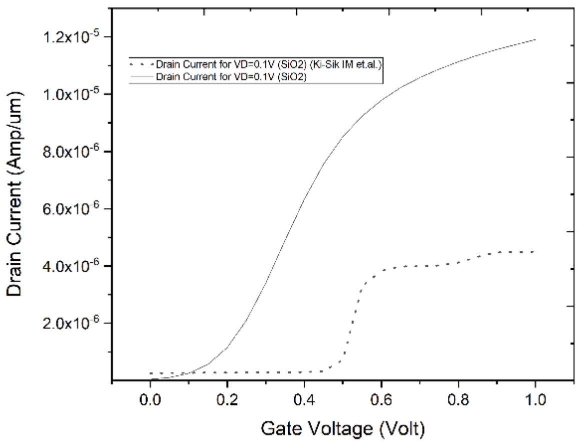


Fig. 2. Comparison of ID-VG curve for different channel material.

Table 2. Comparison of electrical characteristics.

Parameter	KI-SIK IM et al. (2014)	Our work
V_{th} (Volt)	0.465	0.109
I_{ON} (Amp/um)	4.25×10^{-6}	1.28×10^{-5}
I_{OFF} (Amp/um)	2.55×10^{-7}	4.28×10^{-8}

3.1. Temperature Variation

Table 3 shows how gate architecture affects parametric sensitivity by comparing performance parameters [31] like threshold voltage, subthreshold slope, and I_{ON}/I_{OFF} ratio due to temperature variations with HfO_2 as the gate dielectric.

Subthreshold drain current determined by the equation (1)

$$I_{D_{Sub}} = \frac{W}{L}\mu_{effec}C_{OX}\left[(V_{GS}-V_t)V_{DS} - -\frac{V_{DS}^2}{2}\right] \quad (1)$$

When, $V_{GS} > V_t$, where W and L are channel width and length, V_{GS} is the Gate to Source voltage, V_t is a threshold voltage, V_{DS} is the Drain to Source voltage, C_{OX} is the Oxide capacitance.

In this study, temperature fluctuation for three JLT, planer MOSFET, and TG-FinFET models with the same oxide material (HfO_2) was compared for transfer characteristics.

Figs. 3 and 4 show the comparison. According to the study, gate control decreases drive current, but dual-gate design approaches MOSFET at higher temperatures. As 1D to 3D Gate control improves, switching characteristics do too.

The change in threshold voltage (V_t) is also examined as the temperature increases and displayed in Fig. 5. From the plot in the proposed model of the TG-FinFET reveals the change of the threshold voltage is low which in turn became very much advantageous in varied environmental circumstances.

A relative study based on the change in % of device parameters with the variation of temperature is shown in Fig. 6 and it can be surmised that one can obtain the best device parameters from the proposal TG-FinFET model with H_fO_2 as oxide material compared to the other models.

Table 3. Effects in performance parameters due to temperature variation.

Variable	Device	V_t	I_{DSmax}	$I_{leakage}$	SubVt
T = 300	MOSFET (Single Gate)	2.369	2.29E-6	5.47e-09	0.391741
	JLT (Double Gate)	0.436	3.11E-6	2.83E-9	0.067951
	TG-FinFET	0.109	3.21E-6	4.186E-9	0.0893
T = 400	MOSFET (Single Gate)	2.308	1.92E-6	4.04e-08	0.48022
	JLT (Double Gate)	0.420	9.45e-14	4.20e-17	0.14827
	TG-FinFET	0.081	6.33e-07	2.24e-09	0.089612
T = 500	MOSFET (Single Gate)	2.218	1.55E-6	1.56e-07	0.573089
	JLT (Double Gate)	0.404	4.97e-12	1.0e-14	0.184363
	TG-FinFET	-0.024	9.10e-07	6.42e-08	0.159687
T = 600	MOSFET (Single Gate)	2.137	1.08E-6	1.91E-8	0.66696
	JLT (Double Gate)	0.388	4.33E-6	2.29E-7	0.221868
	TG-FinFET	-0.103	6.41E-7	1.10E-7	0.228701

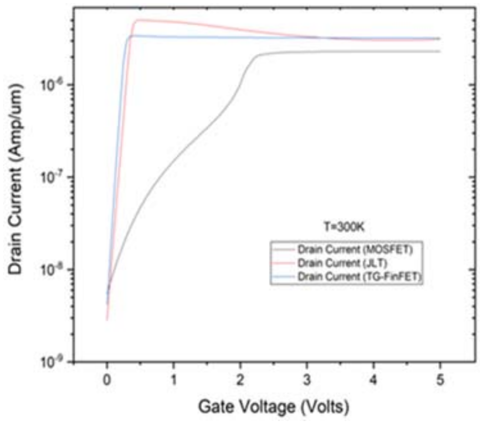


Fig. 3. Drain current variation for different gate architectures at T = 300 K.

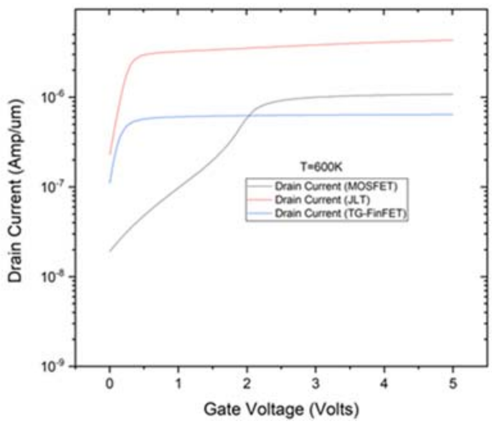


Fig. 4. Drain current variation for different gate architectures at T = 600 K.

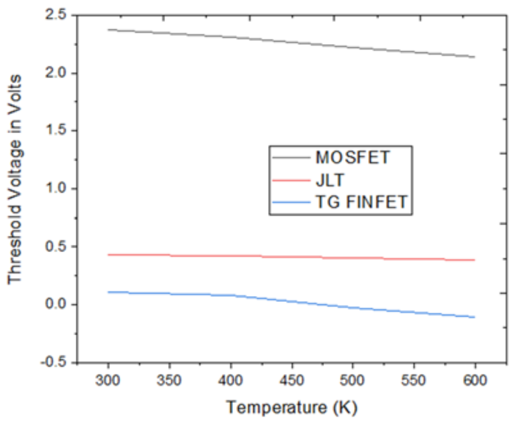


Fig. 5. Threshold voltage variation with temperature.

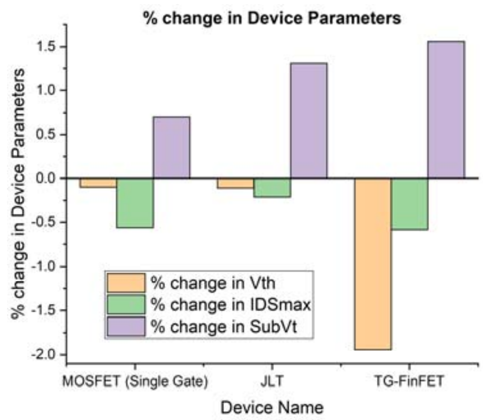
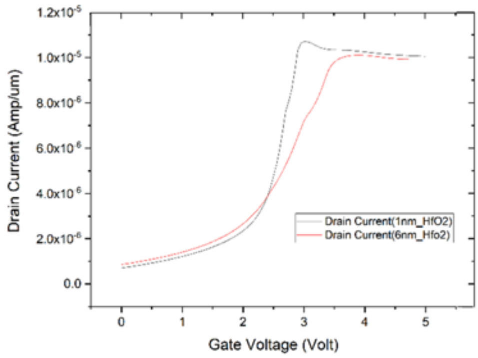


Fig. 6. Percentage change in device parameters with temperature variation.

3.2. Oxide Thickness Variation

Figs. 7a, 7b, and 7c illustrate planar MOSFET, JLT, and TG-FinFET transfer characteristics for different HfO□ thicknesses. Increased oxide thickness reduces tri-gate FinFET drain current. As capacitance between the gate and channel increases, the gate loses its ability to regulate and modulate current. Gate terminal voltage controls most FinFET drain current. Gate voltage influences channel conductance and drain current via an electric field. Oxide thickness increases gate-channel capacitance. Due to increased capacitance, the gate struggles to manage channel conductivity and drain current.

Junctionless transistors' drain current rises with oxide thickness. As oxide thickness increases, tri-gate FinFET drain current decreases. Oxide thickness boosts JLT gate-channel capacitance. Capacitance improves electrostatic channel control and gate-channel coupling. Gate voltage increases channel conductance and drain current via the electric field.



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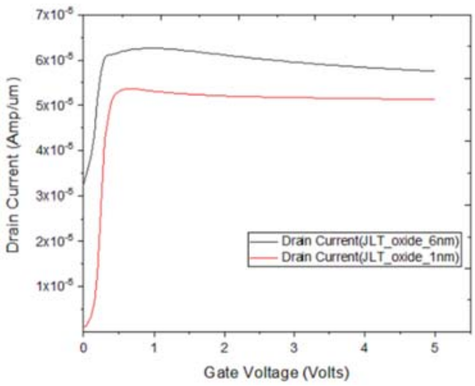

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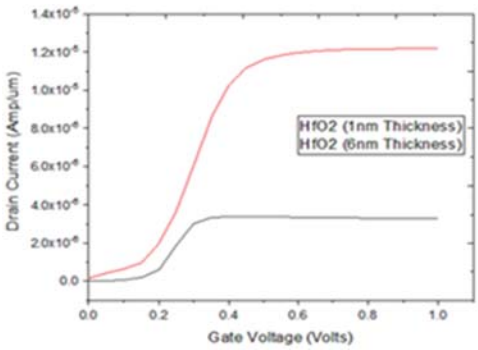


(c)

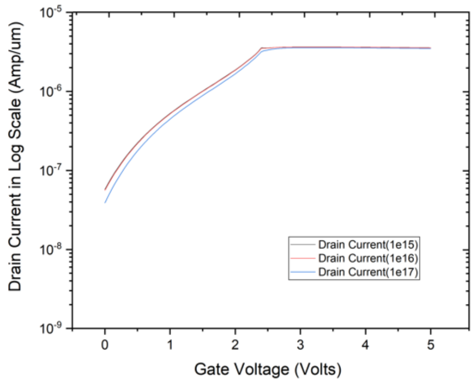
Fig. 7. Transfer characteristics of (a) 1D MOSFET (b) JLT (c) TG-FinFET for tox variation.

3.3. Variation in Channel Doping

Figs. 8a, 8b, and 8c show channel doping variation for three proposed models in transfer characteristics. MOSFET, JLT, and TG-FinFET channel doping greatly affects their electrical performance.

MOSFET channel doping affects key parameters. Channel doping concentration impacts MOSFET threshold voltage. Increasing doping concentrations lowers the threshold voltage, making device activation easier. Reduced doping concentrations raise the threshold voltage and make device activation harder.

The subthreshold slope is a measure of how steeply the MOSFET current changes to the gate voltage. Lower doping concentrations can lead to improved subthreshold slope, resulting in better transistor performance and lower power consumption.



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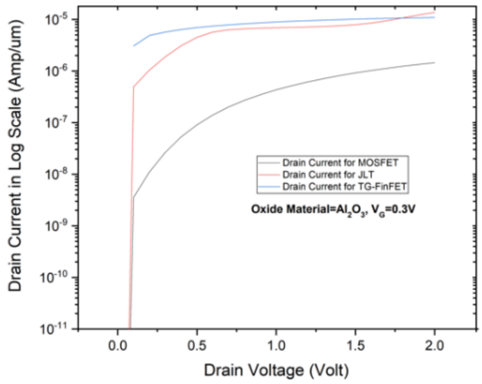

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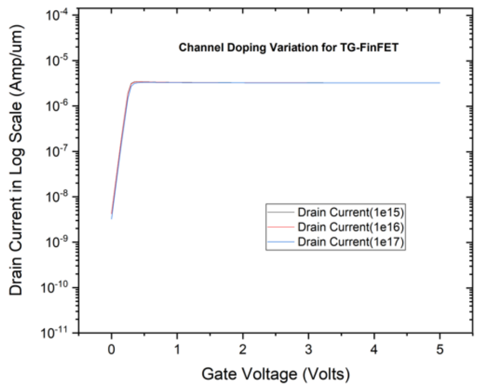


(c)

Fig. 8. Transfer characteristics of (a) MOSFET (b) JLT (c) TG-FinFET for channel doping variation.

Due to its 3D gate control, the TG FinFET has a better subthreshold slope and channel control than standard planar MOSFETs. Conventional planar MOSFETs struggle to grow to smaller technical nodes without increasing leakage current.

This respective study concludes that TG-FinFET has superior transfer properties compared to standard MOSFET and JLT. This advantage is seen in Fig. 8c, where it is noted that the threshold voltage of TG FinFET nearly stays constant despite variations in channel doping.

Fig. 9 plots the ratio of ION to IOFF for three suggested models at different temperatures with a constant drain voltage (VD) of 0.1V. The figure above shows three devices' I_{ON}/I_{OFF} ratio temperature fluctuations. The figure illustrates that TG FinFET is less susceptible to temperature than Planar MOSFET and JLT because its ION/IOFF ratio lowers more gradually with rising temperature. The TG FinFET has less temperature-related performance degradation, making it a viable choice for high-power density devices.

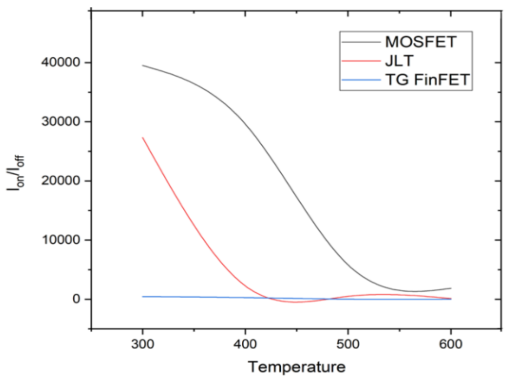


Fig. 9. Variation in ION/ IOFF ratio with temperature for different device.

3.4. Dielectric Material Variation

The relationship between drain current and drain voltage is graphed in Figs. 10a, 10b, and 10c. The comparison is made among three different models with varying dielectric materials with a gate voltage of 0.3 volts.

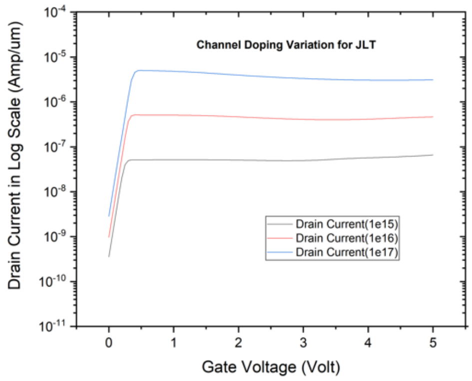
From the comparison, one can conclude that TG-FinFET is showing higher current compared to other models except the model with SiO_2 as a dielectric and the proposed model of TG-FinFET produces the lowest threshold voltage compared to other models.

The proposed JLT model shows higher current for each type of dielectric material, while the TG-FinFET has the lowest threshold voltage when compared to the JLT and planar MOSFET. The nano regime favours the TG-FinFET model. Figs. 11A, 11B, and 11C show the ID-VG characteristics for SiO□, Al□O□, and HfO□ dielectric materials with a drain voltage of 0.1 volts.

Fig. 12 assists in calculating the Drain-Induced Barrier Lowering (DIBL) factor for gate oxide materials such as SiO_2, Al_2O_3, and HfO_2. The lowest Drain-Induced Barrier Lowering (DIBL) material performs best. The lowest Drain-Induced Barrier Lowering (DIBL) values are obtained with a larger gate dielectric. GaN-based TG-FinFET has the lowest DIBL of the three devices. To calculate drain-induced barrier lowering (DIBL), use this equation:

$$\mathrm{DIBL}\left(\mathrm{mV}/_{\mathrm{V}}\right) = \frac{V_{t1_{VD1}} - V_{t2_{VD2}}}{V_{D_2} - V_{D_1}}, \qquad (2)$$

where $V_{D_2} = V_{D_1}$ is a drain voltage, $V_{t1_{VD_1}}$ is a threshold voltage at V_{D_1}, $V_{t2_{VD_2}}$ is a threshold voltage at V_{D_2}.



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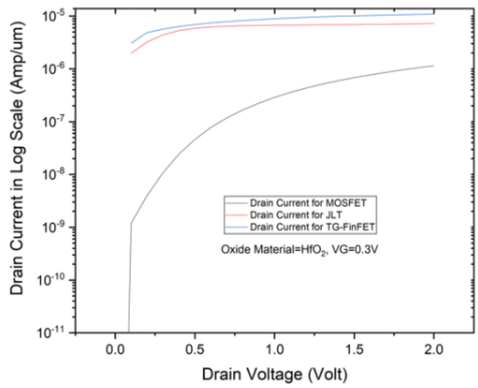

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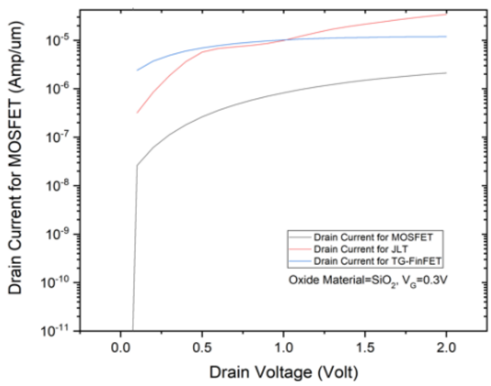


(c)

Fig. 10. ID-VD (a) Al2O3 as oxide material (b) HfO_2 as oxide material (c) SiO_2 as oxide material for VG = 0.3 V.

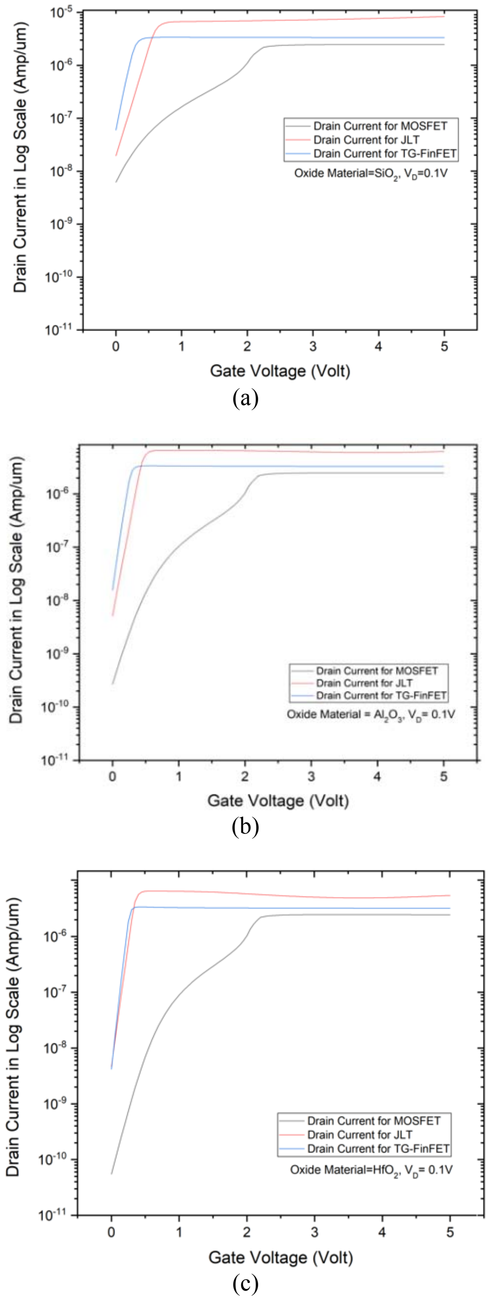


Fig. 11. Variation of drain current for (a) SiO_2 (b) Al_2O_3 (c) HfO_2 as oxide material for VD = 0.1 V.

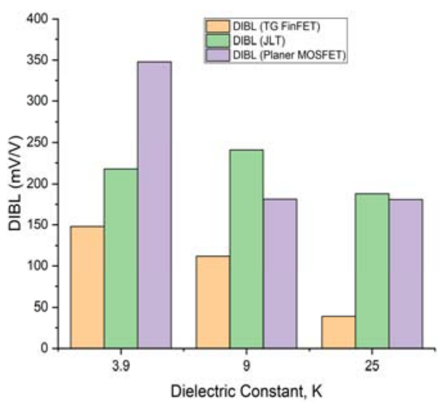


Fig. 12. Variation of DIBL w.r.t dielectric constant for TG-FinFET, JLT and Planer MOSFET.

Fig. 13a, 13b& 13c depict a plot of the ratio between the on current and off current with different dielectric materials for JLT, Planar MOSFET and TG-FinFET. All three diagrams indicate the ratio of Ion to I_{off} increases exponentially as the k value increases. This is because the off currents fall significantly as the k value increases, as shown in Fig. 14a, 14b and 14c. A high ratio is necessary for the efficient switching of the devices.

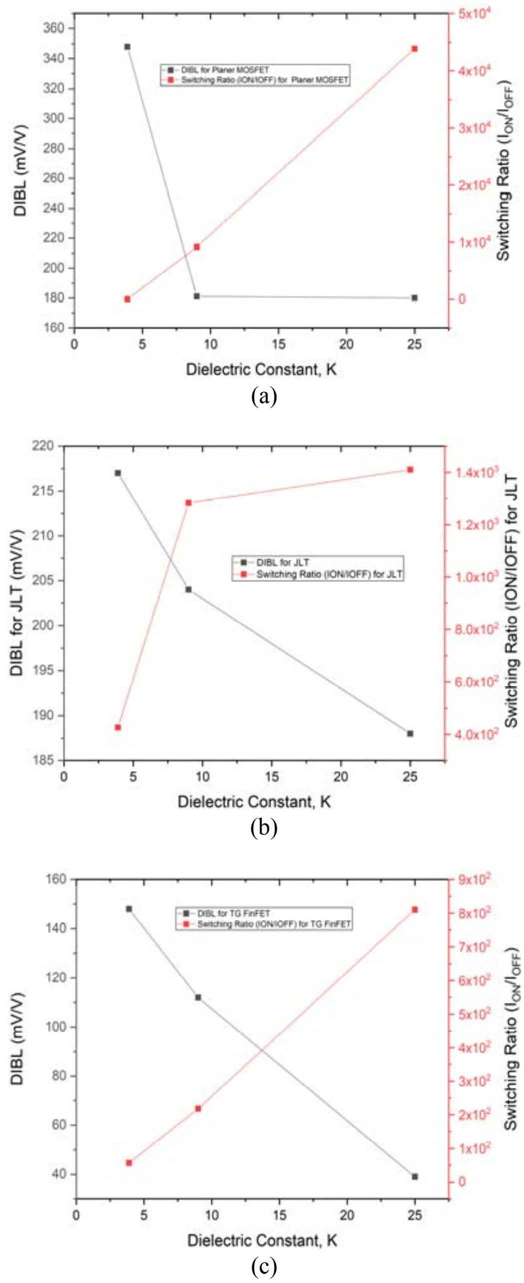
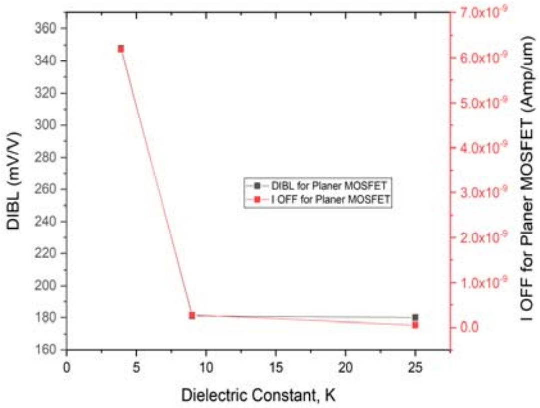


Fig. 13. DIBL & Switching ratio variation for (a) JLT (b) MOSFET (c)TG-FinFET.

Equation (3) used for the calculation of leakage current (I_{OFF})

$$I_{OFF}(amp/\mu m) = 100\, W/L\, 10^{\frac{-Vth}{SS}} \quad (3)$$

The variables V_{th} and SS denote the threshold voltage and subthreshold swing, respectively, which are fundamental parameters crucial for evaluating transistor performance and power efficiency in advanced semiconductor devices. TG-FinFET exhibits enhanced electrostatic regulation and fewer short-channel phenomena in comparison with conventional MOSFETs. The presence of a three-dimensional fin structure in TG-FinFET enhances the ability to regulate the gate across the channel, resulting in enhanced switching performance.



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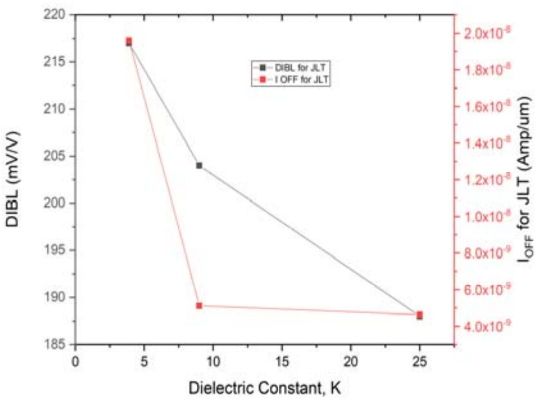

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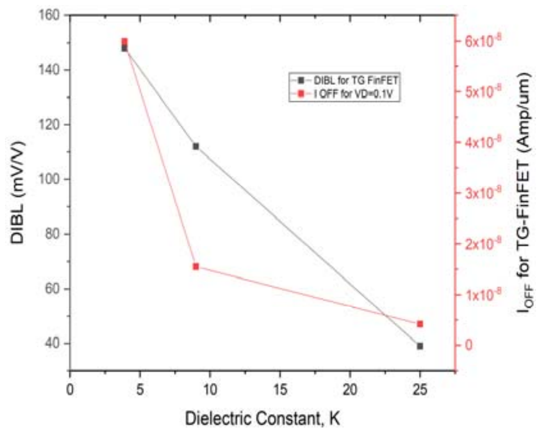

(c)

Fig. 14. DIBL & IOFF variation with K for (a) MOSFET(b) JLT (c) TG-FinFET.

The variation of *subthreshold swing* is studied with the increment of dielectric constant and plotted in Fig. 15. In this plot of subthreshold swing versus dielectric constant, the general trend is that a higher dielectric constant leads to a lower subthreshold swing. This is desirable because a lower subthreshold swing indicates better control over the transistor in the subthreshold region, resulting in lower power consumption and improved energy efficiency. So, it is clear that TG-FinFET produces a lower subthreshold swing compared to the other two devices. The calculation of *subthreshold swing* (*SS*) derived from equation (4)

$$\text{Subthreshold swing (SS)}\left(\frac{\text{mV}}{\text{decade}}\right) = \frac{\delta V_G}{\delta(\log_{10} I_D)}, \tag{4}$$

where δV_G is a shift in gate voltage, $\delta(\log_{10} I_D)$ is a shift in logarithmic drain current.

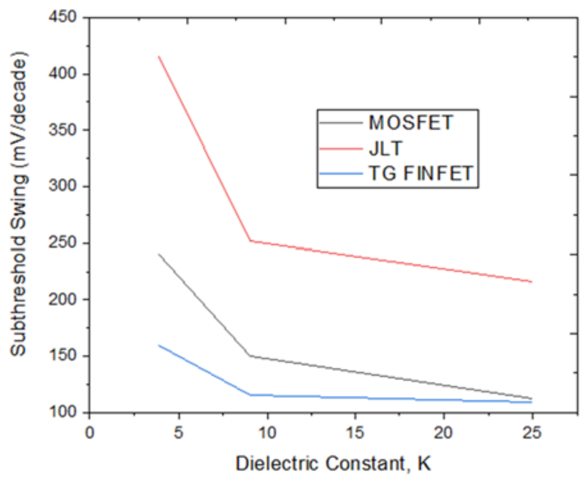

Fig. 15. SS variation with K for Planer MOSFET, JLT & TG-FinFET.

Therefore, it has been determined that TG-FinFET is the most optimal device in comparison to single-gate and double-gate design devices, with HfO□ being the superior high-K dielectric material for replacing SiO□ to control short channel effects at channel lengths of 14 nm. To emphasise this aspect, the performance of the GaN-based tri-gate FinFET with HfO_2 as the gate dielectric is compared with that of a recent tri-gate SOI FinFET device that also uses HfO_2. Renthlei and colleagues developed this device. The comparison of the two devices is now presented in Table 4, which may be seen here. When compared to SOI FinFET, the GaN-based TG-FinFET structure exhibits a somewhat higher current. Additionally, the GaN-based TG-FinFET is observed to have a lower threshold voltage. Moreover, the SCEs are exercising a high level of control over this work.

Table 4. Electrical characteristics comparison of tri-gate FinFET at 14 nm channel length.

Parameter	Renthlei et al. (2021)	This work
V_{th} (volt)	0.293	0.109
I_{on} (Amp/μm)	1.5×10^{-6}	1.65×10^{-6}
SS (mV/decade)	67	150
DIBL (mV/V)	40	38

4. Conclusion

The objective of this study is to examine parametric sensitivity to structural parameters of field-effect transistors – from planar MOSFET to FinFET. Moreover, the temperature sensitivity of TG FinFET is much lower than that of the planar MOSFET and JLT, indicating its suitability for high-power density devices. From the simulation results, it's clear that making the oxide thicker usually reduces the drain current because it increases the capacitance between the gate and the channel, which affects the current flow of the TG FinFET. Therefore, a higher gate voltage must be used to boost the drain current. Therefore, we need to apply a higher gate voltage to boost the drain current. This is in contrast to JLT, where the drain current increases as the oxide thickness increases, a feature that should not be desired in a device. Therefore, the TG FinFET exhibits significant gate-controlling abilities. Also, GaN-based FinFETs are much less affected by temperature changes than the other two devices, making them suitable for high-power density uses. The most important finding of this study is that the threshold voltage of FinFET is much more sensitive to changes in the dielectric than other devices. This study holds promising potential for application as a biosensor.

References

[1]. K.-S. Im, H.-S. Kang, J.-H. Lee, S.-J. Chang, et al., Characteristics of GaN and AlGaN/GaN FinFETs, *Solid-State Electronics*, Vol. 101, 2014, pp. 2-5.

[2]. X. Liang, Y. Taur, A 2-D analytical solution for SCEs in DG MOSFETs, *IEEE Transactions on Electron Devices*, Vol. 51, Issue 9, 2004, pp. 1385-1391.

[3]. S. E. Huang, C. L. Yu, P. Su, Investigation of fin-width sensitivity of threshold voltage for InGaAs and Si negative capacitance FinFETs considering quantum-confinement effect, *IEEE Transactions on Electron Devices*, Vol. 66, Issue 6, 2019, pp. 2538-2543.

[4]. D. K. Schroder, Semiconductor Material and Device Characterization, 3rd Ed., *John Wiley & Sons*, 2015.

[5]. A. Saha, R. S. Dhar, S. Ghosal, A comparative study of GaN and Si-based SOI FinFET, in Tropical Drifts in Intelligent Computing, *Springer Nature*, 2022, pp. 369-379.

[6]. S. D. D. Santos, J. A. Martino, E. Simoen, C. Claeys, Impact of selective epitaxial growth and uniaxial/biaxial strain on DIBL effect using triple gate FinFETs, *Journal of Integrated Circuits and Systems*, Vol. 5, Issue 2, 2010, pp. 154-159.

[7]. S. K. Mohapatra, K. P. Pradhan, P. K. Sahu, Some device design considerations to enhance the performance of DG-MOSFETs, *Transactions on Electrical and Electronic Materials*, Vol. 14, Issue 6, 2013, pp. 291-294.

[8]. Z. Wang, L. Liu, P. Qi, J. Chen, High-breakdown-voltage GaN-based vertical FinFET, *Journal of Power Electronics*, Vol. 24, Issue 1, 2024, pp. 1-8.

[9]. T. Tanaka, K. Takano, T. Mishima, Y. Kohji, et al., GaN epitaxial wafers for high breakdown voltage RF transistor applications, *Hitachi Cable Review*, Vol. 24, 2005, pp. 11-14.

[10]. P. Gangwani, S. Pandey, S. Haldar, M. Gupta, et al., Polarization dependent analysis of AlGaN/GaN HEMT for high power applications, *Solid-State Electronics*, Vol. 51, Issue 1, 2007, pp. 130-135.

[11]. R. S. Pengelly, S. M. Wood, J. W. Milligan, et al., A review of GaN on SiC high electron-mobility power transistors and MMICs, *IEEE Transactions on Microwave Theory and Techniques*, Vol. 60, Issue 6, 2012, pp. 1764-1776.

[12]. P. B. Klein, S. C. Binari, K. Ikossi-Anastasiou, et al., Investigation of traps producing current collapse in AlGaN/GaN high electron mobility transistors, *Electronics Letters*, Vol. 37, Issue 10, 2001, pp. 661-662.

[13]. G. Meneghesso, G. Verzellesi, R. Pierobon, et al., Surface-related drain current dispersion effects in AlGaN-GaN HEMTs, *IEEE Transactions on Electron Devices*, Vol. 51, Issue 10, 2004, pp. 1554-1561.

[14]. K. S. Dubey, A. Islam, Effect of high-k dielectric HfO2 on performance of AlGaN/GaN based MOSHEMT for RF applications, *Microsystem Technologies*, Vol. 30, Issue 5, 2024, pp. 835-842.

[15]. S. Sharma, V. Nath, S. S. Deswal, R. S. Gupta, Analytical modelling, simulation, and characterization of temperature-dependent GaN-HK-SBNWFET for high-frequency application, *Microelectronics Journal*, Vol. 137, 2023, 105797.

[16]. Y. Zhang, A. Zubair, Z. Liu, M. Xiao, GaN FinFETs and trigate devices for power and RF applications: review and perspective, *Semiconductor Science and Technology*, Vol. 36, Issue 5, 2021, 054001.

[17]. M. Verma, A. Nandi, GaN based trigate HEMT with AlGaN back-barrier layer: proposal and investigation, *Semiconductor Science and Technology*, Vol. 37, Issue 6, 2022, 065004.

[18]. A. Kumar, A. K. Goyal, Temperature-dependent analysis of heterojunction-free GaN FinFET through optimization of controlling gate parameters and dielectric materials, *International Journal of Materials Research*, Vol. 114, Issues 7-8, 2023, pp. 732-737.

[19]. M. Karbalaei, D. Dideban, H. Heidari, Impact of high-k dielectric with different angles of coverage on the electrical characteristics of gate-all-around field effect transistor: a simulation study, *Results in Physics*, Vol. 15, 2019, 102823.

[20]. S. Ghosal, A. Sikdar, D. Ghosh, A study of the effect of composite dielectric on the switching behaviour of junction less transistor, *JCSE International Journal of Computer Science and Engineering*, Vol. 7, Special Issue 18, 2019.

[21]. S. Ghosal, M. Ganguly, D. Ghosh, A study on sensitivity of some switching parameters of JLT to structural parameters, *Nanoscience & Nanotechnology-Asia*, Vol. 10, Issue 4, 2020, pp. 491-496.

[22]. S. Nanda, S. Kumari, R. S. Dhar, Exploration and analysis of a n-FinFET implementing stacked high-K at 08 nm gate length, *Sādhanā*, Vol. 49, Issue 2, 2024, 72.

[23]. S. J. P. Bantupalli, A. Arunapriya, R. Hariprasad, Modelling of multigate MOSFET short channel structure for low power application, *Journal of Physics: Conference Series*, Vol. 1964, 2021, 062017.

[24]. S. Huang, W. You, P. Su, Mitigating DIBL and short-channel effects for III-V FinFETs with negative-capacitance effects, *IEEE Journal of the Electron Devices Society*, Vol. 10, 2022, pp. 24-30.

[25]. S. Nanda, R. S. Dhar, Effect of high-k dielectric materials on short channel effects of a 14 nm tri-gate SOI FinFET for reduced area on chip, *Journal of Nano- and Electronic Physics*, Vol. 13, Issue 3, 2021, 03015.

[26]. H. Carrilo-Nunez, M. M. Mirza, D. J. Paul, D. A. Maclaren, et al., Impact of randomly distributed dopants on Ω-gate junctionless silicon nanowire transistors, *IEEE Transactions on Electron Devices*, Vol. 65, Issue 5, 2018, pp. 1872-1879.

[27]. A. Baghi Rahin, V. Baghi Rahin, A low voltage and low power two-stage operational amplifier FinFET transistors, *International Academic Journal of Science and Engineering*, Vol. 3, Issue 4, 2016, pp. 80-95.

[28]. H. V. Nguyen, Y. Kim, 32 nm FinFET based 0.7 to 1.1V digital voltage sensor with 50mV resolution, in *Proceedings of the International Conference on IC Design & Technology (ICICDT'12)*, 2012, pp. 1-4.

[29]. G. Verma, H. Negi, A. K. Saxena, Design and simulation of FinFET based temperature sensor, in *Proceedings of the International Conference on Computing, Communication, and Intelligent Systems (ICCCIS'19)*, 2019, pp. 317-320.

[30]. Y. Hashim, Investigation of FinFET as a temperature nano-sensor based on channel semiconductor type, *IOP Conference Series: Materials Science and Engineering*, Vol. 226, 2017, 012022.

[31]. B. Jeevanrao, D. Rudra, K. Kuleen, B. Arindam, et al., Exploration and analysis of temperature and performance of compound semiconductor-based junctionless GAA FET, *IEEE Access*, Vol. 12, 2024, pp. 61706-61715.

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