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Investigation of Substrate Doping and Thermal Dependence of Gate-induced Drain Leakage in Fully Depleted SOI MOSFETs

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Abstract: Off-state leakage and reliability are greatly impacted by the parasitic bipolar transistor (PBT) effect in fully depleted (FD) silicon-on-insulator (SOI) MOSFETs, which becomes more noticeable with aggressive device scaling. This phenomenon is caused by band-to-band tunneling (BTBT) at the drain-channel junction, which allows excess hole formation when the rising channel potential lowers the energy barrier between the channel and source. A PBT route that increases the gate-induced drain leakage (GIDL) current is triggered by the ensuing hole injection. The interaction between substrate doping concentration and GIDL current amplification in FD SOI MOSFETs is thoroughly examined in this article. Under various substrate doping and back-bias settings, electrostatic potential profiles, carrier generation rates, and leakage current components were examined using two-dimensional TCAD simulations. Additionally, the impact of ambient temperature (300-400 K) on GIDL augmentation and PBT activation was systematically assessed. The findings show that while higher temperatures worsen the impact by raising BTBT production rates, higher substrate doping reduces PBT-induced leakage by decreasing potential modulation in the buried oxide region.

Keywords: Silicon-on-Insulator (SOI), Temperature, Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET), Fully depleted SOI MOSFETs, Parasitic Bipolar Transistor (PBT) effect, Gate-Induced Drain Leakage (GIDL).

1. Introduction

Fully depleted (FD) silicon-on-insulator (SOI) MOSFETs have attracted considerable interest as promising candidates for expanding CMOS technology scaling to the 22 nm technology node and beyond, mainly because of their superior electrostatic integrity and scalability compared to traditional bulk MOSFETs [1–5].Ultra-thin body (UTB) channels combined with high-κ/metal-gate stacks increase subthreshold behavior, efficiently attenuate drain-induced barrier lowering (DIBL), and improve gate controllability [6]. Additionally, the buried oxide (BOX) layer offers dielectric isolation, which reduces parasitic junction capacitances and decreases substrate leakage currents, enhancing switching performance and reducing dynamic power consumption [7]. Furthermore, compared to more complex multi-gate architectures like double-gate, FinFET, and gate-all-around (GAA) transistors, the planar configuration of UTB SOI MOSFETs guarantees improved process compatibility and ease of manufacture [8].

Off-state leakage currents become a major design difficulty when MOSFET channel lengths are decreased to the sub-30 nm region, especially in low-power CMOS applications [9]. Due to its great dependence on electric field strength and electrostatic

coupling effects, gate-induced drain leakage (GIDL) is one of these leakage processes that is particularly concerning in completely depleted (FD) SOI MOSFETs. Band-to-band tunneling (BTBT) at the drain–channel interface is the main cause of GIDL. This process creates extra holes that build up inside the floating body region. A parasitic bipolar transistor (PBT), in which the drain, source, and body function as the collector, emitter, and base of an intrinsic bipolar junction transistor (BJT), is activated by this buildup [10]. This parasitic action's feedback increases the GIDL current, which worsens off-state performance and raises standby power consumption.

The concentration of substrate doping and the applied bias conditions have a significant impact on the interaction between BTBT and PBT processes. The potential barrier between the source and channel is reduced in devices with lightly doped substrates, which makes hole injection easier and improves PBT activation. Higher substrate doping, on the other hand, raises the source-channel barrier, limiting hole feedback and reducing GIDL amplification. Furthermore, the back-gate potential may be effectively controlled through the buried oxide (BOX) layer by providing a substrate bias (V_{sub}), which enables fine-tuning of the front-channel electrostatics and related leakage routes. As a result, back-biasing and substrate doping become crucial design factors for efficient GIDL suppression in cutting-edge SOI MOSFET technologies.

The behavior of GIDL in FD SOI MOSFETs is further complicated by temperature fluctuations. The intrinsic carrier concentration (n_i) grows exponentially with temperature, resulting in increased body charging and hole production, which raises the GIDL current. However, counteracting effects that can partially offset this rise are introduced by temperature-induced bandgap constriction and variations in tunneling likelihood [11, 12]. Therefore, to ensure the thermal stability and dependability of FD SOI-based circuits and to accurately anticipate leakage characteristics under various operating situations, a thorough understanding of thermal impacts is essential.

The distribution of vertical and lateral electric fields at the drain–channel interface is strongly influenced by the gate dielectric material and its stack arrangement, in addition to electrostatic and thermal effects. Because of their high permittivity, high-κ dielectrics like HfO_2 offer better gate controllability and reduced gate leakage; however, the increased electrostatic coupling they cause can intensify local electric fields, amplifying both lateral and transverse BTBT components and raising GIDL [13, 14]. In comparison to non-overlapping structures, this effect is more noticeable in overlapping gate topologies because the drain extension partially reaches beneath the gate edge, adding more vertical field components and increasing tunneling activity.

Comprehensive analyses that simultaneously account for the combined influence of substrate doping, substrate bias, temperature variations, drain voltage scaling, and gate dielectric composition in overlapping and non-overlapping FD SOI configurations are still relatively rare, despite the fact that many studies have examined GIDL and BTBT phenomena in both bulk and SOI MOSFETs [15–17]. Effectively reducing leakage currents and improving device reliability in advanced CMOS technology nodes requires a deep comprehension of these interconnected electrothermal and material-dependent variables.

In this work, the relationship between gate-induced drain leakage (GIDL) and PBT effects in fully depleted silicon-on-insulator (FD SOI) MOSFETs is investigated in depth using TCAD. In order to provide a thorough knowledge of the differences between overlapping and non-overlapping gate topologies, the work methodically investigates how substrate doping and substrate bias affect surface potential modulation and leakage behavior. Through thermal carrier activation and variations in intrinsic carrier concentration, the impact of temperature variation is examined to clarify its role in increased band-to-band tunneling (BTBT) and GIDL amplification. In order to evaluate how dielectric permittivity and electrostatic coupling impact leakage under different geometric configurations, the role of gate dielectric materials is also examined, specifically contrasting ordinary SiO_2 with high-κ HfO_2. The study is expanded to assess the impact of gate work function engineering and drain voltage scaling as practical leakage reduction techniques. All things considered, these evaluations offer useful design recommendations for maximising electrostatic control, material choice, and structural arrangement, opening the door for the creation of low-leakage, thermally stable, and high-performance FD SOI MOSFETs appropriate for upcoming CMOS technology nodes.

2. Structure & Simulation Framework

As shown in Fig. 1, the device structure used in this investigation is an ultra-thin-body (UTB) completely depleted silicon-on-insulator (FD SOI) MOSFET. The simulated transistor is made out of a 50 nm buried oxide (BOX) layer on top of a 10 nm thick silicon substrate. By creating electrical separation between the active region and the substrate, the BOX layer reduces parasitic leakage pathways and improves electrostatic control. A metal gate with a work function of 4.6 eV is utilized to set the appropriate threshold voltage, and hafnium dioxide (HfO_2, $\varepsilon = 22$), a high-κ dielectric material, is used as the gate insulator with an equivalent oxide thickness (EOT) of 1.6 nm.

To investigate the effect on GIDL and PBT behavior, the substrate region is doped with p-type impurities, and its doping concentration is systematically changed from 1×10^{15} cm^{-3} to 1×10^{19} cm^{-3}. While lightly doped drain (LDD) extensions are added with a doping level of 1×10^{19} cm^{-3}, the source and drain areas are severely doped to a concentration of $N_{SD}=5\times10^{19}$ cm^{-3}.

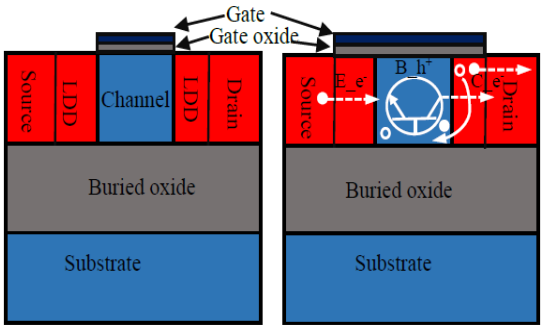

Fig. 1. A schematic cross-section of a fully depleted n-channel MOSFET (a) non-overlapping gate structure (b) Overlapping gate structure. A parasitic bipolar transistor (PBT) is developed in short channel FDSOI MOSFETs where the emitter, base, and collector correspond to the source, channel, and drain regions of the MOSFET, respectively. When PBT is not prominent, the measured leakage current is the actual GIDL current because of BTBT at junctions. However, in presence of effective PBT action the GIDL current is amplified many times, and the measured GIDL current is much larger than the actual GIDL current.

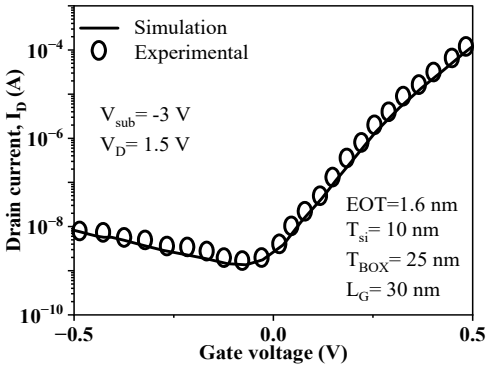

Fig. 2. Calibration of the model parameters using TCAD to align the experimental transfer characteristics presented in Ref. [5].

The Synopsys Sentaurus TCAD suite [14], which provides a thorough and physically correct platform for examining electrostatic behavior and carrier transport in nanoscale devices, was used for all device simulations. The Poisson and continuity equations were solved self-consistently using the drift-diffusion transport model. The Lombardi high-κ degradation model and the Philips unified mobility (PhuMob) model were used to accurately depict mobility deterioration and scattering effects. In order to represent tunneling-induced carrier production, the Schenk band-to-band tunneling (BTBT) model was also used, with electron and hole effective masses set to m_e=0.051 and m_h=0.041, respectively.

To ensure both quantitative consistency and physical precision, the device models were calibrated using previously published experimental data [5]. To accurately resolve high-field locations where tunneling and leakage effects are most prominent, a fine, non-uniform mesh was used close to the drain–body junction and the gate oxide interface. The simulations were run with drain voltages between 0.1 V and 1.5 V and gate voltages between −2 V and 1.5 V. Additionally, temperature-dependent analyses were carried out between 300 and 400 K to examine the thermal dependence of PBT and GIDL processes.

To ensure both quantitative dependability and physical fidelity, the simulated device models were verified against previously published experimental data [5]. A fine non-uniform mesh was used at the gate oxide interface and the drain–body junction to efficiently capture high-field areas linked to tunneling and leakage processes. Gate voltages ranging from −2 V to 1.5 V and drain voltages ranging from 0.1 V to 1.5 V were included in the simulation bias conditions. Furthermore, temperature-dependent simulations were run between 300 and 400 K to examine how thermal fluctuations affected GIDL and PBT properties.

3. Results and Discussion

The simulation findings for the surface potential distribution and GIDL current amplification in fully depleted silicon-on-insulator (FD SOI) MOSFETs under various substrate doping and biasing circumstances are shown in this part. As shown in Fig. 1(a), two structural configurations – non-overlapping gate and overlapping gate designs – were examined. The drain-side spacer region is partially covered by the gate electrode in the overlapping gate construction, which alters the local electric field distribution close to the drain junction and affects the overall leakage characteristics.

Band-to-band tunneling (BTBT) occurs mostly laterally in the non-overlapping gate design because the electric field at the drain edge is mostly vertical. On the other hand, both transverse and lateral BTBT components are present in the overlapping gate structure, and their respective contributions change depending on the polarity and amount of the gate bias. The activation of the parasitic bipolar transistor (PBT) effect is strengthened by this dual tunneling channel, which raises the possibility of hole accumulation within the floating body region.

The impact of substrate doping concentration on the non-overlapping gate FD SOI MOSFET's surface potential and GIDL current amplification is shown in Fig. 3. The channel–source potential barrier is substantially lower at a lower substrate doping level (N_{sub}=1×10^{15}cm^{-3}) than in a highly doped device (N_{sub}=cm^{-3}), as illustrated in Fig. 3(a). This decrease in barrier height implies a greater forward bias state at the emitter–base junction of the parasitic bipolar transistor, which consists of the source, body, and drain. This leads to a noticeable rise in GIDL current, as shown in Fig. 3(b). The higher body potential and the resulting forward biasing of the PBT's base–emitter junction are the main causes of the leakage current's steady increase with decreasing substrate doping.

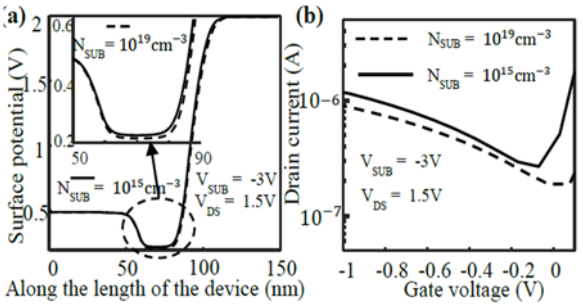

Fig. 3. Effect of substrate doping on (a) surface potential along the length of the channel at channel/gate oxide interface, and (b) GIDL current (ID) in non-overlapping gate FDSOI MOSFETs.

The concentration of the electric field close to the drain extension region greatly increases BTBT production in the overlapping gate design. Stronger vertical electric field components encourage more transverse tunneling, which raises the total GIDL current. Depending on the applied gate and drain bias settings, the overlap region significantly affects whether the device behavior is dominated by lateral or transverse tunneling at a modest substrate doping level ($N_{sub} \approx 1\times10^{17}$ cm^{-3}). This structural dependence emphasizes how important it is to optimize the gate overlap dimension in order to achieve an efficient trade-off between leakage suppression and device performance.

The simulation findings further show that the surface potential distribution and GIDL behavior are significantly affected by substrate biasing. By lowering the body potential, a positive substrate bias weakens PBT activation and suppresses leakage. A negative substrate bias, on the other hand, encourages hole accumulation inside the floating body, which increases leakage and amplifies GIDL. Because lightly doped substrates have a lower electrostatic screening capacity and are more susceptible to possible manipulation, GIDL is significantly more sensitive to substrate bias in these substrates.

Furthermore, the GIDL current's temperature dependency was examined between 300 and 400 K (not included in the picture). The findings show that higher temperatures strengthen the PBT feedback mechanism by increasing BTBT-induced hole creation. However, the temperature-induced widening of the silicon bandgap partially counteracts this impact, resulting in a sublinear increase in leakage current with increasing thermal bias.

Overall, the simulation results show that GIDL and PBT behavior in FD SOI MOSFETs are significantly influenced by both substrate doping concentration and gate overlap geometry. Because of smaller potential barriers and stronger electric field coupling at the drain junction, devices with overlapping gate designs and lower substrate doping show improved GIDL. These findings promote the development of dependable and energy-efficient nanoscale FD SOI technologies by providing crucial design insights for attaining efficient leakage control through substrate engineering and optimal gate architecture.

For a lightly doped substrate ($N_{sub}=1\times10^{15}$cm^{-3}), Fig. 4 shows how surface potential and GIDL current vary with respect to substrate bias (V_{sub}). As shown in Fig. 4(a), the channel–source potential barrier somewhat increases as the substrate voltage drops from –0.5 V to –3 V. This increase in barrier height suppresses hole injection from the body region by lowering the forward bias across the PBT's base-emitter junction. As a result, as the negative substrate bias increases, the GIDL current gradually decreases, as seen in Fig. 4(b). This behavior shows that substrate biasing is a useful electrostatic control strategy for reducing leakage caused by PBT in lightly doped FD SOI MOSFETs.

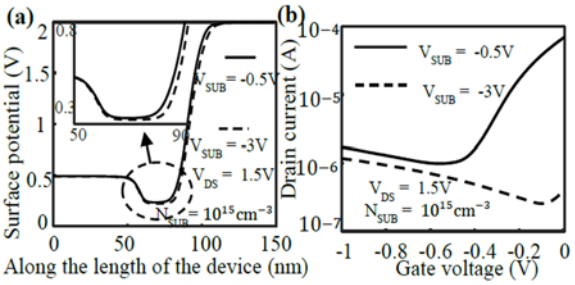

Fig. 4. Effect of substrate bias on (a) surface potential along the length of the channel at channel/gate oxide interface, and (b) GIDL current (ID) in non-overlapping gate FDSOI MOSFETs.

The impact of substrate doping concentration on the overlapping gate FD SOI MOSFET's surface potential and GIDL current characteristics is shown in Fig. 5. The source-channel potential barrier significantly decreases as the substrate doping increases from 1×10^{15} cm^{-3} to 1×10^{19} cm^{-3}, showing increased forward biasing of the base-emitter junction at $V_{GS}=-1.0$V, as illustrated in Fig. 5(a). In contrast, increased substrate doping tends to suppress PBT activation in the non-overlapping gate device. The observed discrepancy results from the overlapping gate region's strong transverse electric field, which modifies the local potential distribution beneath the gate extension and encourages vertical band-to-band tunneling (BTBT) close to the drain edge.

The GIDL current in the overlapping gate design shows greater amplification at higher substrate doping levels, especially at large negative gate biases, as illustrated in Fig. 5(b). It's interesting to note that the two GIDL–V_G curves cross close to $V_G = -0.2$ V, suggesting a change in the dominant tunneling process. Because of the stronger vertical electric fields in the overlap region, the transverse BTBT component becomes dominant at extremely negative gate voltages, while lateral BTBT near the drain–body junction predominates at lesser negative gate voltages. The competing roles of lateral and vertical electric fields in controlling the device's overall leakage

characteristics are highlighted by this crossover phenomenon.

These findings demonstrate the critical role that gate overlap geometry and substrate doping play in the coupled PBT and GIDL behavior of FD SOI MOSFETs. The performance and dependability of next-generation ultra-thin SOI technologies can be improved by precisely controlling gate overlap dimensions and carefully optimising substrate doping levels to achieve an ideal trade-off between leakage suppression and electrostatic integrity.

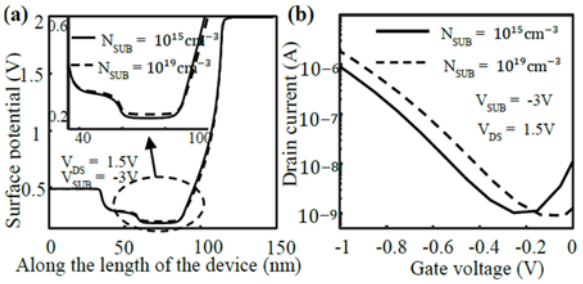

Fig. 5. Effect of substrate doping on (a) surface potential along the length of the channel at channel/gate oxide interface, and (b) GIDL current (ID) in overlapping gate FDSOI MOSFETs.

The overlapping gate FD SOI MOSFET's surface potential and GIDL current characteristics are affected by substrate bias, as shown in Fig. 6. The corresponding GIDL amplification seen in Fig. 6(b) for V_{sub} = −0.5 and V_{sub} =−3.0 V is successfully correlated with the fluctuation in surface potential, as seen in Fig. 6(a). The enhanced vertical electric field in the overlap region promotes band-to-band tunneling (BTBT) under greater substrate reverse bias conditions, which raises GIDL current levels. These results validate that the activation and strength of the parasitic bipolar transistor (PBT) effect are influenced by the electrostatic coupling between the channel and the back gate, which is modulated by substrate biasing.

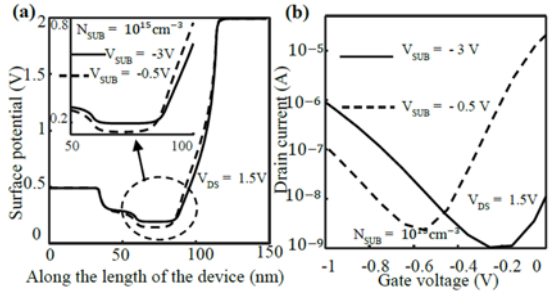

Fig. 6. Effect of substrate bias on (a) surface potential along the length of the channel at channel/gate oxide interface, and (b) GIDL current (ID) in overlapping gate FDSOI MOSFETs.

Overall, the findings show that in overlapping and non-overlapping gate FD SOI MOSFETs, increasing substrate doping has opposing impacts on the channel–source barrier height and GIDL current amplification. Higher substrate doping in non-overlapping devices effectively suppresses GIDL current by raising the potential barrier. On the other hand, even at greater doping concentrations, overlapping gate structures encounter stronger vertical electric fields within the overlap region, which improve transverse BTBT and therefore raise GIDL. In order to achieve an ideal trade-off between leakage reduction and electrostatic performance in modern FD SOI technologies, this conflicting behavior highlights the need to co-optimize gate shape and substrate doping.

The temperature dependency of the gate-induced drain leakage (I_{GIDL} current, measured at V_{DS} = 1.5 V and V_{GS} = −0.5 V) is shown in Fig. 7. I_{GIDL} more than triples when the temperature rises from 280 K to 360 K, demonstrating the leakage mechanism's significant thermal sensitivity. This increase is mainly explained by the intrinsic carrier concentration (ni) growing exponentially with temperature, which promotes carrier production via band-to-band tunneling (BTBT) processes [16]. Higher temperatures cause the silicon bandgap to slightly expand, but this effect is inadequate to offset the overwhelming effect of thermally assisted carrier production, which leads to an overall rise in leakage current.

The spatial distribution of produced holes is shown by the hole density contour plots at two different temperatures in Fig. 8. Increased band-to-band tunneling (BTBT) activity and subsequent hole accumulation within the floating body region are indicated by a marked rise in hole density along the drain–channel interface at higher temperatures. The parasitic bipolar junction transistor's (BJT) feedback mechanism is strengthened by this concentrated increase in hole concentration, which further amplifies the gate-induced drain leakage (GIDL) current.

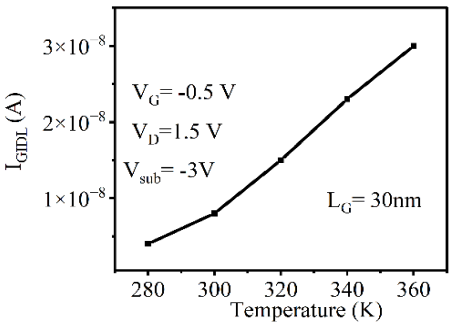

Fig. 7. Effect of temperature on the IGIDL at V_{GS}=-0.5 V, V_{DS} =1.5 V, V_{sub} = -3 V and L_G=30 nm.

In conclusion, the combined examination of temperature dependency, biasing, and substrate doping shows that leakage control in FD SOI MOSFETs is a multifaceted issue. To ensure stable and low-leakage operation at advanced SOI CMOS

nodes, rigorous co-optimization of substrate engineering, gate overlap design, and operating temperature conditions is necessary for effective suppression of GIDL and PBT effects.

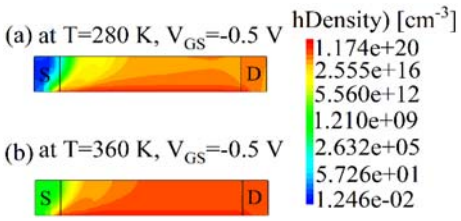

Fig. 8. Contour plot of hDensity at (a) 280 K and (b) 360 K temperature.

In a series of simulations, the drain-to-source voltage (V_{DS}) for both non-overlapping and overlapping gate FD SOI MOSFET structures was varied from 0.5 V to 1.8 V while keeping the gate voltage constant at V_{GS} = −0.5 V in order to examine the impact of electric field intensity on gate-induced drain leakage (GIDL). The effects of electrostatic modulation on leakage behavior were captured by systematically varying the substrate doping concentration (N_{SUB}) from 1 × 1^{15} cm^{-3} to 1 × 10^{19} cm^{-3}. Fig. 9(a) and 9(b), which correspond to the non-overlapping and overlapping gate configurations, respectively, show the ensuing characteristics.

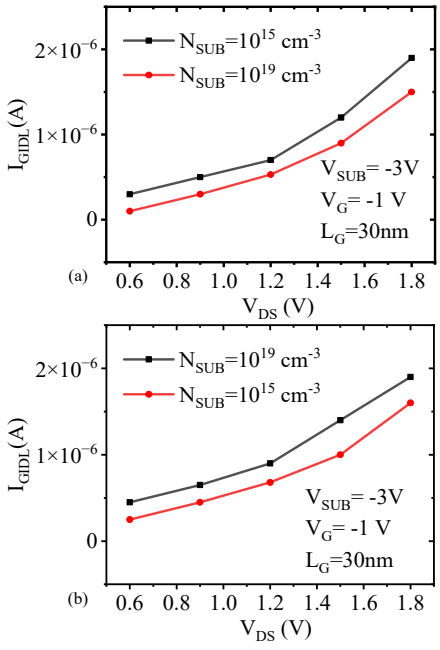

Fig. 9. Variation of GIDL current (IGIDL) with drain voltage (V_{DS}) for different substrate doping concentrations in FD SOI MOSFETs: (a) non-overlapping gate and (b) overlapping gate structures at VGS = −1 V.

The gate-induced drain leakage (I_{GIDL}) current, as illustrated in Fig. 9, shows an exponential increase with rising drain-to-source voltage (V_{DS}) across all substrate doping levels, showing that the electric field at the drain–channel junction primarily controls the leaking mechanism. The lower source-channel potential barrier on weakly doped substrates (e.g., N_{SUB} = 1 × 10^{15} cm^{-3}) enables higher activation of the parasitic bipolar transistor (PBT) under high drain bias, leading to a noticeable amplification of I_{GIDL}. On the other hand, at lower drain voltages, devices with higher substrate doping effectively suppress PBT activation by maintaining a larger source-channel barrier; however, at higher V_{DS} values, field-induced band-to-band tunneling (BTBT) still predominates, resulting in significant leakage enhancement.

Across all substrate doping levels, the overall gate-induced drain leakage (GIDL) current magnitude for the overlapping gate design consistently exceeds that of the non-overlapping counterpart. Band-to-band tunneling (BTBT) is encouraged even at mild drain biases because to the increased transverse electric field created within the gate overlap area. These findings unequivocally show that GIDL amplification in totally depleted SOI MOSFETs is primarily controlled by the strength of the electric field and is further influenced by substrate doping. Furthermore, because of the increased electrostatic interaction between the gate electrode and the drain extension region, overlapping gate designs are more vulnerable to parasitic bipolar transistor (PBT) activation.

SiO_2 and HfO_2 gate stacks, both intended to have an equivalent oxide thickness (EOT) of 1.6 nm to enable comparable electrostatic control, were used in simulations to investigate the impact of gate dielectric material on the leakage characteristics. The gate voltage was held at V_{GS} = −1.0 V, while the substrate doping concentration was maintained at 1 × 10^{15} cm^{-3}. To assess the corresponding changes in leakage behavior, the drain voltage (V_{DS}) was changed from 0.5 V to 1.8 V.

For both dielectric materials, the gate-induced drain leakage (I_{GIDL}) exhibits an exponential dependence on the drain-to-source voltage (V_{DS}), as shown in Fig. 10(a), which corresponds to the non-overlapping gate arrangement. Because of the stronger gate-to-drain electrostatic coupling and the stronger electric field at the drain junction, which promote lateral band-to-band tunneling (BTBT), the device using HfO_2 has a larger leakage magnitude than its SiO_2 counterpart. In contrast, the SiO_2-based device exhibits relatively suppressed GIDL current due to less field penetration into the drain–channel area due to its lower dielectric constant.

The difference in leakage behavior between the two dielectric materials is even more noticeable in Fig. 10(b), which shows the overlapping gate configuration. An additional vertical electric field component is introduced by the gate overlap, and the transverse field intensity is further increased by using a high-κ HfO_2 dielectric. As a result, at large drain biases when both transverse and lateral band-to-band tunneling (BTBT) mechanisms are simultaneously active, the HfO_2-based overlapping structure displays a significantly higher I_{GIDL}. The SiO_2-based

overlapping device, on the other hand, shows a relatively mild increase in leakage current, highlighting its lower field sensitivity and decreased vulnerability to BTBT amplification.

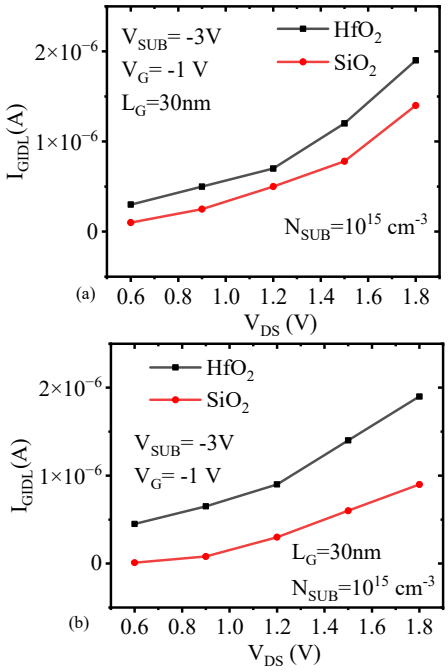

Fig. 10. Variation of gate-induced drain leakage current (I_{GIDL}) with drain voltage (V_{DS}) for two different gate dielectric materials – SiO_2 (ε = 3.9) and HfO_2 (ε = 22) – in (a) non-overlapping and (b) overlapping gate FD SOI MOSFET structures.

These results demonstrate that, particularly in overlapping gate FD SOI MOSFETs, the gate dielectric material significantly affects the gate-induced drain leakage (GIDL) behavior. High-κ dielectrics, such HfO_2, provide better scalability and gate control, but they also increase the gate-to-drain electric field coupling, which makes field-assisted tunneling leakage more likely. Therefore, in order to balance electrostatic control and leakage minimization in future FD SOI device technologies, careful optimization of dielectric properties – such as permittivity, thickness, and interface characteristics – is crucial.

4. Conclusion

The gate-induced drain leakage (GIDL) and parasitic bipolar transistor (PBT) phenomena in fully depletion silicon-on-insulator (FD SOI) MOSFETs were investigated in this work using a thorough TCAD-based analysis. The combined effects of substrate doping concentration, substrate biasing, temperature fluctuations, and gate dielectric material on the leakage characteristics of both overlapping and non-overlapping gate topologies were systematically assessed.

The findings show that the concentration of substrate doping affects the modulation of the source–channel potential barrier in two ways. Higher substrate doping strengthens the potential barrier in non-overlapping gate FD SOI MOSFETs, hence reducing GIDL amplification and moderating parasitic bipolar transistor (PBT) activation. On the other hand, stronger transverse band-to-band tunneling (BTBT) and higher GIDL currents result from enhanced doping in overlapping gate designs, which increases the electric field within the overlap region. Furthermore, substrate bias is a useful control parameter since the application of a negative bias alters the body's internal electrostatics, allowing for partial suppression of leakage.

Since I_{GIDL} increases exponentially with temperature in the region of 280 K to 360 K, temperature fluctuation has a significant effect on the GIDL features. The increase in intrinsic carrier concentration and the improvement of thermally aided tunneling mechanisms are the main causes of this development. Leakage behavior is also strongly influenced by the gate dielectric material selection. Although high-κ dielectrics, like HfO_2, provide better gate electrostatic control, they also increase GIDL in both device designs by amplifying the vertical electric field. In overlapping gate topologies, where transverse electric fields primarily control the leakage mechanism, this effect is very noticeable.

Overall, the results show that minimizing PBT-induced leakage while maintaining robust electrostatic control in sub-30 nm FD SOI MOSFETs requires a balanced co-optimization of substrate doping concentration, gate dielectric properties, and overlap geometry. This work paves the path for energy-efficient CMOS circuits in next technology nodes by providing crucial design recommendations for attaining low-leakage, thermally stable, and high-performance FD SOI technologies.

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