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Comprehensive Dynamic Voltage Drop Analysis on a RISC-V Core: Reliability Evaluation across Extended PVT Corners, Workloads, and Design Parameters

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Abstract: Dynamic voltage drop analysis is a critical aspect of chip design in advanced process nodes, where shrinking dimensions, increasing transistor densities, lower operating voltages, and higher frequencies exacerbate power delivery challenges. These challenges, including voltage fluctuations and localized hotspots, directly impact circuit performance and reliability. This article presents a comprehensive dynamic voltage drop analysis using a RISC-V core as a case study. The analysis evaluates the design's susceptibility under variable statistical workload toggle rates, validated with a compute-intensive real workload. A sensitivity analysis examines the impact of package inductance, variable toggle rates, and the role of decoupling capacitors. Additionally, the article investigates the timing implications of voltage drop, demonstrating how voltage fluctuations can result in severe timing violations. The study includes simulations across extended process–voltage–temperature (PVT) corners to examine how process, voltage, and temperature variations influence dynamic voltage drop and circuit reliability. This characterization provides a clear understanding of voltage stability in RISC-V cores under realistic design and operating conditions. Simulations conducted on a 16 nm FinFET process node offer valuable insights into the interplay between dynamic voltage drop, PVT variations, and timing reliability. To the best of our knowledge, this is the first study to perform such an in-depth analysis on a RISC-V core under these conditions.

Keywords: Dynamic voltage drop, Reliability, RISC-V, PVT corners.

1. Introduction

The stability of an integrated circuit's Power-Delivery Network (PDN) defines its ability to meet timing and reliability targets, where voltage drop is one of the most critical factors affecting power integrity and timing closure in advanced technologies. This phenomenon refers to a temporary reduction in the supply voltage across the power delivery network caused by transient current surges when large groups of transistors switch simultaneously. Excessive voltage drop reduces the effective gate overdrive of transistors, slows switching, and can ultimately lead to timing violations or functional failure.

Two primary categories of voltage drop are generally distinguished. The first is the static voltage drop, which results from resistive ($I \cdot R$) losses in the PDN under steady-state conditions [1]. The second, and the focus of this work, is the dynamic voltage drop, which occurs due to fast transient switching [1]. It arises from both resistive and inductive components and can be expressed as:

$$V_{drop} = (I \cdot R) + L \cdot \frac{dI}{dt} \quad (1)$$

Dynamic voltage drop manifests on both the V_{DD} (power) and V_{SS} (ground) rails, as transient switching activity and rapid current changes cause voltage fluctuations in either direction.

While the resistive term represents voltage loss proportional to current and metal resistance, the inductive term captures the transient behavior associated with the rate of current change. These effects make dynamic voltage drop highly dependent on switching activity, toggle rate, operating frequency, and the parasitic inductance of the PDN and package. Consequently, dynamic voltage drop is inherently time-dependent and more complex to characterize than its static counterpart.

This article presents a comprehensive analysis of dynamic voltage drop using a RISC-V core implemented in TSMC 16 nm FinFET technology. The study evaluates voltage fluctuations under variable switching conditions using two complementary methodologies: (1) vectorless analysis, which estimates switching activity statistically based on toggle probabilities, and (2) workload-based simulation, which employs real switching traces from compute-intensive benchmarks [1]. Together, these methods enable a broad and realistic coverage of dynamic behavior under different design and operating conditions. Furthermore, a sensitivity analysis examines the effects of package inductance, toggle rate, and decoupling capacitance on dynamic voltage drop, emphasizing their importance in power delivery networks. We also quantify the timing implications of voltage drop and show that such drops can lead to significant timing violations.

In addition, this work extends our prior analysis [10] by simulating dynamic voltage drop across 34 process–voltage–temperature (PVT) corners, covering slow–slow (SS), typical–typical (TT), and fast–fast (FF) process conditions, supply voltages from 0.55 V to 1.05 V, and temperatures ranging from −40 °C to 150 °C. This provides deeper insight into how transistor properties such as carrier mobility and drive strength interact with PDN resistance and inductance, collectively determining the stability of the supply voltage.

To the best of our knowledge, this work is the first to provide an in-depth dynamic voltage drop analysis that combines workload-dependent, parametric, and comprehensive PVT variations for a RISC-V core in a 16 nm FinFET technology. The results establish a critical baseline for developing robust power integrity methodologies and voltage drop mitigation strategies for advanced node designs.

2. Related Background and Prior Works

This section reviews the main challenges related to dynamic voltage drop and highlights key prior studies addressing power delivery reliability in modern semiconductor design.

2.1. Dynamic Voltage Drop Analysis

Dynamic voltage drop is a key factor influencing the reliability and performance of modern integrated circuits. As transistor density continues to rise, supply voltages scale down, and operating frequencies increase, maintaining stable power delivery becomes a major challenge. The introduction of advanced multi-die and 3D packaging structures further complicates the power network, amplifying voltage fluctuations and creating localized hotspots that threaten both timing integrity and circuit stability. Ensuring consistent power delivery across these conditions is therefore essential to preserve design robustness, energy efficiency, and functionality.

Voltage drop analysis focuses on identifying reductions in supply voltage within both the package and on-die power-delivery networks (PDNs), which arise as current propagates through their inherent impedance. As illustrated in Fig. 1, the PDN connects the voltage regulator to the standard cells through two primary domains: the package PDN and the on-die power grid. The observed voltage drop is mainly attributed to the combined effects of resistance and inductance within these components, which together determine the effective voltage delivered to each standard cell. A decrease in this supply voltage can cause timing degradation or even functional failures. In advanced chips, dynamic voltage drop is checked at several supply voltages because both current and PDN impedance change with V_{DD}, and similar checks are also performed at different temperatures and process corners to confirm stable behavior under all conditions. Therefore, maintaining voltage drop within strict limits is essential throughout the physical-design process to ensure robust operation and achieve timing closure.

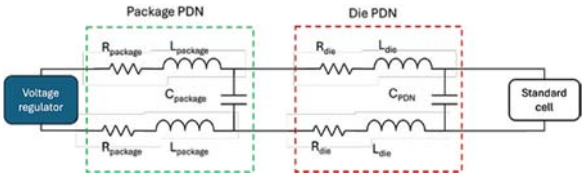


Fig. 1. Power Delivery Network (PDN) model from voltage regulator to standard cell.

2.2. Prior Works

Numerous studies have investigated the impact of dynamic voltage drop in advanced semiconductor technologies, recognizing its increasing influence on power integrity, timing reliability, and overall circuit performance as technology nodes continue to scale. Despite this broad attention, only a limited number of works have presented comprehensive analyses targeting RISC-V processors.

A recent study [3] demonstrated that external parasitic elements including the package, printed circuit board (PCB), and voltage-regulator modules play a decisive role in voltage drop behavior. Using a RISC-V CPU as a case study, it revealed that these non-die components can introduce up to 5.8 %

additional voltage drop, resulting in clock-frequency degradation not captured by conventional chip-level simulations. The work proposed a distributed PDN modeling approach to improve analysis accuracy and bridge chip-to-system correlation.

Another significant contribution [4] proposed a Design-Technology Co-Optimization (DTCO) framework for sub-10 nm process nodes, integrating process-design-kit (PDK) generation, design implementation, and IR-drop-aware PDN optimization. Based on N5-like process assumptions, it demonstrated that PDN and voltage drop awareness are essential for balancing area–power–performance trade-offs. The study reported up to 20 % area gain with minimal voltage drop penalties, and showed that device selection can cause variations reaching 15 % in power, 2× in performance, and 20 % in area.

A complementary work [5] presented a systematic methodology for static and dynamic voltage drop and electromagnetic interference (EMI) analysis using the Apache RedHawk tool. It introduced practical design techniques such as improved power-grid routing, standard-cell layout adjustments, and EMI-reduction strategies to mitigate on-chip power-integrity issues. Additionally, a survey [6] reviewed advanced approaches for robust PDN design and outlined emerging research challenges. Using FinFET-based test cases simulated in ANSYS RedHawk, the study compared multiple design strategies and emphasized the growing importance of PDN co-optimization in nanometer technologies.

More recently, our prior work [10] presented a dynamic voltage drop analysis on a RISC-V core implemented using the TSMC 16 nm FinFET process, focusing on the effects of package inductance, toggle rate, decoupling capacitance, and timing impact under both statistical vectorless and workload-based stimuli. To date, almost no published studies have characterized dynamic voltage drop behavior across full process–voltage–temperature (PVT) corners in a RISC-V core implemented in TSMC 16 nm FinFET technology. The experiment presented in this article addresses that gap by analyzing the interaction of PVT on PDN behavior using Cadence Voltus Training Kit (VTK) vector-less simulations.

3. Dynamic Voltage Drop Simulation Analysis

This section presents a detailed analysis of dynamic voltage drop, beginning with an overview of the simulation environment. It then examines the effects of package inductance, toggle rate, and decoupling capacitance, followed by an evaluation of timing implications consistent with the methodology presented in [10]. The analysis further includes characterization across different process–voltage–temperature (PVT) corners to capture variation trends under realistic operating conditions. Finally, it assesses behavior under compute-intensive workloads, providing a complete view of power-integrity performance in RISC-V 16 nm FinFET technology.

3.1. Experimental Setup and Methodology

The experimental setup utilizes the RISC-V RI5CY processor [2], a compact and energy-efficient core optimized for low gate count and power consumption, making it an ideal candidate for dynamic voltage drop analysis. The implementation environment incorporates the Cadence Genus synthesis tool, Innovus for place-and-route, and Voltus for power-integrity analysis. All simulations were performed using the TSMC 16 nm FinFET process, which features a nine-metal-layer stack with an additional AP layer and a nominal operating voltage of 0.72 V. The synthesis, place-and-route, and voltage drop analyses were executed on an Intel Xeon 8-core workstation with 128 GB RAM, with each simulation requiring approximately 15 minutes to complete.

The dynamic voltage drop analysis methodology, illustrated in Fig. 2, integrates the standard digital design flow with advanced power-integrity verification. The process begins with Verilog RTL design, followed by logic synthesis, place-and-route, and gate-level simulation to generate switching-activity data. These results, combined with the post-layout netlist, form the input for dynamic voltage drop analysis. The simulation setup also supports PVT-based voltage drop analysis by applying the appropriate cell libraries and technology files for each process, V_{DD} and temperature corner in Voltus. This ensures that both device and power-grid variations are accurately captured under real operating conditions.

The Voltus tool supports two complementary modes of analysis. The vector-less (statistical) mode applies probabilistic toggle-rate modeling to estimate switching activity rapidly without explicit input vectors. In contrast, the vector-based mode relies on real switching traces from compute-intensive workloads or dedicated testbenches, achieving higher accuracy at the expense of longer runtime. Both modes feed into the dynamic voltage drop analysis engine, which generates reports such as voltage drop heatmaps and statistical distributions. This dual-mode capability enables both early-stage conservative estimation and late-stage realistic validation, ensuring robust PDN reliability throughout the design flow.

3.2. Package Inductance

The experimental analysis begins by examining the dynamic voltage drop maps shown in Fig. 3, which were generated under a 30 % statistical toggle rate for different inductance values. The color gradient in each map indicates the severity of the voltage drop, where red and yellow regions represent higher drops, while green and blue regions denote lower drops. All figures show a maximum voltage drop of 38 mV.

Fig. 3(a) illustrates the voltage drop distribution at an inductance of 0.1 nH, where voltage levels remain relatively uniform with minimal areas of significant drop. In Fig. 3(b), corresponding to an inductance of 0.5 nH, more noticeable voltage variations and localized drops appear, indicating increased sensitivity to inductance. Fig. 3(c), representing 5 nH, reveals widespread regions of severe voltage drop, demonstrating the substantial effect of higher inductance on power-delivery stability.

To further examine these results, voltage drop histograms were generated under the same 30 % statistical toggle rate for different inductance values. Figs. 4(a) and 4(b) illustrate the voltage drop distributions for 0.1 nH and 5 nH, respectively, where negative and positive values correspond to voltage rebound on V_{SS} and voltage drop on V_{DD}, respectively. The x-axis represents voltage drop in millivolts (mV), and the y-axis shows the total number of occurrences.

For 0.1 nH, most drop events are concentrated around lower values, indicating a stable voltage profile with minimal significant fluctuations. In contrast, the histogram in Fig. 4(b) (for 5 nH) displays a broader distribution, with a clear shift toward higher voltage drop values. This reflects increased variability and a higher frequency of large voltage drops, emphasizing the adverse influence of elevated inductance on power-delivery stability. The wider distribution highlights stronger voltage fluctuations, which may degrade system performance, tighten timing margins, and affect overall reliability.

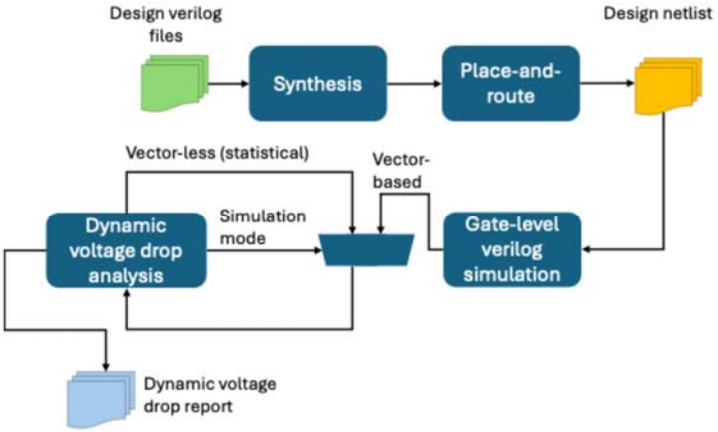


Fig. 2. Dynamic voltage drop analysis flow.

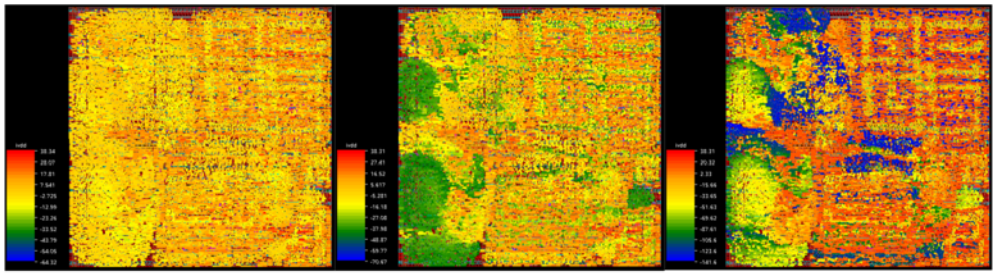
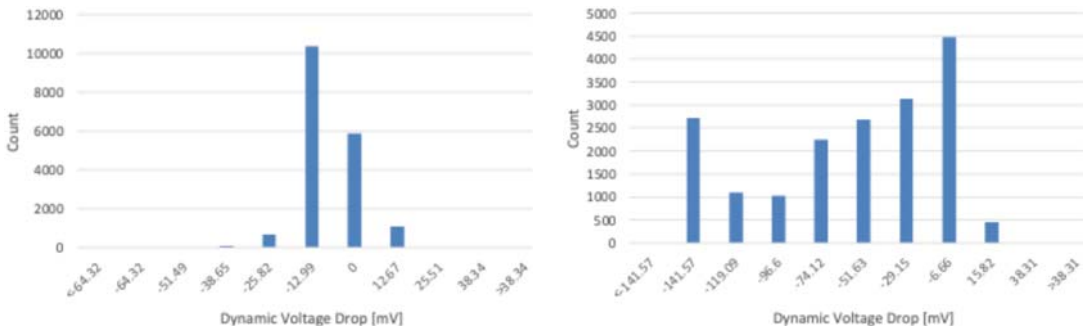


Fig. 3. Dynamic voltage drop maps using 30 % statistical toggle rate and variable inductance values: (a) 0.1 nH, (b) 0.5 nH, and (c) 5 nH.



(a) (b)

Fig. 4. Voltage drop histograms with 30 % statistical toggle rate and variable inductance: (a) 0.1 nH and (b) 5 nH.

3.3. Statistical Toggle Rate

Fig. 5 shows the dynamic voltage drop maps obtained under different statistical toggle rates with a constant inductance of 1 nH. At a 10 % toggle rate Fig. 5(a), voltage drops are minimal and confined to localized regions, reflecting limited switching activity. As the toggle rate increases to 20 % Fig. 5(b) and 30 % Fig. 5(c), the magnitude and spatial extent of voltage drops grow noticeably. This trend continues at 40 % Fig. 5(d) and reaches its maximum at 50 % Fig. 5(e), where high-intensity drops dominate the map. These results confirm a strong positive correlation between toggle rate and dynamic voltage drop severity, emphasizing the importance of robust PDN design for stable operation under high-switching conditions.

Fig. 5(f) presents the corresponding switching-power distribution for the 50 % toggle-rate case. Regions circled in green mark areas of high switching power that produce a debounce effect, resulting in a negative voltage drop. These regions contribute to stabilizing the power delivery network by counteracting voltage fluctuations. Conversely, the red circled areas denote regions of substantial positive voltage drop, where intensive switching activity amplifies transient fluctuations and led to significant voltage instability.

Together, these maps reveal a clear spatial relationship between switching-power density and dynamic voltage drop magnitude. This coupling suggests that parameters such as toggle rate and switching power can serve as effective features for machine-learning-based prediction and mitigation of voltage instability in power-delivery systems.

3.4. Decoupling Capacitors

Decoupling capacitors (decaps) [7] play a fundamental role in maintaining on-chip power integrity. Integrated throughout the power delivery network, they temporarily store charge and release it during switching transitions, thereby compensating for transient current surges. Acting as localized energy buffers, these capacitors suppress rapid voltage fluctuations and significantly mitigate dynamic voltage drops generated when large groups of logic elements switch simultaneously. Through this mechanism, decaps enhance supply stability, preserve timing accuracy, and sustain circuit reliability in advanced process technologies, where reduced supply margins make designs increasingly sensitive to transient disturbances.

To assess their impact within our study, we simulated the design both with and without decaps incorporated into the PDN. The corresponding voltage drop distributions are shown in Fig. 6, where (a) represents the configuration without decaps and (b) represents the case with decaps. In both scenarios, the inductance is fixed at 10 nH, and the statistical toggle rate is 10 %. Comparing these histograms clearly demonstrates how the presence of decaps narrows the spread of voltage drop values, confirming their effectiveness in stabilizing the local supply and improving overall PDN resilience under identical operating conditions.

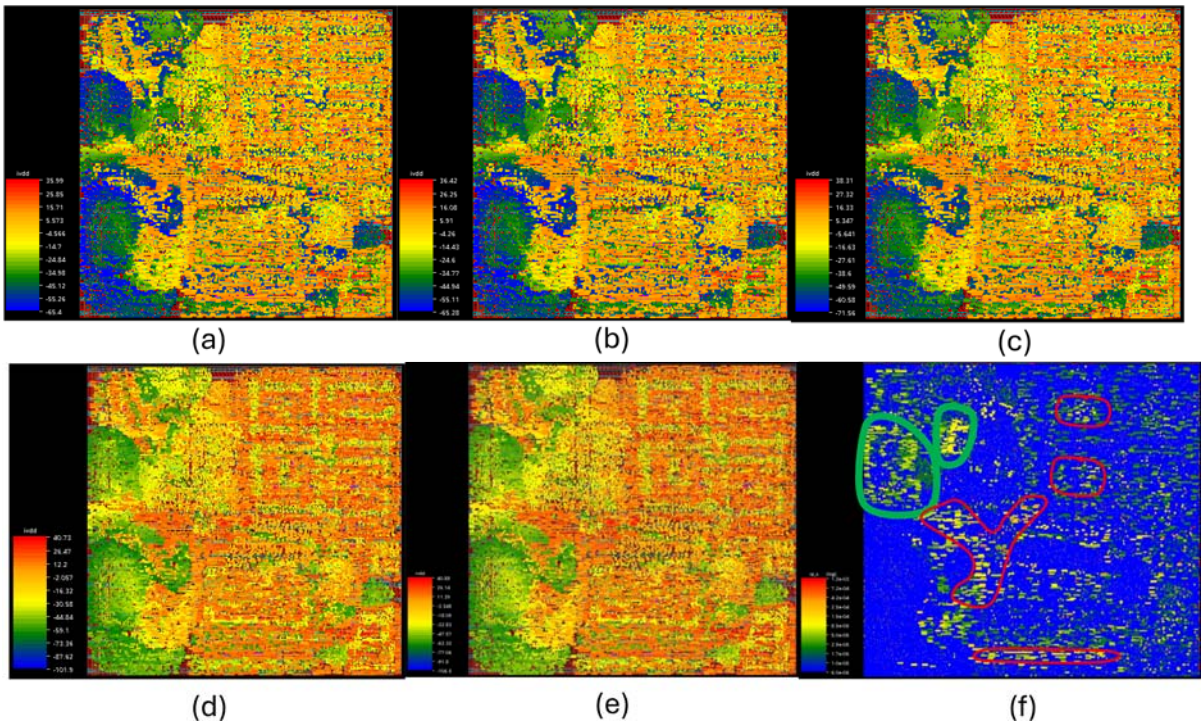


Fig. 5. Dynamic voltage drop maps under variable statistical toggle rates with constant 1 nH inductance: (a) 10 %, (b) 20 %, (c) 30 %, (d) 40 %, and (e) 50 %, respectively. Fig. (f) presents the corresponding switching-power map for case (e).

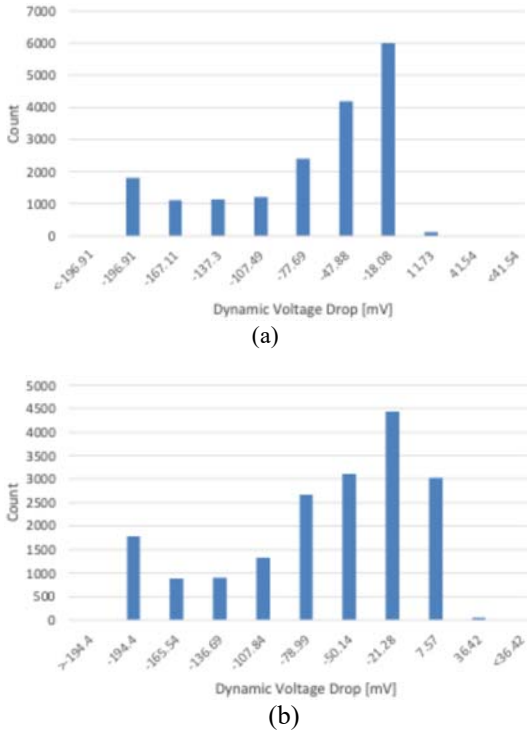


Fig. 6. Voltage drop histograms for 10 % statistical toggle rate and 10 nH inductance: (a) without decaps and (b) with decaps.

3.5. Timing Impact

Voltage drop simulation results indicate a 35.99 mV reduction in supply voltage across the clock buffers in the capture branch, while the launch branch remains unaffected. To evaluate how this voltage degradation alters timing, the relationship between propagation delay and supply voltage is quantified using the alpha-power law [8], expressed as:

$$t_{pd} \propto \frac{V_{DD}}{(V_{DD}-V_{th})^{\alpha}}, \quad (2)$$

where V_{DD} is the nominal supply voltage, V_{th} is the threshold voltage, and $\alpha \approx 1.3$ denotes the velocity-saturation index [8].

Substituting the pre- and post-drop supply voltages together with the threshold voltage into (2) yields an 8.5 % increase in propagation delay for the capture path. This translates to an additional 12.75 ps delay in the capture-clock arrival time, directly degrading the hold-time slack. When the original slack is smaller than 12.75 ps, a hold violation occurs, potentially causing functional failure. Even if the slack margin is larger, the reduced timing headroom leaves the circuit more vulnerable to additional voltage variations or process–temperature fluctuations.

3.6. PVT Corners Analysis

Dynamic voltage drop is highly sensitive to process, voltage, and temperature (PVT) variation. To investigate these dependencies, an extensive set of simulations was performed using Cadence Voltus Vectorless Mode (VTK) on the RISC-V RI5CY core. These simulations covered three process corners slow–slow (SS), typical–typical (TT), and fast–fast (FF) across voltages from 0.55 V to 1.05 V and temperatures between –40 °C and 150 °C, with a fixed 1 nH package inductance and a 50 % statistical toggle rate. This setup provided a consistent PDN baseline for evaluating how device speed and environmental conditions influence transient voltage stability.

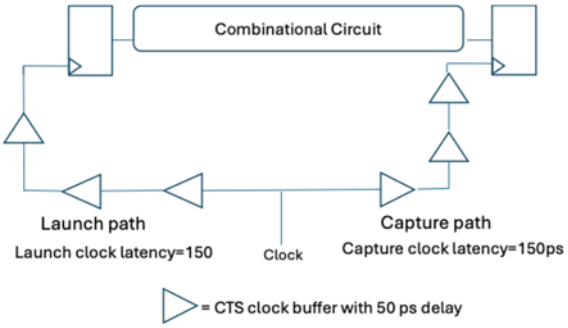


Fig. 7. Launch–capture timing path with clock-tree buffering (three 50 ps stages, 150 ps total).

Across all corners, the supply voltage has a direct influence on dynamic voltage drop. When the supply voltage increases, transistors deliver stronger drive currents and switch faster, resulting in higher current slew rates (dI/dt). These effects amplify both the resistive ($I \cdot R$) and, more significantly, the inductive ($L \cdot dI/dt$) components of the voltage drop. In the SS corner, the maximum drop increases from 21.49 mV at 0.675 V to 53.85 mV at 0.9 V (–40 °C). In the TT corner, raising the supply from 0.55 V to 1.0 V (25 °C) increases the drop from 15.39 mV to 85.54 mV. The FF corner exhibits the steepest rise, reaching 112.25 mV at 1.05 V and 125 °C, the highest recorded value among all simulations. These results confirm that higher supply voltages lead to proportionally larger dynamic voltage drops due to increased current flow and faster switching activity. At any given temperature within the same process corner, Fig. 8(a–c) shows that higher supply voltages consistently correspond to larger dynamic voltage drops.

When comparing process corners, the overall magnitude of dynamic voltage drop increases progressively from SS to TT and FF. The SS corner shows smaller average drops, for example, 30.508 mV at 0.72 V and 0 °C. The TT corner demonstrates moderate drops such as 41.413 mV at 0.75 V and 25 °C. In contrast, the FF corner shows a sharp escalation, where 58.397 mV at 0.825 V, 0 °C and 112.25 mV (at 1.05 V, 125 °C) highlight this trend. In the FF corner, stronger transistors switch faster and draw higher transient currents, creating a larger current change (ΔI) over a shorter interval (Δt). This increases the current slew rate (dI/dt), which

amplifies both the resistive ($I \cdot R$) and, more significantly, the inductive ($L \cdot dI/dt$) components of the voltage drop. As a result, inductive noise dominates, making the FF corner the worst-case scenario for dynamic voltage drop analysis. As shown in Fig. 8, for the same supply voltage and temperature, the FF corner consistently exhibits the highest voltage drop, while the effect gradually weakens in the TT and SS corners.

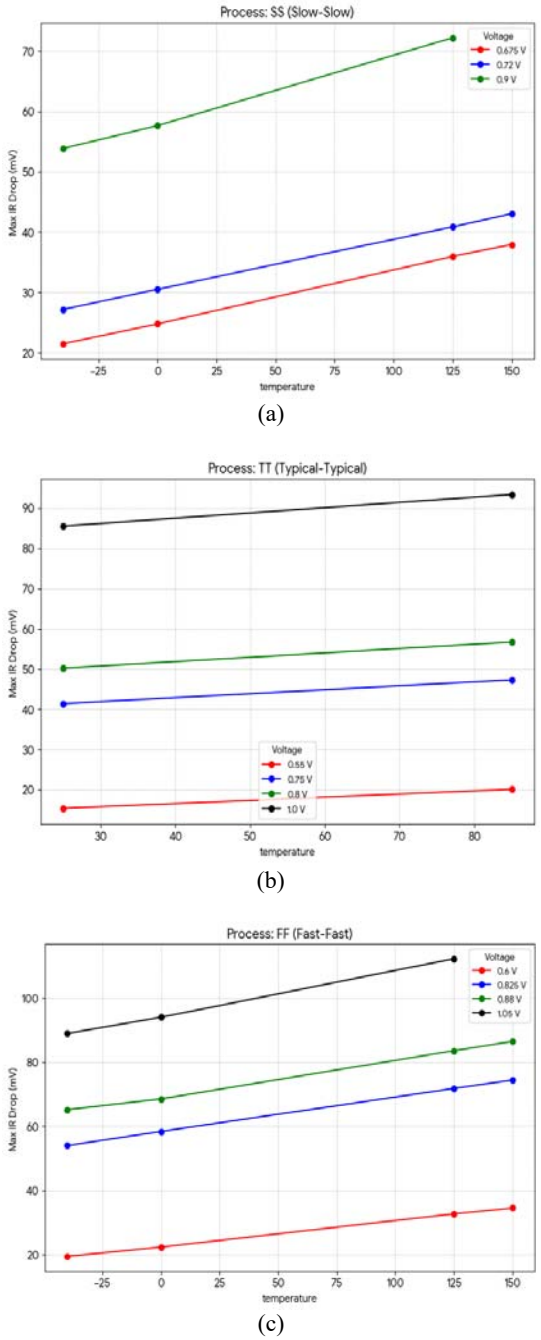


Fig. 8. Maximum Voltage Drop vs. Temperature at Various Voltages for (a) SS, (b) TT, and (c) FF Process Corners.

Temperature further modulates this behavior by altering both carrier mobility and interconnect resistance. As temperature rises, metal resistivity increases, strengthening the ($I \cdot R$) component, while transistor drive current slightly decreases due to reduced carrier mobility. The data shows that the combined effect is a steady rise in total voltage drop, indicating that the increased metal resistance is the dominant factor. For example, in the SS corner at 0.72 V, the maximum drop increases from 27.19 mV (–40 °C) to 43.05 mV (150 °C), while in the FF corner at 0.825 V, it grows from 54.01 mV (–40 °C) to 74.41 mV (150 °C). As clearly shown in the graphs Fig. 8, this steady rise with temperature is consistent across all voltage levels and process corners.

A comparison of the histogram distributions between the SS best-case Fig. 9(a) and FF worst-case scenario Fig. 9(c) provides further insight. The SS histogram displays a narrow drop count peak centered on lower drop values, reflecting lower switching activity and reduced current transients under slow device conditions. Conversely, the FF histogram spreads broadly toward higher counts and larger drop magnitudes, indicating stronger current surges and greater temporal variation in dynamic behavior. These results show that faster process conditions, higher voltage and temperature lead to wider voltage drop distributions and a higher drop values.

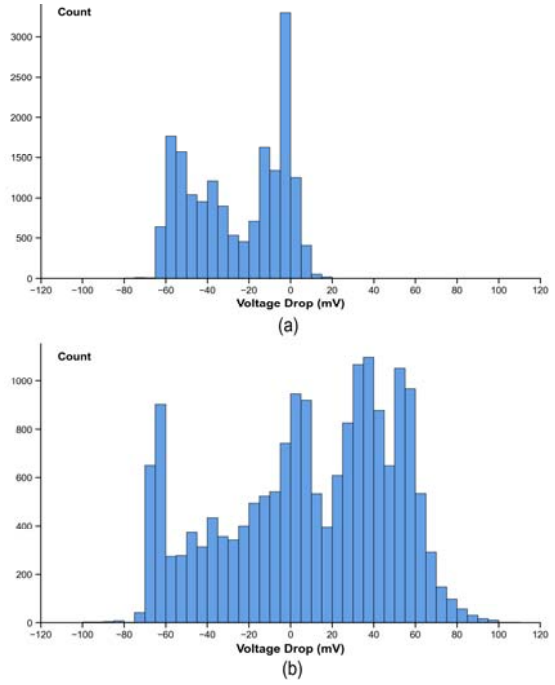


Fig. 9. Histogram Distribution of Dynamic Voltage Drop Magnitudes for (a) SS and (b) FF Corners.

Overall, the PVT characterization demonstrates that both current magnitude (I) and its time derivative (dI/dt) vary strongly with process speed, supply voltage, and temperature.

The combined effects of these parameters dictate dynamic voltage drop behavior in advanced FinFET designs. These findings provide a clear physical explanation of power-integrity limitations and

establish a foundation for corner-aware predictive modeling and reliability optimization in future RISC-V implementations.

3.7. Dynamic Voltage Drop with SHA256 Workload

The final stage of the analysis investigates dynamic voltage drop behavior under a realistic computational workload executed on the RISC-V core. As a representative case, the SHA-256 benchmark [9] implemented in C and compiled for the target processor was employed because its hashing operations induce sustained and spatially distributed switching activity across multiple functional units.

Fig. 10 shows the resulting voltage drop heatmap captured during the peak switching interval with an assumed inductance of 1 nH. The simulation reveals a maximum voltage drop of approximately 64 mV, primarily concentrated in the arithmetic logic unit, register file, and memory interface, corresponding to the regions of highest computational demand in the SHA-256 algorithm.

The corresponding voltage drop distribution is presented in Fig. 11. More than 97 % of instances exhibit only minor voltage reductions, ranging from –0.67 mV to 7.41 mV, indicating that most of the design maintains a stable supply voltage during operation. This distribution is considerably narrower than that observed in the statistical-toggle-rate experiment shown in Fig. 12, even under a 10 % toggle rate.

Hence, the statistical simulations provide a deliberately conservative view of voltage drop severity, whereas the workload-driven analysis reflects more realistic switching conditions encountered in functional operation.

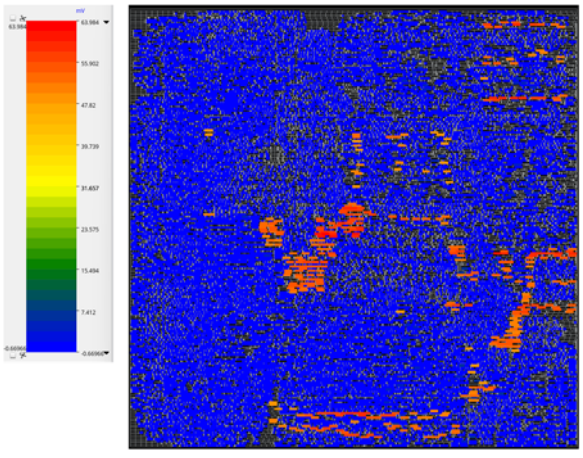


Fig. 10. Voltage drop heatmap during SHA-256 workload execution.

4. Conclusions

This study presented a comprehensive dynamic voltage drop analysis for a RISC-V processor core implemented in a 16 nm FinFET process node. The investigation showed that dynamic voltage drop is primarily governed by package inductance and statistical toggle activity, where larger inductance and higher switching rates intensify voltage fluctuations and broaden the spatial spread of drop occurrences across the design. The inclusion of decoupling capacitors was shown to effectively reduce the voltage drop magnitude by providing local charge compensation during high switching activity, thereby improving supply stability and overall reliability.

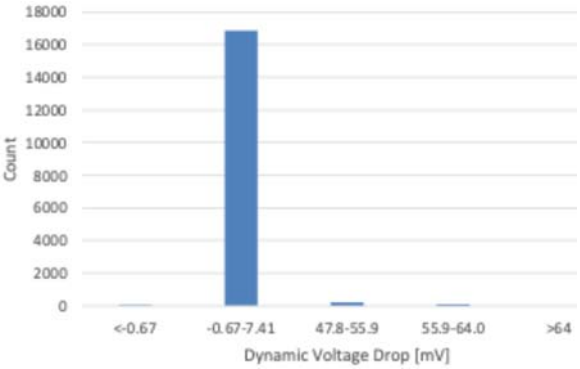


Fig. 11. Voltage drop histogram for the SHA-256 workload.

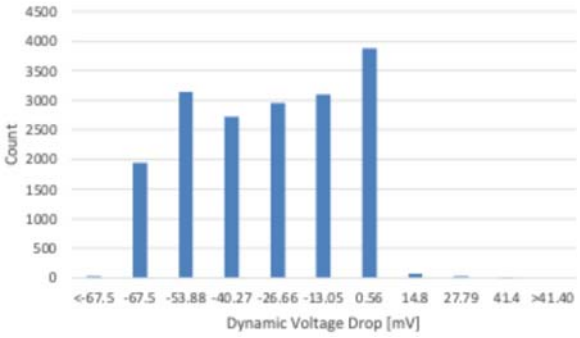


Fig. 12. Voltage drop histograms with 1 nH inductance and 10 % toggle rate.

The timing analysis, based on the alpha-power law, further demonstrated that voltage degradation in the capture clock path can increase propagation delay by up to 8.5 %, corresponding to 12.75 ps, which may lead to hold-time violations when available slack is limited. The investigation across PVT corners revealed that the fast-fast corner, particularly at high temperatures and supply voltages, represents the worst-case condition for dynamic voltage drop. This phenomenon is attributed to faster transistor switching, which generates a higher rate of current change and higher resistivity. Conversely, the slow-slow corner at low temperatures and supply voltages produced the smallest voltage drop. These results confirm that PVT variations critically impact power integrity and must be comprehensively analyzed to ensure robust signoff under all manufacturing and environmental variations.

When comparing statistical toggle-rate simulations with real-workload analysis using the SHA-256 benchmark, it was observed that statistical simulations yield more conservative voltage drop estimates, making them suitable for worst-case validation. In contrast, workload-based experiments showed localized voltage drops up to 64 mV, primarily concentrated in the arithmetic logic unit, register file, and memory interface, reflecting realistic activity under computationally intensive operations.

Overall, the results provide an integrated understanding of how inductance, switching activity, timing behavior, and PVT variation collectively shape dynamic voltage drop phenomena in advanced designs. The presented methodology and outcomes form a practical framework for power-delivery-network optimization, guiding designers in enhancing power integrity and ensuring timing reliability across diverse workloads and process conditions.

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