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Development and Analysis of Nanosheet FETs for Faster Switching Application

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Abstract: Scaling FinFETs beyond the 10 nm technology node leads to worsened short-channel effects (SCEs) prompting a transition from the tri-gate architecture to a Gate-all-around (GAA) architecture. The nanowire type GAA offer superior electrostatic control, while wider nanosheets deliver higher ON current and superior switching speed. A novel GAA nanosheet device is developed in rectangular architecture utilising HfO_2 gate stack dielectric. A chronological design of GAA Nanosheet evolution from a single rectangular GAA to 3×2 and 2×3 Nanosheets are projected with (i) stacked gate high -k, (ii) gate underlaps in nanosheet (iii) variation in channel height and (iv) underlap wrapping with high-k (HfO_2). The Ion/Ioff current ratio, transconductance, and SCEs such as subthreshold slope and DIBL are acquired for each device and compared with the 2 nm node IRDS 2022 for performance enhancement. On varying the channel height, the device with lesser height (Device I) displays more ON current and device with lesser width (Device H) provides enhanced short channel performances. Hence, the superior performances of the Stacked Nanosheet (SU-NS) FETs with high-speed switching brand them suitable for fast processors, RF circuits and related applications; thus, equipped as the future device of the semiconductor industry.

Keywords: Gate all around, Nanowire, Switching speed, Gate underlap, Stacked nanosheet.

1. Introduction

The present technological era demands the semiconductor industries to scale down the transistor size while acquire low power dissipation, maximize operating frequency, low leakage current, and increase transistor density on chip for faster high performing processors. On shrinking the transistors continuously, the devices are approaching nano regime, which results in a loss of gate control inducting short channel effects (SCEs), such as subthreshold swing, gate leakage current due to oxide thickness scaling, drain-induced barrier lowering (DIBL), channel length modulation and so on [1, 2]. These SCEs degrade device performances, thereby sabotage the required outputs [1-3]. To overcome these effects, several novel FET device structures are developed such as double gate FET, omega gate, pi gate, tri gate, FinFET and GAA FET, which are basically multi gate devices [4]. Out of these FinFET technology is one of the most matured alternative and it cordons the advantage of reducing SCEs by fin width scaling for added gate

controllability, fin height scaling for more DC current, and fin pitch scaling to reduce parasitic capacitances [5]. In FinFETs, healthier device performance is achieved by increasing the fin height. However, the resulting performance improvement is less than expected because of the increase in parasitic capacitances [5, 6].

Further, the researchers focused on decreasing the thickness of the insulating layer while scaling down the device. As the gate-oxide thickness (t_{ox}) decreases, gate quantum meth dioxide is replaced with high-k dielectric materials such as Al_2O_3, HfO_2, ZrO_2 as gate insulators to increase the physical gate height while keeping the same effective oxide thickness (EOT) [7]. However, due to excessive surface phonon scattering for the presence of interface traps at the high-k and silicon interface the mobility of carriers reduces hence, the ON current decreases [8]. This problem is observed to be lessened by the use of Gate High-k Stack a combination of both SiO_2 and a high-k dielectric used as gate oxide [6-10]. In this case SiO_2 is placed between the silicon channel and high-k dielectric providing a healthier oxide interfacing while SiO_2 forms a good bonding with the Si channel. This composite arrangement reduces interface traps and scattering to a big extent [9, 10]. With these modifications FinFETs provide enriched performances but, as the scaling continues down to nanoscale regime the FinFETs are again struggling to reach the expected results due to increase of the capacitances and lose the gate control over the channel region by virtue of close proximity of source and drain.

Among all these modern structures developed, Gate All Round (GAA) FET is a multigate device structure that allows further scaling down of the feature size below the 10 nm technology node without degrading short channel performances providing enriched electrostatic gate control [7-9] and ballistic carrier transport. As the GAA FET have low characteristic length, high drive current and high packing density than DG FETs or FinFETs, higher performance and controlled SCEs are observed [6, 7, 9, 10]. More so, the electron mobility of silicon GAA FET is higher than planer MOSFETs leading to velocity saturation and in some cases ballistic transport exists due to stronger quantum carrier confinement. GAA FETs provide excellent gate control significantly minimizing the SCEs [10-12], but still on reduction of the device to be at per with the 5 nm technology node as per IRDS 2022 [13] the SCEs revamp disturbing the performance efficacy by induction of band-to-band and quantum mechanical tunnelling [9-12]. Introducing an underlap onto this device disseminate the SCEs to some extent as in case of DG FETs subduing the DIBL [14-16]. Y, Potaraju et.al. [15] develop of a novel Gate- All-Around Field-Effect Transistor (GAAFET) incorporating a strained silicon channel with a 10 nm. The GAAFET, featuring an ultrathin strained silicon channel, demonstrates enhanced performance compared to the IRDS 2022 reference device, offering superior characteristics and better control over short-channel effects (SCEs).

Further the underlap region provides immunity against GIDL and fringing capacitances, which are developed due to the sidewall spacers. But attributing to the concept of underlap structure, the effective channel length becomes long in the subthreshold region and short in the on-state thereby reduces the leakage as well as the ON current [17, 18], which is not a desired outcome. Also, it is to be noted that the silicon underlap regions formidably interacts with the gate contact generating another fringing field in nano-devices leading to reduced ON current, which needs to be controlled. Sachid et. al. [19] suggested optimizing the source-drain underlap dimensions so that the short channel performances of the devices can be improved due to longer effective gate length.

In MOS device evolution, the Nanosheet FETs with GAA arrangement is considered as the ultimate scalable structure, having superior electrostatic integrity compared to FinFETs [21, 22]. Recently, IBM suggested that the nanosheet gate-all-around FET (NS FET) structure should be the concluding resolution for the ultimate MOS device [22, 23]. Jang et. al. [20] proposed a 2×2 Nanosheet FET of four nanowires connecting the bulk source to bulk drain incorporating both underlap and GAA for a gate length of 10 nm, which performed well with enriched I_{ON} current comparable to the 7 nm technology node as per IRDS. But, the device observes unprecedented leakage current (I_{OFF}) along the gate edges due to the channel being long with underlap and the leakage happening through the side walls, which inducts variety of SCEs such as subthreshold slope, fringing field, and DIBL; thus, the device can no further be upgraded to be at per with the proposed 2 nm technology node of IRDS 2022. Also, this device endures parasitic resistances and parasitic based fringing capacitance that degrades drive current and overall performance therefore, not suitable to provide the desired outcome. Hence, a device providing enriched performance is to be formulated to meet the necessities of IRDS 2022.

Considering these aspects of development and the zeal of having faster switching devices a number of GAAs are acquired with underlap to work together in the form of Nanosheet FET (NS FET) for an enriched ON current with reduced leakage. Further to reach the conceptualized proposal of 2 nm technology node of IRDS 2022, the stack high-k is referred in the NS FET to reduce leakage current by subliming the gate quantum tunneling and is the core focus of this article. Also dicing the possibility to reduce fringing field effects and increased electric-field coupling between the underlap regions and the gate electrode to lower the barrier potential with minimized quantum effects is a requirement, which is analyzed in this article. Thereby, the Stacked high-k Underlap Nanosheet (SU-NS) FET at 10 nm gate length is proposed and developed here for the first time as a promising candidate replacing the regular GAA FET to be the future and even subdue the 2 nm node proposal strands of IRDS 2022. The SU-NS FET is expected to reduce

the gate quantum tunneling, parasitic effects and fringing barrier field while increase the ON current to meet the IRDS 2022 proposed challenge.

2. Device Structure and Theory

Silicon (Si) is the chosen electronic semiconductor material due to its well-established technology and distinctive native oxide. Si electrical devices typically have a 150 °C junction temperature limit. Si chips and power devices must not exceed this temperature. Modern devices cannot use Si due to its low charge transfer and maximum velocity. The pursuit of smaller components has enhanced semiconductor circuit power density during the past decade. Short-channel effects, tunnelling-induced leakage current, high-frequency switching, and smaller device surface area have elevated device mean operational temperatures. High-bandgap alloys might replace silicon. Thus, device scientists target novel materials like SiGe, SiC, and group III-V semiconductors. Group III nitride semiconductors, especially Gallium nitride (GaN) and associated alloys, have drawn attention for their unique properties for 20 years. GaN offers great potential in optoelectronic and high-power device development. GaN has a breakdown field strength of 20 MV/cm [8], stronger than GaAs (4 MV/cm) and Si (3 MV/cm). Additionally, its electron velocity is 3×10^7 cm/s [9], exceeding GaAs and Si (2×10^7 cm/s). The military and commercial application of GaN technology is due to its enhanced electron transport [10-12]. At 14 nm, high-k dielectric [13-18] replaces SiO_2 to limit short channel effects.

Considering this aspect Device C is designed by reducing the channel width to 4 nm, hence underlap width is also reduced and is equal to the channel while Device D is rendered by only reducing the channel height to 4 nm. This allows optimizing the devices B, C, and D, schematically as shown in Fig. 1, for enriched performance based on both the ON and OFF currents. Knowing from literature with introduction of the underlap both ON and OFF current decreases [18] so, increasing the drive current stands as a requirement.

Hence, Device E is developed here with a 2×3 GAA FET horizontal stack composition forming the Nanosheet FET (NS FET) device. This NS FET consists of two layers of Nanosheet each containing three rectangular GAAs with a channel height of 4 nm while length and width are maintained at 10 nm. Thus, the stack of nanosheets, N_{sh}, comprises of each GAA to have wide width, W_{sh}, and height, H_{sh}. For a Nanosheet GAA, the effective channel width is calculated as:

$$W_{eff} = [2H_{sh} + 2W_{sh}] \times N_{sh} \tag{1}$$

It is to be noted that the source-drain bulk of Device E is double in size to that of device C because it uses two sheet layers, so six GAAs are placed between the bulk source-drain. A thickness of 1 nm SiO_2 cannot control gate tunneling and the gate leakage current of device increases resulting in increase of various SCEs in the circuit hence, degrading the circuit stability and device performance [1-3]. Therefore, high-k dielectric materials with a combination of SiO_2 forming a stack at a given equivalent-oxide-thickness (EOT) are used as gate insulators to reduce the gate leakage current [6]. By replacing gate oxide with gate stack system comprising of the high-K dielectrics of HfO_2 with SiO_2 as gate insulators increase physical height of gate keeping the EOT same. For convenience of the new gate oxide in terms of its equivalent SiO_2 thickness the EOT is calculated as:

$$EOT = t_{ox} = \left(\frac{3.9}{K_{high-K}}\right) t_{High-K} \tag{2}$$

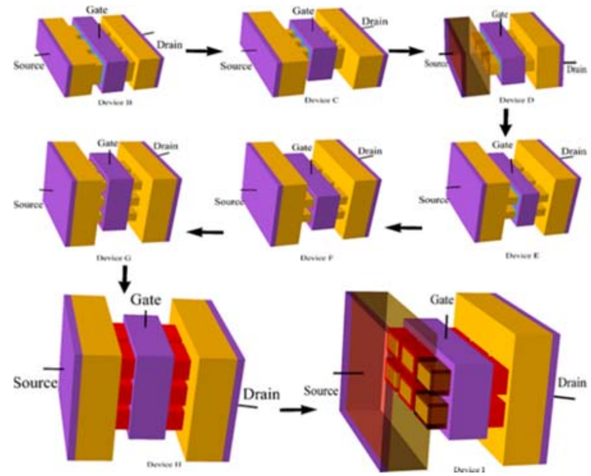


Fig. 1. A 3-D schematic view of Device B – Device I showing the step-by-step development of Stacked high-k Nanosheet FET (SU-NS) FET.

The aim is to develop high-K oxides that allow scaling to maintain low values of EOT of the stack, which is given by:

$$EOT = T_{eq} = t_{High-K}\left(\frac{K_{ox}}{K_{high-K}}\right) + T_{SiO_2}, \tag{3}$$

where K_{ox} is the relative permittivity or dielectric constant of SiO_2 layer. The relative permittivity or effective dielectric constant of the stack is found as:

$$K = \frac{K_{high-k} K_{ox} t}{K_{high-k} t_{ox} + K_{ox} t_{high-K}}, \tag{4}$$

where t is the total physical thickness of the stack.

Kumari et.al [28] investigated the performance of stack high-k material based FinFETs with Si_3N_4, Al_2O_3, ZrO_2 and HfO_2 and observed that the stack with HfO_2 proved to provide lesser leakage currents and healthier short channel performances. Also, the other high-K dielectrics materials available are either expensive or have interface issues with Si based

devices [29], hence HfO_2 based high-k is considered here. The nanosheet devices are consequently expected to provide further improved performances on adding the stack high-k of HfO_2. Here to maintain the physical height of gate a compiled gate oxide thickness of 1 nm is deliberated having SiO_2 and HfO_2 as high-k each with a thickness of 0.5 nm forming Device F with a 3×2 Nanosheet geometry for the first time, which is the upgraded version of Device E as shown in Fig. 1. Now on having Device F with the 3×2 NS FET based construction, Device G is also developed with a 2×3 Nanosheet being a novel geometrical structure having three layers of nanosheets and each sheet of two GAAs. Device G is framed to estimate and analyse performance of the varied dimensional GAA based NS FETs so, the widths of the device is reduced keeping the height fixed in the construction as evidently observed from Fig. 1.

All these devices developed so far are designed with underlap regions to improve the short channel performance, but as identified from literature these underlap regions engulf an additional resistance that increases the total resistance [15, 17-19] of the device acting as parasitic effect while also the fringing [19, 30] fields are created due to the gate electrode, suffices the degradation of the ON current in the device. Even the first timers Device F and Device G, which are expected to provide enriched drive current performance may be prone to these parasitic and fringing effects. Accordingly, a novel concept of wrapping high-k dielectric material of HfO_2 on the underlap regions of both the source and drain sides for each of the GAAs with a thickness of 1 nm is intimidated here for the first time. By this the insulator height on the underlap regions stands equivalent to the stack gate oxide layer, hence the novel device of Stacked high-k Underlap Nanosheet (SU-NS) FET at 10 nm gate length is developed here for the first time. Thus, the concept is engrossed to harness Device H and Device I in 2×3 and 3×2 formats respectively, as the nanosheet devices consisting of six rectangular GAAs arranged in three layer two stack and two layer three stack system with the underlap of each GAA wrapped with HfO_2 (high-k) as clearly shown in Fig. 1.

Further, Device J is deliberated here, which is a simple NS FET of 2×2 rectangular GAA designed for calibration and validation with the existing literature Device K [20] having similar structure with reduced channel height along the underlap, with the details given in Table 1. Also, this comparison validates the development of Device A-G structures in this article. The proposed 2 nm technology node necessities as per IRDS 2022 [13] are considered as shown in Table 1 for comparison on the efficacy of the novel devices (Device H and I) developed here. A multi-channel device increases the drain current as the number of channels increase. The design parameters employed for the devices are listed in Table 2.

The experimentally fabricated device of 26 nm gate length vertically Stacked Gate-All-Around Si Nanowire CMOS Transistor as reported by Ritzenthaler et al. [31] is employed for the purpose of calibrating the Silvaco TCAD tools [32]. The I_D-V_{GS} characteristics of the said device are generated at V_{DS} values of 0.7 V and 0.05 V and their results are observed to closely align with the similar structure device developed here when incorporating the mobility model, as shown in Fig. 2(a). The drift diffusion simulation method and carrier Lifetimes model for constant carrier lifetimes in SRH recombination for impurity concentration are considered here and reflect the first-order impact of confinement on carrier distribution and electrostatics. Hansch quantum effects approximation model for N channel MOS devices, FERMI carrier statistics for electron and holes are invoked simultaneously in this device analysis. Newton and Gummel's methods are also concurrently indebted for mathematical simulation based calculations. The numerical iteration of Newton and Gummel methods are employed by SILVACO for recombination characteristics and to solve differential equations for further analysis of the novel devices developed here for the future era. Therefore, this experimental device serves as a reference for effectively calibrating the electrical properties of the novel GAA devices developed in this study.

Table 1. Device description.

Sl. No	Devices	Device Description
1.	Device A	Rectangular GAA with Underlap
2.	Device B	Three Rectangular Channel GAA with Underlap
3.	Device C	Device B with 4 nm channel width (W:H = 4:10)
4.	Device D	Device B with 4 nm channel height (W:H = 10:4)
5.	Device E	Nanosheet (2×3) GAA
6.	Device F	Device E with stack high-K
7.	Device G	Nanosheet (3×2) GAA with stack high-K
8.	Device H	Device G with HfO_2 wrapped underlap
9.	Device I	Device F with HfO_2 wrapped underlap
10.	Device J	Nanosheet (2×2) GAA (W:H = 10:4)
11.	Device K [20]	Nanosheet (2×2) GAA (W:H = 10:10)
12.	IRDS 2022 [13]	IRDS proposed 2 nm node for 2022

Fig. 2(b) further illustrates the probable fabrication process flow for the novel Nanosheet FET device. The channel region is constructed using epitaxial growth. This multi- channel consists silicon layer and a nanosheet structure, grown to fill the nanosheet space. The channel region is formed by encapsulating the silicon layer with high-k and thereby the gate contact, thus creating an ultra-thin nano regime channel in the

Nanosheet GAA. With the patterned nanosheet/channel structure, including gate and source/drain regions, typically formed using advanced lithography and etching techniques. Then by applying surface functionalization agents or self-assembled monolayers (SAMs) selectively to the gate and source/drain regions. These passivating layers inhibit nucleation of HfO_2 during the ALD process. The underlap region remains unpassivated, preserving its surface reactivity.

Table 2. Parameters used for device design.

Parameters	Dimensions
Source/Drain length, $L_{S/D}$	10 nm
Underlap length, L_U	5 nm
Underlap oxide thickness, T_{UO}	1 nm
Channel length	10 nm
Source/Drain bulk length	10 nm
Oxide thickness, t_{ox}	1 nm
Oxide thickness, t_{ox} (SiO_2-HfO_2)	0.5 nm each
Permittivity of HfO_2	25
Channel doping	10^{15} cm^{-3}
Source/Drain doping	10^{18} cm^{-3}

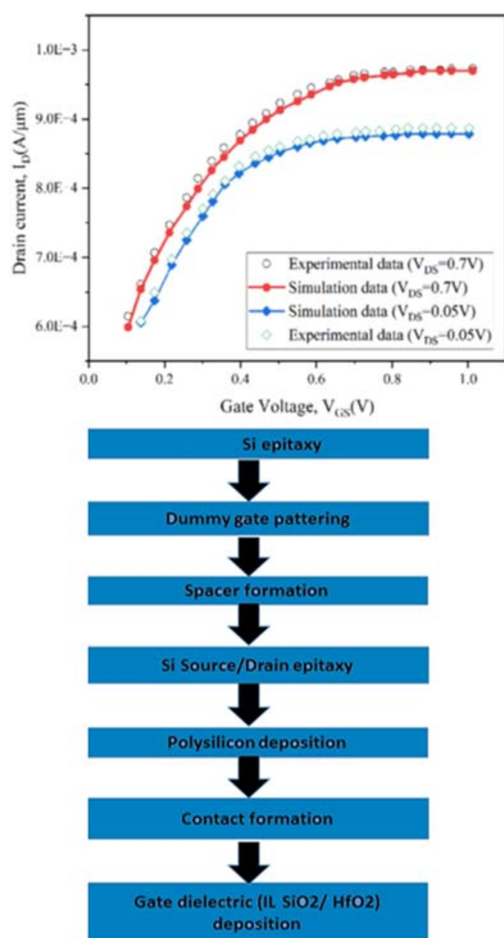


Fig. 2. (a) Electrical parameter fitting for calibration to the experimental data and the physical parameters of the device [31] with I_D-V_{GS} logarithmic graph where V_{DS} represents drain voltage, (b) Fabrication process flow of Nanosheet GAA FET.

The developed 10 nm gate length devices are thereafter compared for enriched performances and analyzed for quantum effect study at nano regime to be implanted further for faster switching operation of the device.

3. Results and Discussion

3.1. Analysis of Electrical Characteristics

The GAA FETs developed here are compared and analysed for the performance and the short channel effects of the devices. The threshold voltages of Device A – I are presented in Fig. 3 with V_{th} varying between ~0.245 V and ~0.295 V. It is observed that the devices with smaller widths have slightly higher threshold voltage as in case of Device G in comparison to Device F. Similarly, Device H has a higher threshold voltage than Device I due to reduced channel width of Device H. As expected, Device H and Device I have higher threshold voltage in comparison to all other devices because of the underlap region wrapping with the high-k (HfO_2).

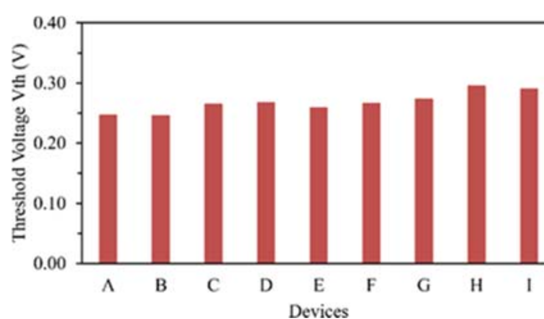


Fig. 3. Threshold voltage variation of Device A – I.

The transfer characteristics (I_D – V_{GS}) of Devices A – D are plotted in Fig. 4 at VDS = 1 V. The ON-state current incorporation of three GAA channels in the device. In Device B, the ON current increases, but the OFF current also increases as observed from Fig. 4 inset resulting in higher subthreshold slope. To reduce this leakage current, Device C and Device D are concurrently developed by reducing channel width and channel height of Device B, respectively. It is pragmatic that the ON current is less in Device C and D than Device B due to decrease in channel dimensions as the space of the channel and underlap region becomes smaller and the carrier flow from source to drain is lessened, but Device C and D probably stand to be the optimized alternatives.

A comparison of the ON currents of the new devices is carried out and presented in Fig. 5(a). Device B showcases enriched ON current in comparison to Device A-D. In Device C and Device D, the ON current is lower than Device B, because the carriers flowing from source to drain through the channel is tapered attributing to reduced channel

dimensions. From Fig. 5(b), the leakage current in Device B seems to increase, which is possibly due to the inculcation of corner effect as the electrons are trapped at four corners increasing the electron concentration. Also, the channel having equal dimensions in Device B leads to enriched gate quantum tunneling, thereby supplementing the leakage current. In Device C and D, the IOFF is reduced due to decrease of channel dimensions as seen in Fig. 5(b). Since the electron concentrations at corners minimize, which is expected to decrease the subthreshold slope according to Vandamme et al. [33]. Considering this aspect of high leakage, Device B is discarded further. In Devices C and D, the parameters such as leakage current (0.13 nA/μm) and subthreshold slope (~63 mV/Dec) are almost same as detected from Fig. 5(b), except the ON current where 4 % increase for Device D as compared to Device C is observed from Fig. 5(a). This occurs due to Device D being a flattened one having increased channel width while narrow devices experience degraded electron mobility according to the resolutions of Wong et al. [34] that the impact of mobility degradation is less for wider devices henceforth, Device D is further considered while Device C is not considered in further analysis.

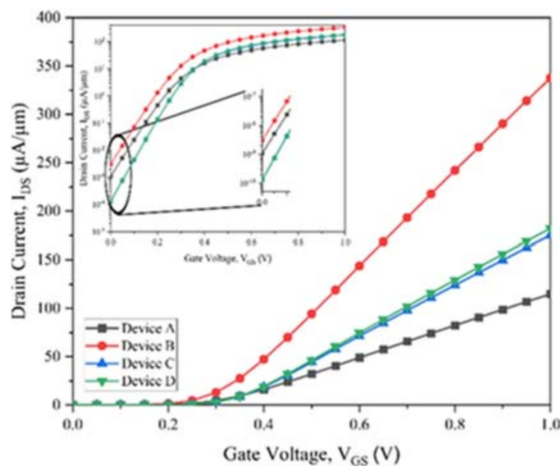
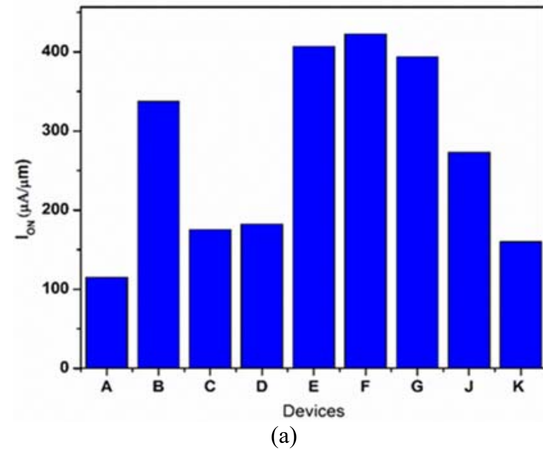
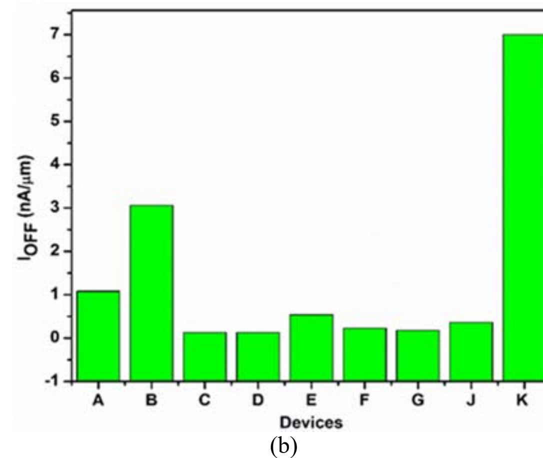


Fig. 4. Transfer characteristics (ID vs VGS) at VDS = 1 V for Device A – D in linear scale focusing ON current and inset depicts OFF current in logarithm scale.

Considering the benefits of Device D, Device E is designed to have twice as many GAA channels as Device D. Thereafter, Device F and G are also developed as discussed in Section II earlier while Device J is a NS FET for calibration and validation of the work and Device K [20] is the existing device. A comparison of ON currents of Device D – G, J and K are also revealed in Fig. 5(a) while the OFF current analysis is done in Fig. 5(b). It is perceived that Device E (2×3 Nanosheet GAA FET) is attaining more ON current (~407 μA/μm) than Device D because Device E has a greater number of channels, so the carriers flowing from source to drain is increased. It is to be noted that Device F is developed from Device E as 2×3 NS FET with stack high-k, which provides nearly same ON current but a much reduced OFF current as detected from Fig. 5(b) due to the incorporation of high-k gate stack oxide system that diminishes the gate quantum mechanical tunneling of electrons through the oxide layer not affecting the inversion channel, so large amount of carriers' flow.



(a)



(b)

Fig. 5. Comparative analysis for the Device (a) ON current and (b) OFF current.

Device G in parallel is also developed as a 3×2 NS FET with high-k to counter Device F. The ON current for Device F and G are ~422 μA/μm and ~394 μA/μm, respectively, as observed from Fig. 5(a). Though both the devices (F and G) use stack high-k as gate oxide, the ON current in Device G decreases due to the decrease in the overall width of the device as per the design seen in Fig. 1 degrading the electron mobility of the NS FET thereby, current conduction decreases in line with the observations of Wong et al. [34]. Device J is observed to have higher I_{ON} in comparison to Device K [20] attributing to lessened channel height. In line with Device F, as perceived from Fig. 5(b), the leakage current in Device G is reduced due to the use of stack gate high-k with increased physical thickness of oxide layer in contrast to Device E. Device D has less ON current and Device E has

higher OFF current due to extensive corner effects and increased gate quantum tunneling at the side walls of NS FET as detected from Fig. 5(a) and (b).

The Nanosheet (NS FET) of Device J provides much lesser leakage current than Device K due to reduced channel height; the leakage through side-wall is decreased and fringing capacitances between channel and underlap region is also reduced. The leakage current of Device K is 7 nA/µm and Device J is 0.36 nA/µm which is much higher than Device F (~0.23 nA/µm) and Device G (~0.18 nA/µm) due to larger leakage current through gate quantum tunneling. Henceforth, Device J and K are not analysed further.

Transfer characteristics (I_D vs V_{GS}) of Device F – I at V_{DS} = 1 V are plotted in Fig. 6(a). The ON currents for Devices H and Device I are observed to be higher as in Fig. 6(a) due to the high-k dielectric wrapping around the underlap regions. This insertion is a novel concept that evidently subdues the parasitic resistances and fringing fields in the devices leading to increased ON current. It is to be realized that the leakage current of the corresponding devices (H and I) is also diminished as devised from Fig. 6(b), directly attributing to the wrapping of high-k on underlap regions thereby reducing the fringing field effects occurring between gate and underlap regions.

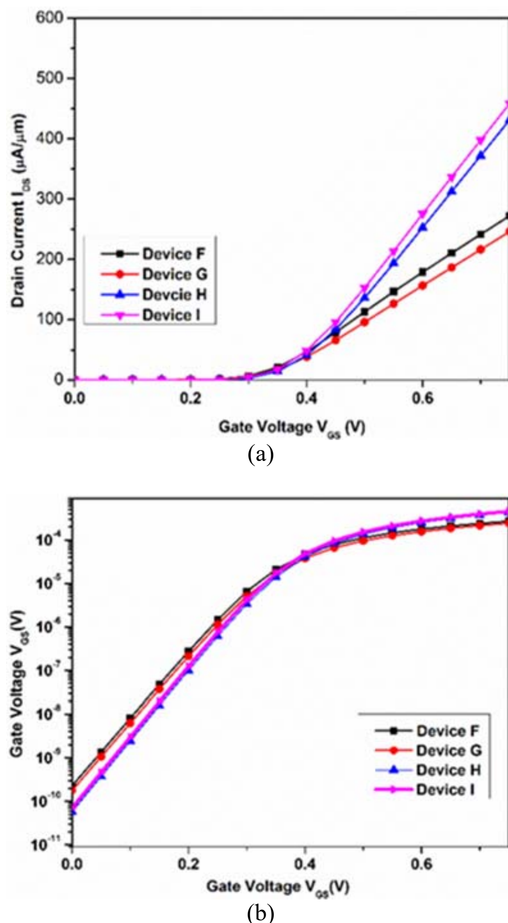


Fig. 6. Comparative analysis for the Device (a) ON current and (b) OFF current.

The ON current in Device H and Device I is ~726 µA/µm and ~757 µA/µm, respectively, as perceived from Fig. 7(a), which is quite high in comparison to Device F and G and also the 2 nm technology data of IRDS 2022 [13] Nanosheet (NS FET) device. The comparison with IRDS node serves as a theoretical guideline rather than an empirical baseline. A 20 % enhancement in ON current in comparison to the IRDS 2022 is clearly resolved from Fig. 7(a). The analysis of OFF current among Device F – I and IRDS 2022 indicate that the leakage current in Device H (~0.06 nA/µm) and Device I (~0.07 nA/µm) are abridged in contrast to the 2 nm technology node data of IRDS 2022 (~0.1 nA/um) [13] due to the introduction of the stack high-k leading to lessened gate quantum tunnelling and reduced fringing field effect between gate and the underlap regions.

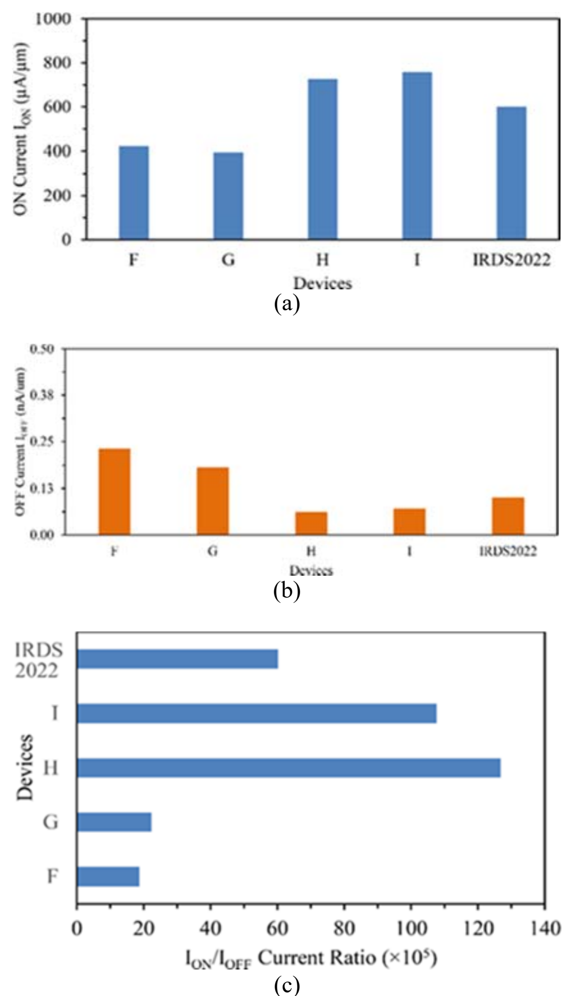


Fig. 7. Comparative analysis for Device F-I and IRDS 2022 a) ON current; b) OFF current; c) I_{ON}/I_{OFF} ratio.

The stack high-k wrapping on underlap minimizes the underlap resistance effect and subdues fringing capacitances, which diminishes the related leakages through the channel edges on source and drain side, thereby enriched performances are achieved. The I_{ON}/I_{OFF} current ratios for these devices are conceded

to estimate the switching performance. Device G (~22.3×10^5) is observed to be better than Device F (~18.7×10^5) having less leakage current as detected in Fig. 7(c). Device H and Device I resolve enormous I_{ON}/I_{OFF} ratio as detected from Fig. 7(c) overtaking all existing literature devices and also the newly devices developed here, which is solely due to the enhancement of ON current and reduced leakage currents attributing to the infusion of stacked gate high-k and the gate underlap region wrapping for the devices. The switching ratio (I_{ON}/I_{OFF}) for Device I and H are ~126×10^5 and ~10^7×10^5, which are enriched by 83 % and 82 % in comparison to Device F and G, respectively. The total device width of Device I is less in contrast to Device H so the mobility decreases leading to a drop in ON currents so the ION/IOFF ratio is higher for Device H. Thus, the analysis led to the evolution of novel devices with superfast switching required for next generation devices.

Short channel effects such as subthreshold slope and DIBL of all the devices are analysed and compared as shown in Fig. 8 and are observed to slowly reduce and be same along with the device structures developed here. Device F – K and IRDS 2022 data employs use of high-k material as gate oxide to reduce the OFF current so subthreshold slope (SS) and correspondingly DIBL decreases, except for Device K [20] which is in unrest condition due to high fringing field and capacitances as perceived from Fig. 8(a) and (b). Device F and Device G have similar SS of ~64 mV/decade while DIBL are ~24 mV/V and ~30 mV/V, respectively. Due to the incorporation of the high-k wrapping on gate underlap regions the subthreshold slope in Device H and Device I is ~61.30 mV/Dec approaching ideal condition shown in Fig. 8(a) and DIBL is ~4.66 mV/V and ~14.31 mV/V, respectively, which is extensively improved when compared to all other devices as witnessed in Fig. 8(b) subjected to the reduced fringing effects and gate quantum tunneling. In addition, due to the reduced device width, DIBL of Device H is recorded to be quite less at only ~4.66 mV/V. Hence, supplementing towards performance enrichment and provides support to attain enhanced switching speed for the device.

Further, the transconductance of Device F-I are acquired and presented in Fig. 9(a) while the output conductance and the output resistance are displayed in Fig. 9(b). Huge gm is resolved for both Device H and I due to reduced fringing effect caused for the gate underlap region wrapping leading to condensed parasitic in the devices. The detailed variations of all the performance parameters are tabulated in Table 3, thereby indicating the enriched device for the future, which is also the probabilistic future device outperforming the 2 nm technology node data of IRDS 2022 [13] requirements. The augmented Ion/Ioff current ratio with near ideal SS of ~61 mV/Dec and reduced DIBL for Device H and I evidently symbolize the SU-NS FET as the futuristic next generation devices suitable for the semiconductor industry with faster switching speed in comparison to others.

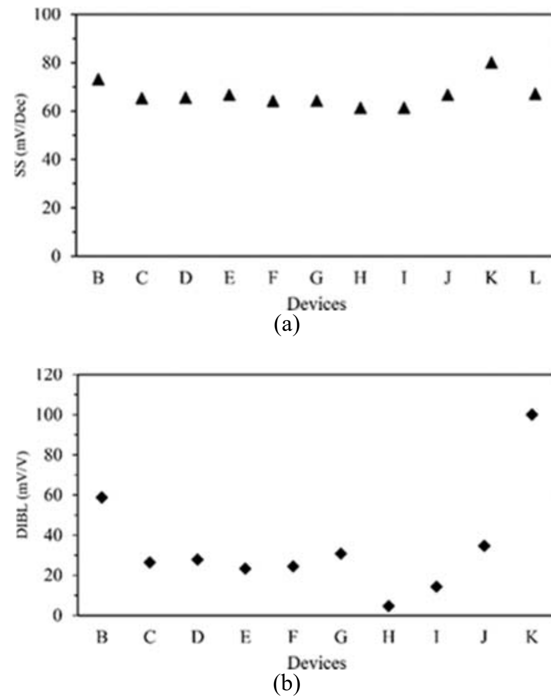
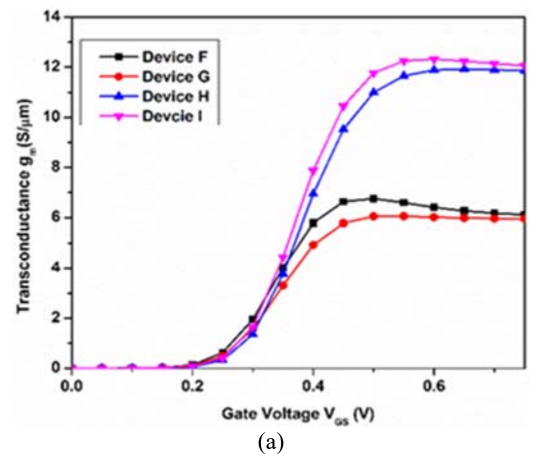


Fig. 8. (a) Comparison of subthreshold swing for Device B – K and IRDS 2022. (b) DIBL for Device B – K are compared.



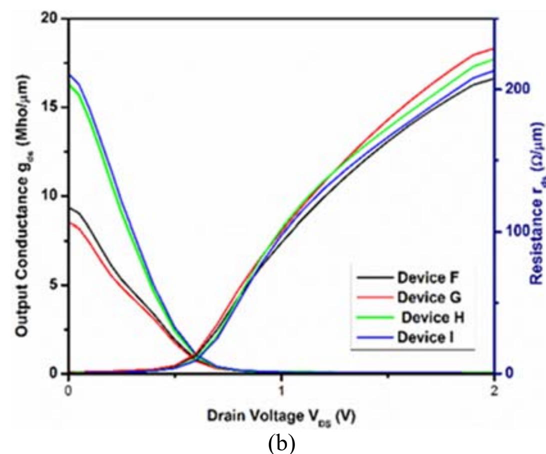


Fig. 9. (a) Transconductance of the Device F-I (b) Output conductance and output resistance of Device F-I.

Table 3. Comparative analysis of all the devices.

Devices	V_{th} (V)	I_{ON} (µA/µm)	I_{OFF} (nA/µm)	I_{ON}/I_{OFF} x 10^5	SS (mV/Dec)	DIBL (mV/V)
A	0.246	114.88	1.08	1.07	73.39	62.70
B	0.245	337.52	3.06	1.10	73.06	58.77
C	0.264	175.27	0.13	13.78	65.26	26.36
D	0.267	182.30	0.13	13.55	65.48	27.86
E	0.258	407.07	0.54	7.58	66.62	23.26
F	0.266	422.78	0.23	18.73	64.14	24.30
G	0.273	394.00	0.18	22.32	64.17	30.05
H	**0.295**	**726.24**	**0.06**	**126.80**	**61.30**	**4.66**
I	**0.290**	**757.38**	**0.07**	**107.67**	**61.27**	**14.31**
J	0.258	273.00	0.36	7.57	66.65	34.63
K [20]	--	160.00	7.00	0.23	80.00	100.00
IRDS 2022 [13]	0.271	602.00	0.10	60.20	67.00	--

The output performance characteristics of Device F – I are measured at V_{GS} = 0.8 V and publicized in Fig. 10 realizing that the drain current of Device F and Device G are ~309 µA/µm and ~282 µA/µm, respectively. In SU-NS FETs (Device H and I) the drain current increases due to the negation of the source and drain underlap parasitic resistance and the reduction of the fringing field capacitances by wrapped the high-k on gate underlap regions. The drain current output performance of Device I and H are enhanced by 41 % and 43 %, respectively, in comparison to Device F and G while a slight difference is observed between Device H and I and in Device G and F attributing to the total device width. As reduced width is instituted for Device G and Device H decrease in the carrier flow from source to drain occurs due to corner effect at the premises of the devices, thereby the performance is slightly cut short. But, still commissioning the analysis both the novel SU-NS FETs (Device H and I) provide an overwhelming performance on comparing with all the other devices. Hence, both Device H and I are inevitably in a position to challenge and meet the requirements stated by IRDS 2022 [13] for the 2 nm technology node.

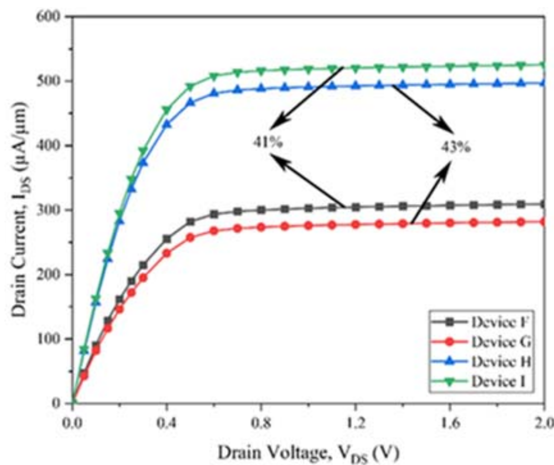


Fig. 10. Output performance characteristics (ID vs VDS) at VGS = 0.8 V of Device F – I.

Based on this analysis, Device H and Device I thus provide enriched ON current by minimizing the parasitic resistances and capacitances, decreases the leakage current by indulging gate quantum tunneling and reduces the short channel effects of subthreshold swing and DIBL by subduing the fringing field capacitances with underlap wrapping. Hence, Device H and Device I are observed to be the most effective and suitable device for faster speed and switching operations with enhanced performances and well ahead of the requirements of IRDS 2022 2 nm technology node.

3.2. Analysis of Quantum Effects

Nanosheet FETs developed here conspire with gate underlap regions on either side of the channel connecting the source and the drain, thereby incorporates gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{dg}). The major components of these capacitances are the channel to underlap parasitic capacitance and the gate to underlap fringing capacitance. Jang et al. [20] though developed the 2×2 NS FET (Device K) which operates at par with the 5 nm technology node of IRDS 2022 have huge leakage along the gate edges due to these parasitic and fringing capacitances at both source and drain sides. Considering these aspects, fringing electric fields also acts from the gate through the underlap regions. Hence, the novel SU-NS FET that are developed here as Device H and I having high-k wrapping the underlaps to reduce the fringing and parasitic effects. Commissioning to this aspect the electric field is cordoned so as not to penetrate the channel and disrupt the flow of carriers that induces leakage currents. This is evidently observed from Fig. 11(a) disseminating the field through the gate oxide enduring saturated lateral electric field while low leakages are already observed in Table 3. Also, the electric field is detected to be high in the source side underlap than the drain side due to the impact of fringing field and the source being grounded during device operation.

The electron velocity contour is shown in Fig. 11(b), which sustains increased velocity in the

underlap regions. Due to the grounded source a higher consortium of fringing field acts at gate to source underlap, hence the electrons are initially accelerated at the source with high electron velocity and decreases in the channel. Again, due to fringing field on drain underlap a slight increase is observed. The overall electron velocity in Device H and I are observed to be much higher than the saturated velocity in the order of ~30×107 cm/s in channel region as in Fig. 11(b).

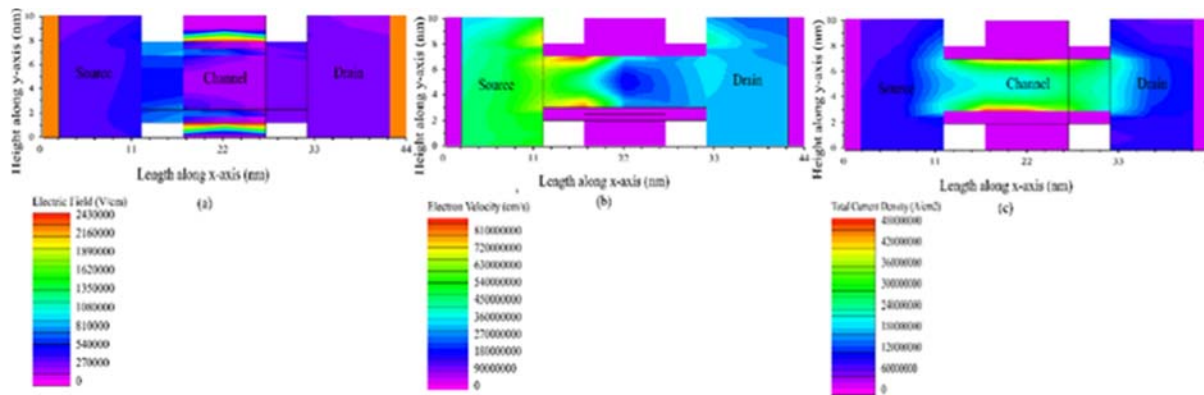


Fig. 11. Contours of a) electric field b) electron velocity c) total current density.

In Device I the stack high-k gate on the channel and the wrapping of the gate underlaps reduce the gate quantum tunneling and fringing capacitances leading to controlling the related parasitics. The dielectric constant for HfO_2 material makes its permittivity high, due to which the field strength at a given voltage alters the spatial distribution of the electric field lines.

This change reduces the extent to which the field lines fringe out to the source and drain regions, thereby reducing fringing capacitance and related parasitic effects. Hence, the flow of charge carriers from source to drain avoiding current charge accumulation at edges of nanowires by reducing the overall capacitance is evidently observed from the current density contour of Fig. 11(c) while showcasing an overcall drive current enhancement for the device.

The current density across the channel region is further shown in Fig. 12 and it is observed that the current density is more in all side than the center of the channel because of applied gate voltage and the electron concentration is increased below the oxide layer so the current density is high. Current density is more at the corners than at the sides due to trap of electrons at the corners increasing electron concentration. In this Nanosheet (NS FET) device the mobility degradation in the width side is due to surface roughness scattering, which is directly attributed to the imperfect interface between materials, phonon scattering and surface orientation. The electron concentration is decreased at the edge of the width side so the current density also decreases.

4. Conclusion

The transitions from a single rectangular GAA FET with underlap to a Nanosheet (NS FET) device design featuring six nanowires in stacked configuration is developed here. The GAA Nanosheet FET is further optimized by varying dimensions, using a high-k dielectric gate stack in the insulating layer, while also incorporating high-k (HfO_2) for wrapping the gate underlap region of the device. The Nanosheet FETs with equal channel dimensions deliver high ON current while also exhibit increased leakage current. To address this, reducing the channel dimensions mitigates leakage current and enhances short-channel effects, albeit at the cost of reduced ON current. Therefore, to optimize and develop a novel device a series of devices are developed from Device A to Device I. To boost the ON current, designs with increased channel numbers, such as 2×3 and 3×2 Nanosheets are introduced, which enhance ON current while maintain improved short-channel characteristics. The devices (H and I) are developed in two-layer horizontal sheet shows better ON current performance, whereas two-layer vertical sheet devices excel in improving short-channel effects. In addition, stack high-k gate is used to increase drain current and further enhances short-channel performances. Adding high-k material to the underlap region significantly improves ON current, reduces leakage current, and enhances short-channel effects by controlling the fringing field effect and the parasitics. The Devices H and I demonstrate ON currents of 726 µA/µm and 757 µA/µm, respectively, exceeding the 2 nm technology node data of IRDS 2022 benchmark of 602 µA/µm. Leakage currents are 60 pA/µm and 70 pA/µm, significantly below the IRDS data of 100 pA/µm. The subthreshold swing for both Device H and I are ~61.30 mV/dec and approaches the ideal value, while the DIBL of ~4.66 mV/V and ~14.31 mV/V are acquired, thus outperforms all other devices. This evidently highlights the superior performance of the novel Nanosheet (SU-NS) FET devices evolved here that are ready for high-speed operation and therefore stand as the future device of the semiconductor industry.

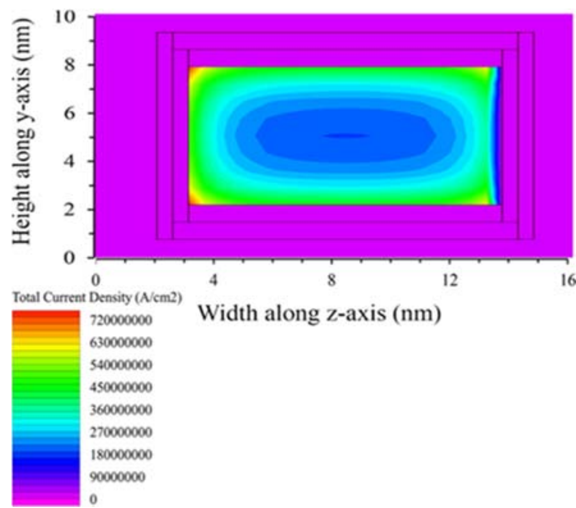


Fig. 12. Contour of total current density across the channel region for Device I.

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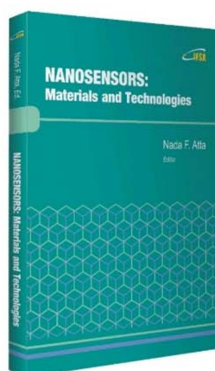

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