MicDAT 2022

Microelectronic Devices and Technologies

Proceedings of the 4rd International Conference on Microelectronic Devices and Technologies (MicDAT '2022)

21-23 September 2022

Corfu, Greece

Edited by Sergey Y. Yurish

IFSA Publishing

Sergey Y. Yurish, *Editor*
Microelectronic Devices and Technologies
MicDAT '2022 Conference Proceedings

E-mail (for orders and customer service enquires): ifsa.books@sensorsportal.com

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ISBN: 978-84-09-43856-3
BN-20220915-XX
BIC: TJFD

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Foreword

On behalf of the MicDAT' 2022 Organizing Committee, I introduce with pleasure these proceedings devoted to contributions from the 4th International Conference on Microelectronic Devices and Technologies (MicDAT '2022), 21-23 September 2022. The conference is the fourth of a series of annual International Conferences on Microelectronic Devices and Technologies (MicDAT) held in Barcelona (Spain) in 2018, Amsterdam (The Netherlands) in 2019 and 2020 (virtual format). The conference is organized by the International Frequency Sensor Association (IFSA) in a technical cooperation with our sponsors IFSA Publishing, S.L., (Barcelona, Spain) and media partners - MDPI 'Micromachines' (ISSN 2072-666X) and 'Low Power Electronics and Applications '(ISSN 2079-9268)' open access journals (Switzerland).

The conference program provides an opportunity for researchers interested in microelectronics to discuss their latest results and exchange ideas on the new trends and challenges. The main objective of the MicDAT' 2022 conference is to encourage discussion on a broad range of microelectronics related topics and to stimulate new collaborations among the participants.

The proceedings contains all papers presented at the conference. We hope that these proceedings will give readers an excellent overview of important and diversity topics discussed at the conference.

We thank all authors for submitting their latest work, thus contributing to the excellent technical contents of the conference. Especially, we would like to thank the individuals and organizations that worked together diligently to make this conference a success, and to the members of the International Program Committee for the thorough and careful review of the papers. It is important to point out that the great majority of the efforts in organizing the technical program of the conference came from volunteers.

Prof., Dr. Sergey Y. Yurish
MicDAT' 2022 Chairman

(005)

Negative Voltage Analysis Model for Evaluation on Control IC Driving of MOSFET Application

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Summary: In power converter applications, MOSFETs are used as switches to control the value of current or voltage and the control ICs are used to drive and control the MOSFET turn on/off to achieve high-frequency switching. In general, the absolute maximum negative voltage rating of the driving pin at these control IC is not sufficient and the driving pin would be damaged by negative voltage which would be induced as MOSFET switching off. The main purpose of this paper is to use the analysis model to evaluate and find out the parameter of MOSFET which leads to the control IC damaged.

Keywords: Parameters of MOSFET, Control IC, Gate drive, Negative voltage.

1. Introduction

In many of switching power supply and DC/DC converter applications, the gate drive pin of the control IC would be damaged by the negative voltage over the maximum rating. The driving of the power MOSFET is related to the switching speed of the turn-on/off in the switching power supply design. It needs to be considered the characteristic of the MOSFET and the capability of the gate driver at the same time [1-5]. Due to the parasitic inductance of the MOSFET lead and PCB circuit trace, the reverse recovery time (T_{rr}) and the reverse recovery charge (Q_{rr}) of MOSFET's parameters could generate the negative voltage by high current deviation [6-8].

2. Implementation of Circuit

Among circuitry topologies for the switching power supply, LLC converter is usually chosen as the main DC/DC topology, shown as Fig. 1. The S_1 and S_2 are the high voltage MOSFETs of half bridge and configured to output the square wave voltage. The low voltage MOSFETs S_3 and S_4 are the power switches of the secondary side synchronous rectifier to minimize power loss.

2.1. Gate Resistor

The switching speed of the turn-on/off is related the parasitic capacitance of the MOSFET and gate driving circuit [9-11]. The basic driving circuit is shown as Fig. 2. The resistor R_{gs} is to make the gate-source voltage down to 0 V while the gate-source voltage is open. Therefore, we recommend placing 10 kΩ ~ 100 kΩ resistor for reducing malfunction of the switch. The resistors R_{g_ext} and R_g and the input capacitance would affect the switching speed and the switching loss. For external R_{g_ext} selection to reduce switching loss, the following equation is recommended for the setting of V_{gs} rise/fall time by 5-time constants:

$$t_{rise/fall} = 5 \times (R_{g\_ext} + R_g) \times C_{iss}, \quad (1)$$

where C_{iss} is the input capacitance. R_g is the internal gate resistor. R_{g_ext} is the external resistor to change the switching speed for efficiency or EMI optimization in the gate drive circuit. From Potens' experience, we choose: where C_{iss} is the input capacitance. R_g is the internal gate resistor. R_{g_ext} is the external resistor to change the switching speed for efficiency, thermal or EMI optimization in the gate drive circuit [12, 13]. From Potens' experience, we choose:

$$\frac{t_{period}}{t_{rise/fall}} \geq 50, \quad (2)$$

where t_{period} is the period (cycle duration). The relation of the period and the switching frequency f_s is:

$$t_{period} = \frac{1}{f_s} \quad (3)$$

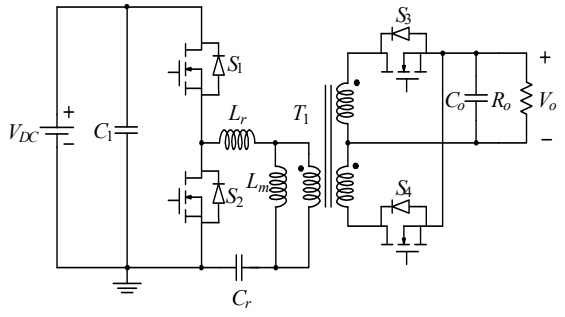

Fig. 1. The LLC converter for application.

From equation (1) to (3), R_{g_ext} can be expressed as below:

$$R_{g\_ext} \leq \frac{1}{250 \times f_s \times C_{iss}} - R_g, \quad (4)$$

We can use equation (4) to determine the suitable external resistor for the gate drive circuit.

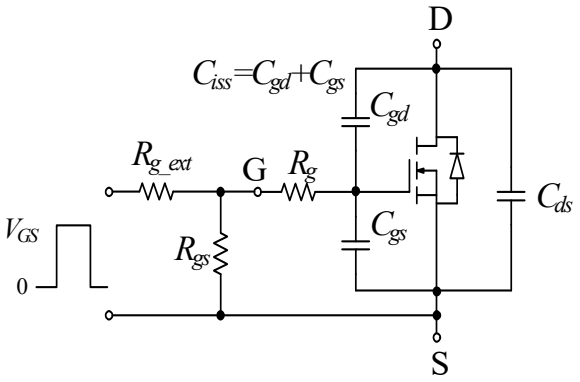

Fig. 2. The basic gate drive circuit.

2.2. Negative Voltage Analysis Model

The gate drive circuit loop with parasitic inductance (L_{p1}), the gate drive voltage (V_{GS}), the gate drive resistor (R_g), the gate drive resistor voltage (V_R), the gate drive current (I_g), and gate to source voltage (V_{gs}) are shown in Fig. 3.

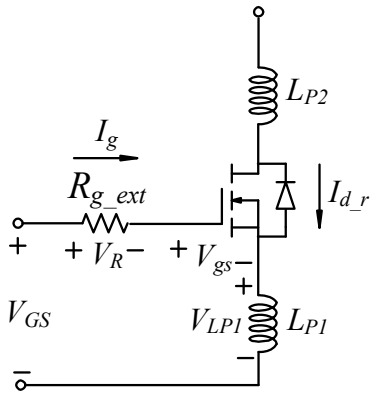

Fig. 3. The gate drive circuit with parasitic inductance.

In reverse recovery related period, I_{dr} is defined as the current of body diode. Fig. 4 is the relation between the reverse current of body diode and the voltage of parasitic inductance. The I_{RM} is the maximum reverse current of body diode, t_{rr_P} is the period of the positive induced voltage and t_{rr_N} is the period of the negative induced voltage. Therefore, the magnitude of the negative voltage can be derived as

$$V_{LP1} = L_{P1} \times \frac{dI_{d_r}}{dt} = \\ = L_{P1} \times \frac{0 - I_{RM}}{t_{rr\_N}} L_{P1} \times \frac{I_{RM}}{t_{rr\_N}} \quad (5)$$

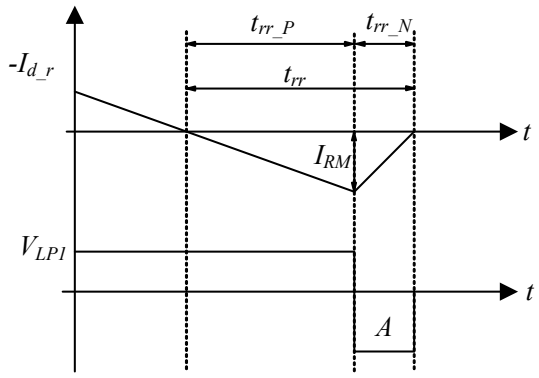

Fig. 4. Relation between the Id current and the voltage.

The relation of the reverse recovery charge, the reverse recovery time and the maximum reverse current is shown as

$$Q_{rr} = \frac{1}{2} I_{RM} \times t_{rr}, \quad (6)$$

The duration of the negative voltage means the energy stress on the gate drive pin of the control IC. The more duration the negative voltage sustains; the more control IC will be damaged. And we can drive the negative voltage energy as

$$A = |V_{LP1}| \times t_{rr\_N} \quad (7)$$

Substitute equation (5) and (6) into (7), we can derive the area of the negative voltage energy as

$$A = 2 \times L_{P1} \times \frac{Q_{rr}}{t_{rr}} \quad (8)$$

The equation (8) means that the energy might damage the IC is related to the ratio of the reverse recovery charge and the reverse recovery time.

From the above relation, we can establish the negative voltage analysis model considers the influence on the gate drive circuit and MOSFET equivalent circuit. The MOSFET parameters such as R_g, T_{rr} and Q_{rr} are as inputs of model and the parasitic parameters are assumed as another inputs of model. By this analysis model, we can obtain the negative voltage as the output and estimate the influence of the negative voltage on the gate drive pin of the control IC from this model. Fig. 5 is the negative voltage analysis model. In gate drive circuit, the gate drive voltage can be derived as

$$V_{GS} = V_{L_{P1}} + V_R + V_{gs} = \\ = L_{P1} \times \frac{dI_{d\_r}}{dt} + V_{gs} + I_g \times R_g \quad (9)$$

When the gate drive resistor is increased, the magnitude of the negative voltage is decrease as the following relationship:

$$R_g \uparrow \Rightarrow |V_{GS}| \downarrow \quad (10)$$

From above relation, the smaller the negative voltage is, the smaller the energy is. Therefore, the possibility for IC damaged is being low.

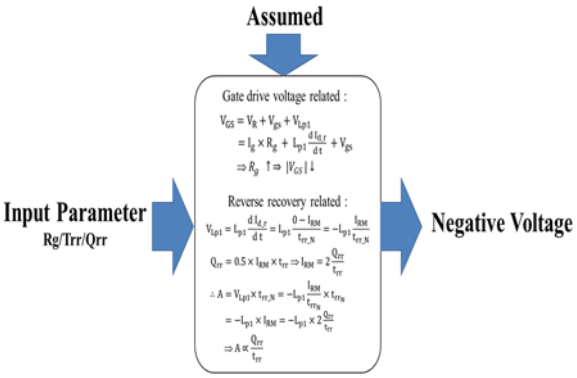

Fig. 5. Negative voltage analysis model.

3. Verification Based on Experimental Result

To demonstrate the effectiveness of the proposed, a 300 W LLC converter platform is chosen for demonstration. The operation principle of the proposed approach is experimentally implemented and verified through LLC converter platform utilizing secondary side synchronous rectifier. Fig. 6 is the prototype of LLC converter with driving, feedback circuit. The main component selection and circuit parameters are given in Table 1 [14].

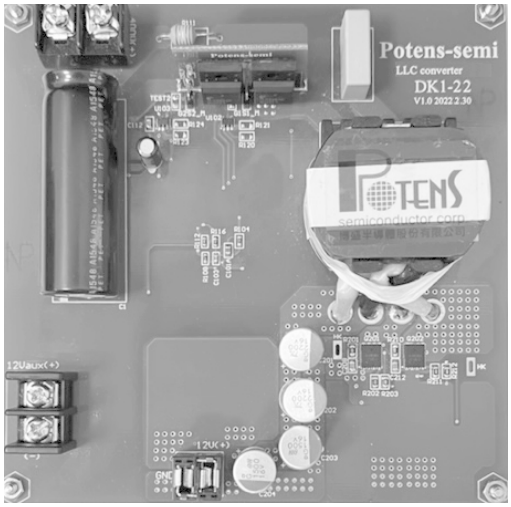

Fig. 6. Proposed circuit board.

Fig. 7 shows the turn on waveforms of the PDEC69F0BX-5 that Rg is 96 Ω, and Fig. 8 shows the turn on waveforms of the PDC6988BX-5 that Rg is 0.9 Ω. The result shows that a larger Rg will have a smaller negative voltage [15, 16]. We take three different MOSFETs as example. The measurement data of these three MOSFETs and the calculation results are shown in Table 1. From the Table 2, we could conclude that the result 3 with ratio of the reverse recovery charge and the reverse recovery time is the highest possibility to damage the gate drive pin of the control IC.

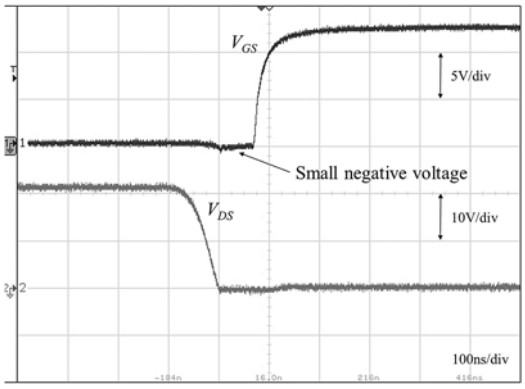

Fig. 7. The turn on waveforms of PDEC69F0BX-5.

Table 1. Parameters of main circuit.

Parameter	Value	Description
C_1	220 uF	450 V electrolytic capacitor
S_1, S_2	PJF14N65N	650 V, 14 A, SJ MOSFET
T_1	L_m = 600 μH, L_r = 100 μH	CC33, N_p: N_{s1}: N_{s2} = 34:2:2
C_r	68 nF	1 kV film capacitor
S_3, S_4	PDEC69F0BX-5/ PDC6988X-5	60 V MOSFET
C_o	1500 uF × 4	16 V electrolytic capacitor

Table 2. MOSFET parameters and negative voltage.

No.	t_{rr} (ns)	Q_{rr} (nC)	I_{RM} (A)	t_{rr_N} (ns)	V_{Lp1} (V)	$A=\lvert V_{Lp1} \times t_{rr\_N}\rvert$ (V·ns)	$\frac{Q_{rr}}{t_{rr}}$
Result 1	229.6	1946	16.95	40.45	-4.19	169.5	8.5
Result 2	244.1	2139	17.52	58.2	-3.01	175.2	8.8
Result 3	254.9	2300	18.05	50.3	-3.58	180.1	9

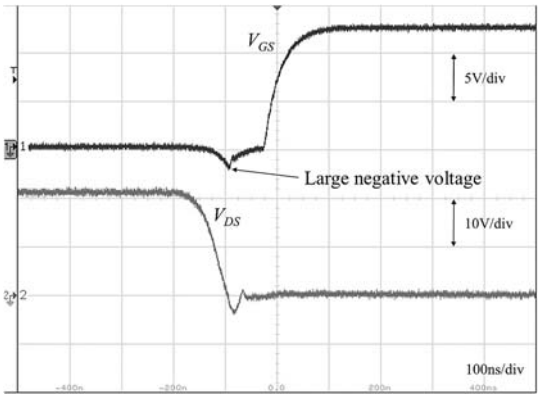

Fig. 8. The turn on waveforms of PDC6988BX-5.

4. Conclusions

This paper shows an analysis method to evaluate the influence of the negative voltage caused by the parasitic inductance of the MOSFET lead and PCB circuit trace and to impact on the drive pin of the control IC. The reverse recovery time is also the

highest possibility to damage the gate drive pin of the control IC. The more duration the negative voltage sustains, the more possibility that the control IC will be damaged. However, we could reduce the negative voltage drop at the gate drive pin by increasing the gate drive resistor.

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Gallium Nitride Trench FET Development

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Summary: In this paper, we report on device and epitaxial process developments for realization of vertical gallium nitride field effect transistors on a silicon carbide substrate. Physical based Technology Computer Aided Design (TCAD) models are employed to propose a wafer stack, dimensions and doping levels for a gallium nitride epitaxy to achieve a normally-off device with a specific on-resistance of $R_{sp,on}$ = 1.4 mΩ.cm^2 and blocking voltage capability of BV = 540 V. In addition, electrical performance of the first generation of manufactured GaN-on-SiC devices is presented.

Keywords: GaN, FETs.

1. Introduction

Gallium Nitride (GaN) based devices enable highly efficient and more compact conversion systems compared to conventional silicon counterparts [1-6]. All commercially available GaN power devices are lateral. However, for medium and high-power applications vertical devices are more desirable. This will allow reduced dimensions, bring uniform heat generation/dissipation, avoid dynamic on resistance and improve reliability [1]. For feasibility reasons, GaN vertical devices need to be grown on a foreign substrate. Therefore, a substrate with a lower lattice mismatch is desirable [1]. For a commercial success, there needs to be compelling reasons to utilize GaN on silicon carbide (SiC). In this paper, epitaxial growth and device fabrication steps of a vertical GaN-on-SiC structure are presented for 200-600 V class applications.

2. Device Structure and Simulation Results

We target design and specification of vertical GaN trench Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). We grow $Al_xGa_{1-x}N$ layers on top of an n-type SiC substrate by MOCVD. The designed wafer stack comprises 20 nm n + GaN ($10^{19}\,cm^{-3}$), 200 nm n-GaN ($5 \times 10^{18}\,cm^{-3}$), 400 nm p-GaN ($2 \times 10^{17}\,cm^{-3}$), 4 µm n-GaN ($2 \times 10^{16}\,cm^{-3}$), 1 µm n + GaN ($10^{19}\,cm^{-3}$) and 1 µm buffer layers grown respectively on a SiC substrate. Fig. 1 is the predicted output characteristics of a fully vertical GaN with 5.6 µm of gallium nitride epi layers on top of a 1 µm buffer at different gate biases. The simulation methodology and complete device structure were given in [1].

3. P-type Doping in GaN Stack

P-type doping is achieved by utilizing Magnesium (Mg) atoms in gallium nitride material. It is well known that reaching a high level of active Mg dopants is challenging in a wide bandgap.

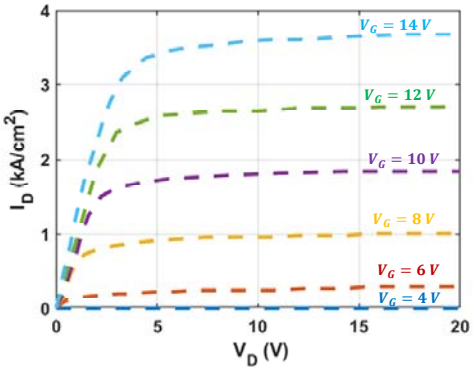

Fig. 1. Predicted family of curves (I_D-V_{DS}) for proposed design employing Nickel for gate metal and interface state of FC = $1.5 \times 10^{12} cm^{-2}$ between GaN and dielectric.

Fig. 2 is a complex doping profile of Mg in GaN. The intentional doping was meant for the upper 0.4 µm of the epitaxy. However, migration back into nominally undoped GaN is clearly observed. This is found to be dependent on the growth process.

4. Trench Development

The quality of the trench plays an important role in vertical device performance. According to our simulations, best performance is obtained with

90 degrees side walls without micro trench and with rounded corners. Fig. 3 shows the SEM image of a dielectric deposited on surface after trench was formed.

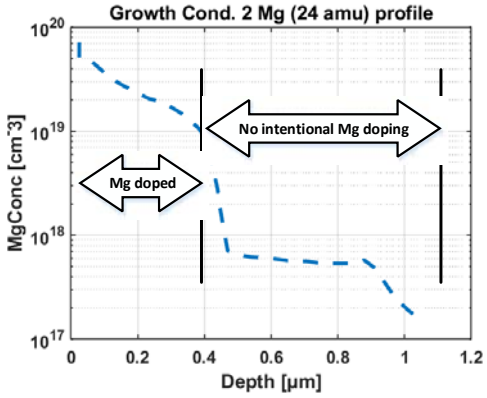

Fig. 2. SIMS data showing complexed migration of Mg back into underlying layer.

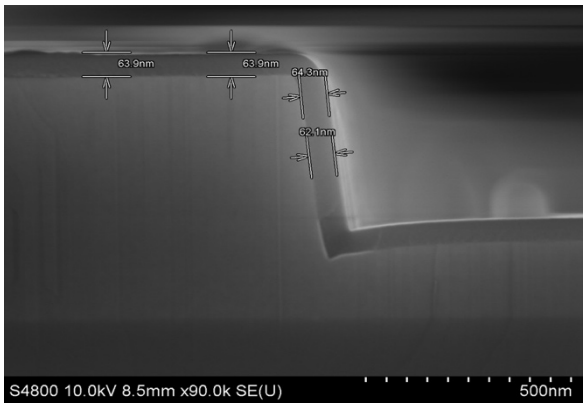

Fig. 3. SEM images of dielectric deposition on GaN showing highly conformal film.

5. First Generations

Fabrication process stars with 1 µm deep etch for gate contact using a hard mask. Etched surfaces are smoothed by TMAH treatment. RTA is performed to activate remaining p-GaN layers at side walls. SiO_2 was deposited to form a gate oxide. Ti/Au forms the contacts.

Fig. 4 is the microphotograph of manufactured vertical GaN on SiC substrate and Fig. 5 is its transfer characteristics. The threshold voltage is larger than expected due to the quality of gate contact, its dielectric and existence of interface states. Results are fed into next round of material growth and device fabrication to achieve the desired performance.

6. Conclusions

We present major steps of developing vertical gallium nitride FETs. The initial work shows promising results to achieve a low specific on-resistance of $R_{sp,on}$ = 1.4 mΩ.cm^2 and high voltage blocking capability of BV = 540 V. These are important steps towards future commercialization of vertical GaN-on-SiC for medium to high power applications.

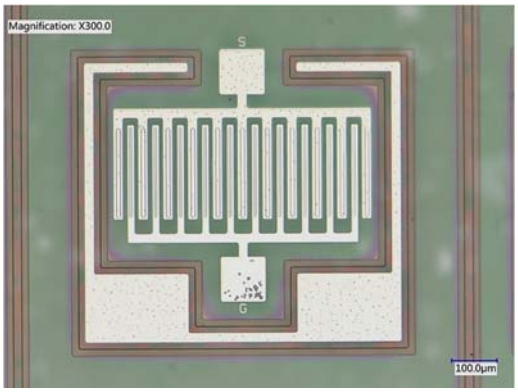

Fig. 4. Micro photograph of first generation of manufactured vertical GaN on SiC substrate with 10 fingers. Gaps between source and drain fingers are 10 µm. Trench is 10 µm wide. Fingers are 20 µm wide.

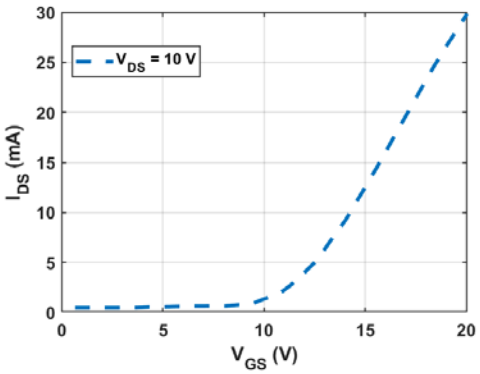

Fig. 5. Measured transfer characteristics (I_D-V_{GS}) of first generation of manufactured vertical GaN-on-SiC device at V_{DS}=10 V and room temperature.

Acknowledgements

This work is part of Gallium Nitride Trench-FET Development for Automotive Power Applications (GaNTT) project funded by Innovate UK.

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Nanostructured Zincite Thin-films Modified with Squaraines for Solar Energy Harvesting

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Summary: Solid state solar cells (SC) of the newer generations are multilayered thin-films. Their high efficiencies and performance rely on the successful generation and extraction of electron-hole pairs from the photoactive layer trough electron and hole transport layers toward the electrodes. Multilayer thin-films allow vast number of upgrades but with one major drawback which is the mutual dependency of the constituting layers. Possible ways of improving the SC efficiency are the use of novel absorbing materials, like squaraine (SQ) dyes, that are easy to synthesise, have high absorption coefficients with tuneable bandgaps and are very stable; or the use of nanostructured electron transport layers (ETL) like zincite that can improve the charge carrier generation and separation, or preferably both. In that case, the remaining concern is the demystification of the charge carrier transfer pathways with respect to aforementioned mutual dependency of the constituents. In this work, we try to find and utilise the appropriate tool to evaluate the influence of the SQ layer in combination with the nanostructured ETL zincite on some of the critical functional aspects of hybrid-organic SC. For the purpose specially configured atomic force microscope (AFM) was used.

Keywords: Squaraine dyes, Tunable bandgaps, Thin-films, Nanostructured zincite, Solid-state solar cells, Atomic force microscopy.

1. Introduction

Solar cells aim to cost below 0.1 € for 1 W of solar electricity and maintain stable, flexible, efficient and eco-friendly. Organic photovoltaics (OPV) are cheap and considerably stable, allow flexibility and don't pollute. While fully organic absorbing layers can allow further price drop and environmental upgrades as they withhold from common use of metal-based absorbing-layers, they don't reach high efficiencies like perovskite solar cells (PSC). Hybrid-organic photovoltaics (H-OPV) maintain OPV benefits but narrow down the limitations gap. In addition to compositional aspects, when designing the constituting materials, the size of the domains plays an important role. For some constituents it may be demanding to control the degree of polymerisation and purity as well as to achieve reproducible interfacing and grain growth due to the strong precursor-batch dependence [1]. On the contrary, the use of simple absorbing chemicals facilitates the process and favours reproducibility, but such systems can hardly follow the demands of the 3rd generation of SC. In between, we find small molecules, intrinsically without such flaws, having sufficient complexity to allow desired 3rd generation SC functionality while having molar mass defined and low enough to allow reproducibility and simple interfacing.

Dihydroxycyclobutenedione (squaric acid) was first synthesized by Cohen et al. in 1959 [2]. Squaric acid can be used to easily derive molecules forming π–acceptor–π systems within, commonly known as squaraines (SQ) (Fig. 1). This group of small molecules (in solid-state) yield distinctive intense (and relatively sharp) absorbance or fluorescence in the red-VIS spectra and extremely high molar extinction coefficients, thereof are ideal candidates for solar energy application.

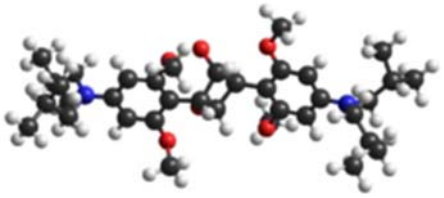

Fig. 1. 3D molecular structure of the synthesised SQ derivative.

By implementing SQ dyes in SC one may rely on the upgrades in ability to tune the photoactive material bandgap for better utilisation of the solar spectrum, to combine absorbers having high absorption coefficients and thickness less than 100 nm to maximise utilisation of the available solar radiation, to deepen the donor highest occupied molecular orbital (HOMO) levels to increase open circuit voltage (Voc), to modulate molecular interactions to allow favourable morphology and thereof charge transport, and to efficiently collect charge using metal electrodes.

To increase the efficiency of SC, one can use the incident light better, which can be achieved by use of nanostructured layers that improve charge carrier collection and separation. Zincite is, after titania, the most widely used electron transport layer (ETL), owning to its low cost, non-toxicity, and ease of synthesis in various nanostructured forms. Namely 1D configuration enables boosting of physical properties, consequently enabling a major role in optoelectronic

devices. Growth of ZnO nanorods (NRs) can be achieved various physical and chemical methods. While physical deposition techniques have been used successfully, many require demanding conditions for successful reaction, such as high purity atmosphere, high temperature and pressure. On the other hand, chemical solution processes, e.g., chemical bath deposition [3], greatly facilitates the fabrication of well-aligned ZnO NR on a large scale at moderate temperatures, with a facile control of the growth, and can be used on different kind of substrates (glass, Si wafers, etc.).

2. Experimental

Chemical bath route was used to prepare zincite NR on various substrates. Several routes were used to prepare SQ dyes which were blended with other polymers and spin coated at NR. The system was broadly characterised (XRD, SEM, UVVis, TEM, PL), especially using dedicated atomic force microscopy (AFM) system.

3. Results and Discussion

We wanted to tune the SQ molecule structure. Among other routes we condensated squaraine with different groups, in symmetric and asymmetric manner. Plethora of nucleophilic groups are available; still major concern is their symmetry. The literature still does not over clear consensus over which symmetry is better for SC application. If any, SQ limits are found in propensity for self-aggregation. Thereof, the pragmatic approach is to derive symmetrical SQ and purify to isolate and combine 1,3-SQ-isomers. The 1,3-SQ-isomers should also show among highest squaraine thermal stabilities [4]. In order to take advantage of the distinctively strong absorption in the red part of the VIS spectra of the SQ electron donor material, an appropriate polymeric electron acceptor will be blended-in to allow better utilisation of the solar spectra. Commonly, fullerene based $PC_{60}BM$ and $PC_{70}BM$ electron acceptors are used.

The SQ is placed onto zincite ETL. The morphology and diameter of zincite nanorods is closely related to the nature of underlaying substrate (Fig. 2). The substrate also strongly impacts the zincite NR growth qualitative and quantitative parameters, optical properties, E_g, etc. One of the major advantages of the chemical approach is it enables the use of flexible and conductive substrates (such as ITO foil) [5].

Characterisation-wise, collecting information on type of the as-achieved morphology of the SQ in combination underlying rough (nanostructured) surfaces is critical. Spectroscopic methods (UVVIS, PL) revealed the extent of transparency and optical activity, while on behalf of electron microscopy (SEM, TEM) and diffraction (XRD) characterisation, morphological features and crystalline composition were confirmed. These and additional methods rarely fully elucidate local and average chemical homogeneity, electronic structure distribution and textural organisation issues. Requirements to cover wide sample surface with reliable, sensitive and adaptive analysis are still met by flexible multi-channel imaging methods, such as atomic force microscopy (AFM) with additional modules. Here we utilised Nanosurf FLEX-ANA automated system. In addition, synthesised, assembled and completed H-OPV SC having configuration of ZnO / SQ:$PC_{70}BM$ / PEDOT:PSS / Ag were also fully electrically characterized.

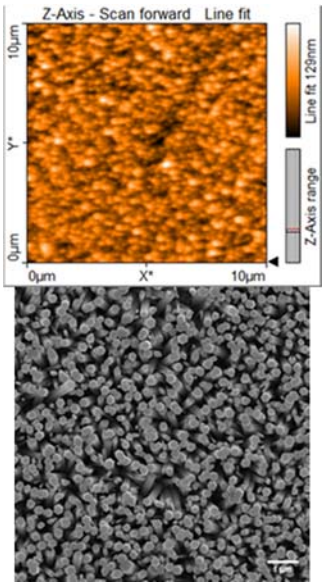

Fig. 2. a) AFM image of zincite nanostructured thin-film on glass substrate, b) SEM image of the zincite nanostructured thin-film on Si substrate.

4. Conclusions

We examined the feasibility of the SQ-material for H-OPV on behalf of interdisciplinary bottom-top approach and showed the effect of the different selected parameters on final properties of the selected SC. We mainly focused on the effect of the achieved SQ structure, domain formation and interaction of these with the ETL morphology, on the optical and electrical properties of the whole system. The developed and presented conceptual novelties (both for characterisations and syntheses) may shift the strategies of the SC design.

Acknowledgements

The authors acknowledge the support by the projects UIP-2019-04-2367 SLIPPERY SLOPE and PZS-2019-02-1555 PV-WALL of the Croatian Science Foundation.

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Physical Features of Branched Circuits with Contact Potential Differences

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Summary: Conditions are formulated under which the contact differences of potentials in a branched chain can be neglected. 1) A relatively small current value at which the Peltier and Zeeman effects can be neglected. 2) Constant current in all elements of loop current. 3) The constancy of the energy spectrum of current carriers. A detailed analysis of contact phenomena in a bipolar transistor is carried out. It is shown that an abrupt increase in the input voltage upon the appearance of a collector voltage is associated with disturbances in the energy balance, when the electron energy spent on the metal-emitter barrier transition cannot be compensated for in the base-metal transition. The balance is disturbed due to the different energy spectra of electrons in the transitions of the transistor. The adopted concept, together with the constructive solution of the semiconductor device, the properties of the metals used to actually connect the transistors.

Keywords: Branched chain, Contact phenomena, Bipolar transistor.

1. Introduction

A real electrical circuit usually contains components made from different materials. In classical electrical engineering, this circumstance is rightly not given much attention [1-9]. In real conditions, contact potential differences are inevitably present in a closed circuit, but they completely compensate each other, allowing the physical laws, discovered and formulated several centuries ago, to be used quite reasonably for their calculation. On the other hand, the Peltier and Zeeman effects (associated with contact phenomena) successfully work in technology, allowing both to measure the temperature and change its value in the required direction. The physical nature of the contact potential difference provides an opportunity to both increase the energy of carriers falling into the zone of its action, and to lower it. Naturally, specific changes in energy depend on the polarity of the potential difference, the direction of the carrier velocity, and the polarity of the carriers themselves. These phenomena are of particular importance in semiconductor technology, which has penetrated everywhere and has changed practical life, in which they occupy a large and important place. However, contact phenomena are not always correctly explained, since, oddly enough, the laws that determine their influence are still not clearly defined.

2. An Example of a Branched Circuit with Contact Potential Differences – Bipolar Transistor

A classic example of where the contact difference manifests itself in a paradoxical way is the bipolar transistor, about which everything from school textbooks to serious fundamental books on electronics seems to be written [1]. The first thing we learn from these sources is that a transistor is a device whose main function is to amplify or convert a weak signal from a measuring sensor into a voltage or current supplied to the device.

The most common way to turn on a transistor is with a common emitter circuit for maximum power gain. In this case, both the input current and the input voltage increase at the output of the circuit. For practical calculations, equivalent circuits of real transistors are used, in which there are models of the input base circuit and the output-collector circuit. The main element of this circuit is the current source in the collector circuit, and the magnitude of this current is linearly related to the magnitude of the current in this circuit, and the coefficient determining this relationship is much greater than unity. However, some unpleasant phenomenon occurs in the circuit - with the help of the collector current in bipolar transistors of the npn type, it is necessary to increase the voltage supplied to the base. Moreover, this phenomenon, noticeable on real input (basic) characteristics, is of an abrupt nature - it manifests itself immediately after a slight increase in the collector voltage (current). In classical equivalent circuits, this effect is described by the feedback coefficient between the collector voltage and the base voltage. The purpose of this article is a physical interpretation of this phenomenon, showing the obvious fallacy of the accepted interpretation. The longevity of this misconception is probably due to the fact that the effect itself manifests itself in the "inoperative" region of the transistor, when the required current gain (the main concern of the

transistor designer) is far from the maximum value. LTspice, an excellent electronic component simulator created to advertise products from the famous Analog Device, fails when trying to describe the operation of a transistor in this area. Analysis of contact phenomena in a bipolar transistor npn.

Let's consider in detail what happens in a real transistor switching circuit. In practice, a device whose basic principles of operation are determined by semiconductors is inevitably connected to the measuring circuit using metal contacts. Naturally, in each such connection, a contact potential difference arises. In the diagram shown in Fig. 1, they are represented by voltage sources in the form of circles with a polarity designation – the method adopted in the LTspice program.

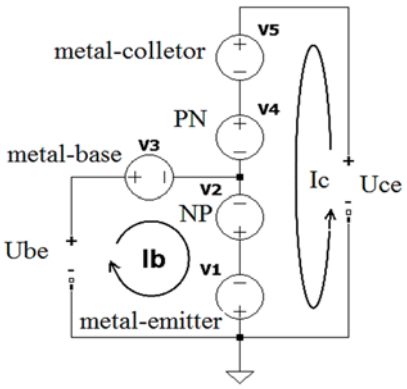

Fig. 1. Connection diagram with a common emitter of an NPN bipolar transistor. V1 – contact potential difference metal-emitter, V2 – np transition emitter-base, V3 – contact potential difference metal-base, V4 – pn base-collector junction, V5 – pin potential difference collector metal.

The input characteristics of the transistor necessarily include the original curve of the dependence of the current on the input voltage in the absence of the collector voltage, and, consequently, the collector current. At zero collector current, the contact differences of the metal connections of the transistor fully compensate each other, without exerting any influence on the formation of the input voltage, which is completely dependent on the junction voltage np. Naturally, this characteristic is not linear and corresponds to the current voltage characteristic of a semiconductor diode. At first glance, the appearance of the collector current does not change the situation in any way: the contact differences remain the same, and the weak base current, being part of the total emitter current flowing to the base, should not be influenced by the contact differences on the transistor electrodes. In this case, in both cases, the contact potential difference V1, which arises during the metal-semiconductor connection due to the different electron concentration in the metal and semiconductor, is the first barrier for electrons. As a result, electrons penetrate into the emitter, the average energy of which is less than the average energy of electrons in the metal contact. Let us consider in more detail what happens in the transitions of the bipolar transistor itself in Fig. 2.

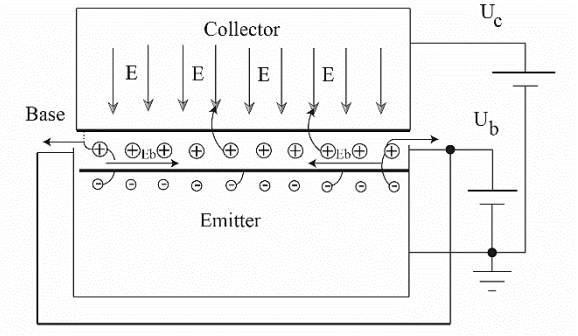

Fig. 2. Scheme of a bipolar transistor n-p-n (circuit with a common emitter).

Electrons entering the base layer through the emitter move in crossed electric fields. The relatively weak base voltage (Eb) forces them to move along the thin base layer, while the high collector voltage can drag them into the collector junction zone. For the most part, electrons with a relatively large kinetic energy get there. Such electrons have a high mobility and are likely to fall on the collector, avoiding the possibility of getting into the base contact. As a result, out of the total number of electrons that passed into the collector through the metal-emitter contact junction, most of them have a higher energy than the electrons entering the base. As a result, the energy spectrum of electrons going to the base differs from the energy spectrum of electrons reaching the collector. The average energy of these electrons is less than the average energy of the electrons entering the emitter. The contact difference V3, which increases their energy, is nevertheless not able to restore its value to the value that they had in the metal in contact with the emitter. Thus, the base-collector branching circuit is a device that sorts electrons by the amount of their energy. The base current does not change, it coincides with the fraction of the current flowing from the metal to the emitter, but the energy spectrum of electrons changes. Thus, when the collector current appears in the base circuit, irreplaceable energy losses occur. The kinetic energy of electrons that have lost energy during the transition of the metal-emitter contact cannot be restored to their original value when passing through the base-metal contact. Thus, an abrupt change in the input voltage with the appearance of even a small collector voltage, or rather the collector current, turns out to be associated with the contact potential difference of the metal-semiconductor. Based on the above, it is possible to formulate the conditions under which the contact potential differences do not affect the current in the branched circuit:

1) A relatively small current value at which the Peltier and Zeeman effects can be neglected;
2) Equal current value in all circuit elements;
3) The invariability of the energy spectrum of current carriers.

In the base circuit of the transistor, to make up for energy losses when a collector current appears and a concomitant change in the energy spectrum of electrons, it is necessary to increase the input voltage of the transistor. Fig. 3 shows the dependence of the ratio of the average energy E_m of electrons in a metal to the minimum energy of free electrons E_0, depending on the value of the minimum energy of the conduction band, expressed in meV, calculated at normal temperature. As follows from the graph, the presence of a contact potential difference that decreases the average energy of electrons is equivalent to an increase in their minimum energy and, consequently, a greater inhomogeneity of the energy spectrum of electrons.

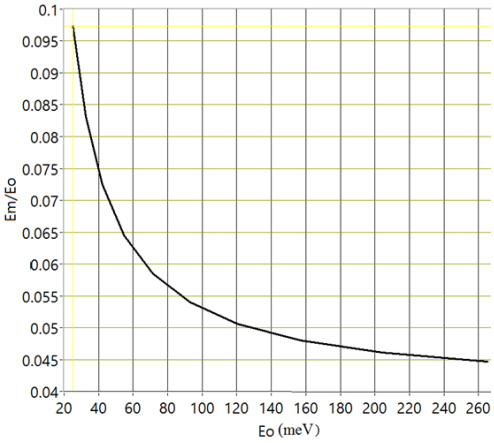

Fig. 3. Dependence of the ratio of the average energy of electrons in a metal to the minimum energy on the minimum energy at normal temperature.

A feature of the type of input characteristics of the n-p-n transistor is the high constancy of the amplitude of the input voltage jump. Figure 4 shows a sample of a typical input characteristic (n-p-n) of an Analog Device MAT-02 transistor.

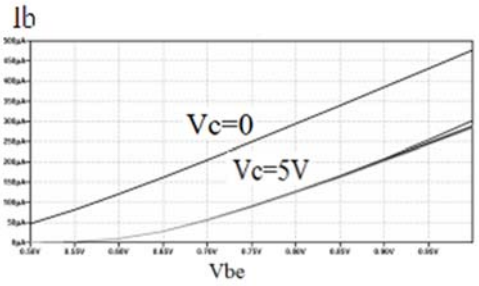

Fig. 4. Sample of a typical input characteristic (n-p-n) of an Analog Device MAT-02 transistor.

It is easy to see that the same value of the input current is achieved by increasing the input voltage by an almost constant increase in the input voltage by an amount equal to 0.2 volts. The constancy of this value is an additional argument in the erroneous interpretation of the input voltage jump from the appearance of the collector voltage. Of course, the accepted interpretation of the effect creates additional computational difficulties, since apart from the properties of the transistor itself, the properties of the metal used for contact with the terminals of the transistor must be taken into account. Studying the characteristics of p-n-p transistors, one can notice manifestations of the opposite effect – when the collector current appears, the absolute value of the input voltage decreases. This phenomenon is also easily interpreted within the framework of the proposed analysis and is associated with contact phenomena that arise when the transistor is actually turned on in the working circuit.

3. Conclusions

1. Conditions have been formulated under which contact potential differences in branched electrical circuits can be neglected.
2. The error of the classical interpretation of the input voltage jump when the collector current appears is shown.
3. A physical interpretation of the effect of a step change in the input voltage of bipolar transistors is carried out.
4. The ways of analyzing the operating mode of bipolar transistors are discussed, which make it possible to eliminate the shortcomings of the existing calculation models.

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Finite Element Analysis of Stress Distribution in CIS Package Under Thermal Cycling Condition

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Summary: With the development trend of high integration and miniaturization of CMOS image sensors (CIS), the requirements for chip functions are getting increasingly higher. In this work, CIS packages were tested under thermal cycling conditions and presented two failure modes: (1) Delamination between the RDL and wafer functional layers, and (2) Fracture in the SMF layer above the metal pad. Finite element analysis was used to study the stress distribution of the CIS structures. Through the analysis of the simulation results, high stress concentration at the failure location of the package during the test, which indicates that the thermal mismatch between different materials under thermal cycling is the dominant factor for the generation of crack. By adjusting the structural parameters in the simulation model, the effect of the TSV trench, RDL, and PA thicknesses on the stress concentration of the CIS package was investigated. The structure shows the lowest stress concentration as the trench, the thickness of the via, and the width of the via is 90, 60, and 50 μm, respectively. In this study, when the trench thickness, via thickness, and opening length are 90 μm, 60 μm, and 50 μm, respectively, the stress of this structure is the smallest, which is 524.41 MPa. Compared with other parameter settings, the stress concentration is relatively small when the via opening length is 50 μm. When the opening of the via is 45 μm, the model of 90+60 shows lower max stress than the other two. When the opening length of the via is 55 μm, the 100+50 design appears lower stress concentration in the package. The local simulation results for the RDL layer show that the stress concentration in the structure locates at the RDL layer close to the solder pad. Pure Cu should play as the recommended RDL material in the structure and process design since it presents the lowest stress concentration of the others. For a two-layer design, the thickness of Cu and Ni in the RDL should be closer. With the increase in the thickness of the PA layer, the maximum stress of the structure tends to decrease.

Keywords: Finite element, RDL, Thermal cycling, Stress.

1. Introduction

With the development of electronic information and artificial intelligence, intelligence has become an important development direction in automotive electronics [1]. Among them, image sensors, including CCD (Charge Coupled Device) image sensors and CMOS (Complementary Metal-Oxide-Semiconductor), are important components of automotive electronics intelligence. There are differences in the structure of the two, in which CCD is composed of optical coupling devices, while CMOS is composed of metal oxide devices. Compared with CCD, CMOS image sensor (CMOS Image Sensor or CIS) has the characteristics of fast frame display speed, high integration (can reduce the use of peripheral components and system cost), low power consumption, etc., and has obvious performance and cost. Advantage [2-5]. Therefore, CMOS image sensor (CIS) has become one of the most widely used sensors in automotive electronics. In the past two decades, Moore's Law has promoted the rapid development of integrated circuit technology, and integrated circuit products have higher and higher requirements for packaging technology. With the development trend of high integration and miniaturization of automotive electronics, CIS chips need to undertake more functions and loads, which puts forward higher requirements for its reliability [6-12]. Therefore, it is of great significance to carry out research on the reliability of CIS packaging [13-17].

Xiao et al. performed microstructural observations and finite element simulations on TSVs with a diameter of 35 μm and an aspect ratio of 3:1 and analyzed devices that failed after reliability testing. According to the simulation results, the high interface stress concentration of the silicon dioxide layer is the main factor leading to the failure of the device [18]. Zhou et al. conducted a simulation study on a CMOS image sensor using the WLCSP packaging process and analyzed the influence of the thickness of the silicon layer and the shape of the UBM on the stress distribution of the pad during temperature cycling. The results show that the thickness of the silicon layer has little effect on the stress of the Cu pad. The equivalent stress of the Cu pad increases linearly with the diameter of the TSV, and the maximum von Mises stress decreases linearly as the θ angle (UBM shape) increases, the distance between the neck and the UBM increases [19]. Chen et al. simulated the through-silicon via (TSV) structure by finite element simulation and studied the effect of TSV thickness, diameter, and spacing on the equivalent thermal conductivity of composite TSVs. The results show that the thermal conductivity in the z-direction increases with the Cu diameter and decreases with increasing

spacing, while changes in thickness do not affect this value. The thermal conductivity in the x and y directions increases with increasing TSV spacing but decreases with increasing TSV thickness and copper diameter. Furthermore, the SiO_2 layer with thermal conductivity of 1.57 W/(mK) has a significant effect on the equivalent thermal conductivity of the TSV composite structure [20].

In this study, finite element simulation was used to study the stress distribution of the CIS package under thermal cycling conditions, and the dominant factors leading to the crack generation were analyzed. The effects of TSV structure parameters, RDL (Re-Distribution Layer) thickness, and PA (Passivation) thickness on the stress distribution of the package structure were studied. The research results are of great significance for the optimizing design of the CIS package.

2. FEM Model and Materials Properties

2.1. Failure Positions in Experiments

The complete CIS package structure is complex. To improve the efficiency of the simulation work and ensure the accuracy of the simulation results, it is necessary to obtain the typical features and sensitive areas of the CIS structure through experimental methods for model building. Therefore, the temperature cycle test was carried out under the conditions of -40 ℃ -125 ℃, and the CIS samples were analyzed after 1000 cycles to clarify the failure position. Fig. 1 shows the surface morphology and local optical magnification image of the CIS package. It can be seen from the figure that cracks generated on the surface of the CIS structure close to the BGA solder joints.

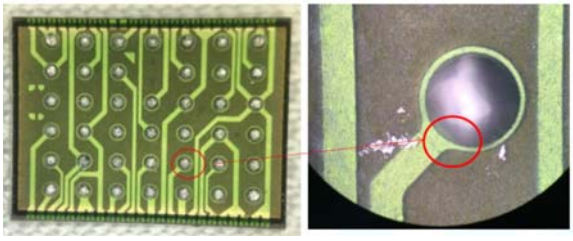

Fig. 1. Optical morphology of the package.

To further confirm the specific location of the crack formation, the failed samples were inlaid, ground, and polished, and the SEM morphology of the cross-section of the samples was analyzed, as shown in Fig. 2. According to the SEM morphology, during the thermal cycling test of the sample, cracks formed and propagated in the RDL and PA layers close to the BGA solder balls, and this area on the surface was the sensitive location for the failure during the reliability test.

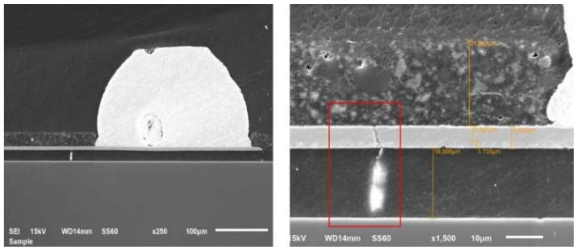

Fig. 2. SEM morphology of the failure area.

2.2. Finite Element Model

Based on the experimental results, the concerned areas of the CIS package are modeled and simulated. Fig. 3 shows the schematic diagram of the structure of the TSV area and the BGA solder ball area. The model includes such as SMF (solder mask face), CV (cavity wall), Epoxy, Oxide, RDL, and BGA (Ball Grid Array). Table 1 shows the geometric sizes while Table 2 presents the material parameters in the models.

Table 1. Geometric sizes in the models.

SMF (μm)	RDL (μm)	CV Epoxy (μm)	BGA Height (μm)	BGA Diameter (μm)
25	5	40	175	300

Table 2. Material parameters in the models.

Materials	Density (g/cm^3)	CTE (10^{-5}/℃)	Young's module (10^5/MPa)	Poisson's ratio	λ ($W \cdot m^{-1} \cdot k^{-1}$)
SMF	6.600	5.80	0.460	0.300	0.19
Si	2.330	0.28	1.100	0.240	131.80
Cu	8.942	1.69	1.290	0.345	396.70
Ni	8.092	1.30	2.000	0.300	82.57
SAC305	7.380	2.35	0.510	0.400	58.00
Sio_2	2.200	0.05	0.700	0.270	27.00
PA	0.105	5.40	0.025	0.380	0.200

Thermal analysis follows the first law of thermodynamics. There is no inflow or outflow of mass, and can be described as follows:

$$Q - W = \Delta U + \Delta K_E + \Delta P_E, \quad (1)$$

where Q and W are the heat and work, ΔU is the internal energy of the system, ΔK_E is the kinetic energy, and ΔP_E is the potential energy. The thermal steady-state analysis used in the text means that the heat flowing into the system is equal to the heat flowing out, i.e., Q = ΔU = 0. When the system is in a thermally steady state, the heat flowing into the system and the heat generated by the system itself is equal to the heat flowing out of the system, indicating that the net heat flow rate of the system is 0. In the steady-state

thermal analysis, the temperature of each node in Ansys does not change with time, and the energy balance equation is as follows.

$$[k] \bullet \{T\} = \{Q\}, \quad (2)$$

where [K] is the conduction matrix including thermal conductivity, convection coefficient, and shape function. {T} nodal temperature vector and {Q} is nodal heat flow rate vector. According to the conservation of energy, the steady heat balance can be expressed as:

$$[C] \bullet \{T\} + [K] \bullet \{T\} = \{Q\}, \quad (3)$$

where [C] is the specific heat matrix, $\{\dot{T}\}$ is the derivative of temperature to time. For thermal stress analysis, the thermal stress can be obtained as follows:

$$\{\sigma\} = [D] \bullet (\{\varepsilon\} - \{\varepsilon_0\}), \quad (4)$$

$$\{\varepsilon_0\} = \alpha \bullet T \bullet [\alpha \bullet T, \alpha \bullet T, \alpha \bullet T, 0,0,0]^T, \quad (5)$$

where {σ} is the thermal stress, {ε} is the deformation of the system, $\{\varepsilon_0\}$ is the deformation caused by temperature change, and [D] is the elastic modulus matrix. α is the coefficient of liner expansion, and T is the change of temperature, which corresponds to the nodal results of steady temperature analysis.

The thermal cycling load is set as the loading condition. According to the JESD22-A104 standard, the relationship between temperature and time is shown in Fig. 4. Among them, the temperature cycle range is -40 °C-125 °C, the temperature rise, and fall speed is 15 °C/min, and the high and low temperature holding time is 5 min. The heat exchange between the model and the environment is natural convection.

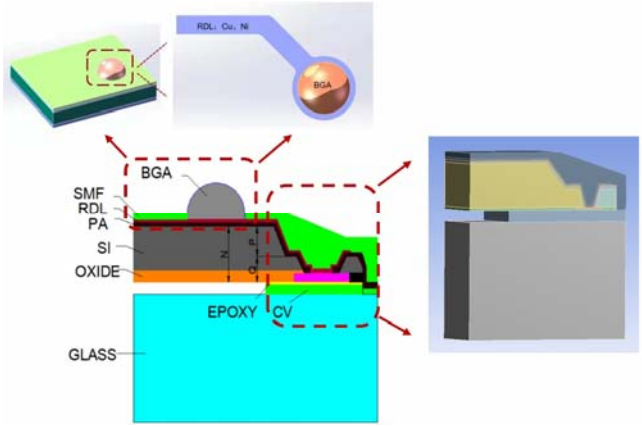

Fig. 3. The diagram of the package structure.

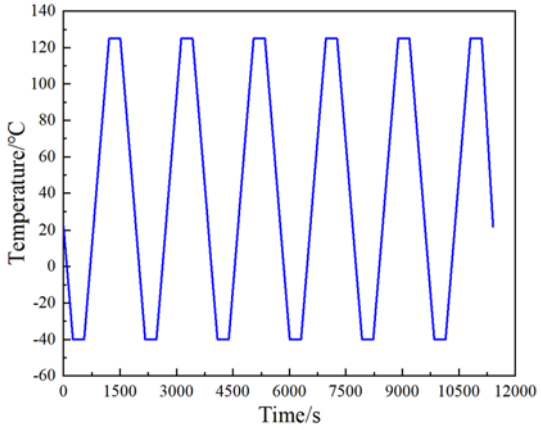

Fig. 4. Curve of temperature change with time.

3. Results and Discussion

3.1. Effect of TSV Trench on Stress Distribution

In the CIS package, Si is the body material of the entire structure and is a dominant factor affecting the thermodynamic characteristics of the package. To investigate the stress distribution characteristics of CIS package under thermal cycling conditions, the influence of trench, via, and opening sizes on the stress distribution was discussed. According to the structural features of the CIS package, six models were built with varying the geometric sizes of the trench, via, and opening in the structure. When the trench thickness is 90 μm, the thickness of via is 60 μm. When the trench thickness is 100 μm, the thickness of via is 50 μm. For the above two structures, the size of via opening is 45 μm, 50 μm, and 50 μm, respectively.

According to the cross-sectional view of the package, the geometric model is built with SolidWorks software, as shown in Fig. 1. Fig. 5 shows the meshed model in the finite element software. The model structure mainly includes the SMF, RDL, PA, CV, and Epoxy layers. The sizes and material parameters can be seen in Table 1 and Table 2. Fig. 6 shows the finite element simulation results of the model. Under thermal cycling conditions, the maximum value of the package equivalent stress appears at the interface between SMF and RDL, close to the solder joint, with a max data of 534.72 MPa. The main reason for the localized stress

concentrations is the thermal mismatch of multiple layers of materials in the package structure during thermal cycling.

Fig. 5. Meshed model of the package.

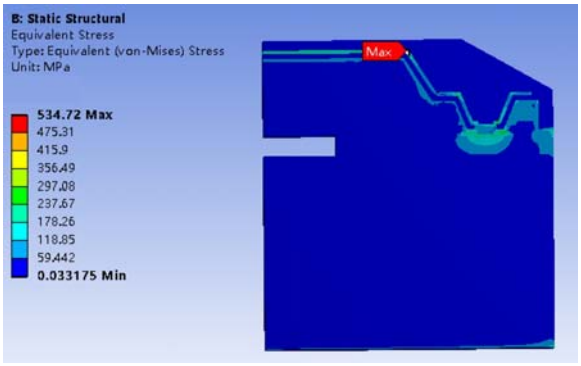

Fig. 6. Stress distribution in the package.

Fig. 7 shows the max equivalent stress for different TSV structural designs. The stress concentration areas of the structure are the same with various geometric parameters of the trench, via, and opening. The maximum stress is 524.41 MPa when the parameter is 90+60/50. This data is 596.19 MPa when the parameter is 90+60/55. Besides, the max equivalent stress in the 100+50/45, 100+50/50, and 100+50/55 models is 628.86 MPa, 534.82 MPa, and 543.12 MPa, respectively. The max equivalent stress is the lowest when the TSV parameter is 90+60/50 among all the models. To the models with the same trench and via thickness, the max equivalent stress appears in the model with the opening length of 50 μm. When the opening of the via is 45 μm, the model of 90+60 shows lower max stress than the other two. When the opening length of the via is 55 μm, the 100+50 design appears lower stress concentration in the package.

3.2. Effect of RDL Thickness on Stress Distribution

According to the discussion above, the stress concentration of the entire CIS package under thermal-cycling conditions locates in the RDL layer. Since the constituent materials of the RDL layer are mainly Cu and Ni in industrial applications, to study the stress distribution characteristics of the RDL layer, the effect of the thickness of Cu and Ni in the RDL layer on the stress distribution was investigated. Here the total thickness of the RDL layer is 5 μm. When the thickness of Ni is 3 μm, the thickness of Cu is 2 μm. When the thickness of Ni is 1 μm, the thickness of Cu is 4 μm. In addition, the cases when the RDL layers are all Ni or Cu were also concerned.

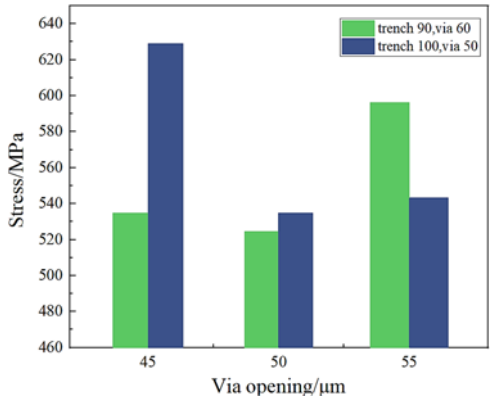

Fig. 7. The maximum stress of the packages.

The related model structure is shown in Fig. 1, and the model size and material parameters are as shown in Table 1 and Table 2. Fig. 5 shows the simulation results of the RDL layer. As presented in the figure, the max equivalent stress in the structure locates at the RDL layer close to the solder pad. It is consistent with the crack generation during the experimental tests, as shown in Fig. 1 and Fig. 2. According to the experiment and simulation analysis, the dominant factor for the RDL crack in the experiment is supposed to be the high-stress concentration here during the thermal cycling conditions. At the same time, the consistency between the simulation results and the experimental results supports the accuracy of the simulation model. As presented in the figure, the max equivalent stress in the structure is 130.59 MPa, located at the RDL layer near the Cu pad. There is a contact angle between the RDL and the Cu pad. As this contact angle increases from 0° to 180°, the deformation behavior due to thermal expansion at this area transforms. Consequently, a lower contact angle leads to higher stress concentration since the thermal deformation is weak due to its limited space. In addition, only one side of the pad is connected to the RDL layer, while the other side of the Cu pad is equivalent to a free end. Compared with the case where both ends have RDL constraints, this free end is more prone to thermal deformation in a changing temperature environment. It makes the stress in the sensitive area more concentrated. In addition, there are BGA solder balls on those Cu pads in the CIS package. It aggravates the phenomenon of stress concentration and cracks propagation.

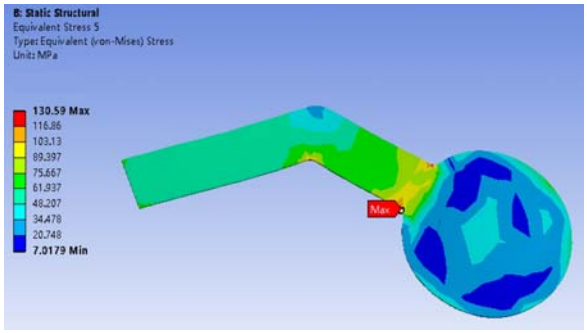

Fig. 8. Stress distribution on RDL with Cu and Ni layers.

According to the simulation results, the maximum equivalent stress concentration position under the concentrated RDL design is the same, and its data is as shown in Fig. 9. As can be seen from the figure, when the RDL layer consists of only Cu, the highest equivalent stress is the smallest, which is 118.46 MPa. When the RDL layer material is Ni, the max data here is 137.25 MPa, which is 16 % higher than the Cu RDL structure. The different material parameters between Cu and Ni are the dominant factor leading to the difference in their stress distribution. As shown in Table 2, Young's modulus of Ni and Cu is 2.0×10^5 MPa and 1.29×10^5 MPa, respectively. Young's modulus is an index reflecting the ability of a material to resist deformation. A high Young's modulus means that it is difficult for the material to deform and relieve stress when subjected to changes in ambient temperature loads. Therefore, the Ni RDL structure shows a more stress concentration than the Cu RDL. Another design is that the RDL consists of two materials. When the thickness of Cu is 4 μm while the thickness of Ni is 1 μm, the maximum equivalent stress of the structure is 148.78 MPa. The highest equivalent stress is 130.59 MPa when Cu thickness is 2 μm while Ni is 3 μm. It can be seen from the above results that the local stress concentration phenomenon of the all-Cu structure under the thermal cycling environment is weak. For a two-layer design, the thickness of Cu and Ni in the RDL should be closer.

3.3. Effect of PA Thickness on the Stress Distribution

Since the RDL layer connects to the PA layer, its material thickness influences the local stress concentration in the structure. Based on the previous study and processing technology restrictions, the thickness of the PA layer investigated is 10 μm, 20 μm, and 30 μm, respectively, in the simulation model. The stress distribution behavior of the package under thermal-cycling conditions is studied. As shown in Fig. 10, when the thickness of the PA layer is 10 μm, the max equivalent stress of the structure is 143.18 MPa.

The stress concentration locates at the connection between the Cu pad and RDL. When the thickness of the PA layer changes, the stress distribution of the structure under thermal-cycling conditions do not change, but the max value of the equivalent stress changes. Fig. 11 presents the data of maximum stress of the packages with different PA thicknesses. When the thickness of the PA layer is 20 μm, the max value is 130.59 MPa. When the thickness of the PA layer reaches 30 μm, the stress in this region becomes 113.59 MPa. With the increase of the PA layer's thickness, the max value of the structure tends to decrease. According to the cross-sectional SEM morphology of the package shown in Fig. 2, the PA layer locates between the RDL and the Si layers. As shown in Table 2, there is a big difference between the thermal expansion coefficient of Si and the metal material of the RDL layer, and the thermal mismatch between the two is serious when the ambient temperature changes, resulting in the formation and accumulation of stress. Since PA shows plastic behavior, it can alleviate the thermal mismatch between RDL and Si. This stress-relieving effect is better when the thickness of PA increases. Therefore, appropriately increasing the thickness of this layer helps reduce stress concentration and improve the reliability of the structure.

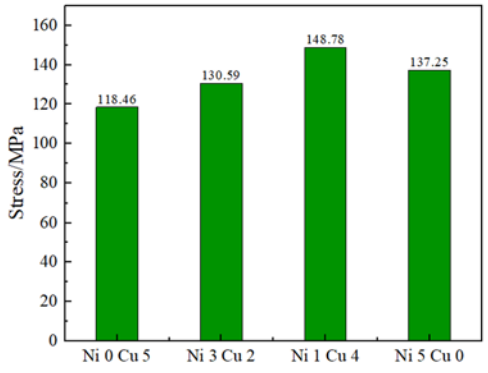

Fig. 9. Maximum stress with different RDL structures.

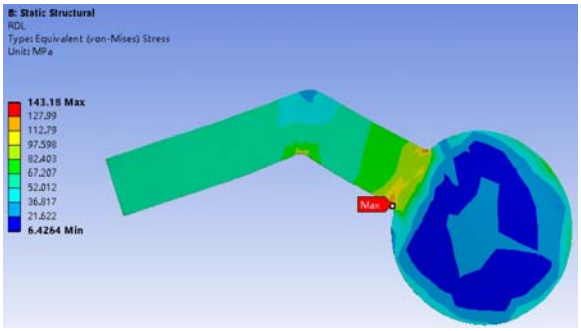

Fig. 10. Stress distribution with PA thickness of 10 μm.

4. Conclusions

This work uses experiments and finite element simulation analysis methods to study the stress distribution characteristics of the geometry effects of

the trench, the via, the RDL, and the PA on the CIS package structure under temperature cycling conditions. The results show that the geometric size of the TSV significantly affects the stress distribution of the whole package. When the trench thickness, via thickness, and opening length are 90 μm, 60 μm, and 50 μm, respectively, the max equivalent stress of the CIS package structure is the smallest. Compared with other parameter settings, the stress concentration is relatively small when the via opening length is 50 μm. The local simulation results for the RDL layer show that the stress concentration in the structure locates at the RDL layer close to the solder pad is the main reason for cracks at this position during the experiment. Adding a Ni layer to the RDL layer will aggravate the stress concentration and affect the structural reliability. Pure Cu should play as the recommended RDL material in the structure and process design. The increase in the thickness of the PA layer helps relieve the stress concentration under the condition of thermal cycling.

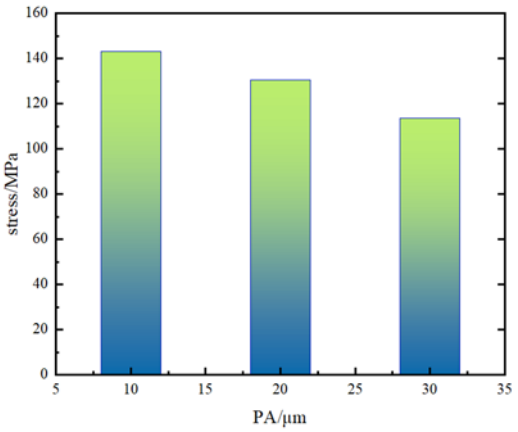

Fig. 11. Maximum stress with different PA thicknesses.

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Total Ionizing Dose Effect on the 3D Interconnection Structure of Microsystem

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Summary: Microsystem technology has brought a new direction to the development of integrated circuits. However, for space applications, the radiation environment brings new challenges to the reliability of microsystems. The radiation effect represented by the total dose effect will threaten the safe operation of the microsystem. Therefore, to study the influence of the total-dose effect on the microsystem, irradiation experiments were carried out on the interconnect structure in the microsystem. A vector net-analyzer is used to measure the scattering parameters of the specimens before and after irradiation. The effect of irradiation dose on the transmission performance of the microsystem was studied. In addition, based on the experimental results, an equivalent circuit simulation model is established to analyze the mechanism of radiation-induced signal transmission performance changes. The research results show that the total dose effect mainly affects the internal parasitic parameters of the interconnect structure and leads to the degradation of the transmission performance of the interconnect structure.

Keywords: Microsystem, Total dose effect, Scatter parameters, TSV, Equivalent circuit.

1. Introduction

Microsystem is an advanced technology in satellites, aircraft, missiles, radar, and other relative fields. System in package (SiP) is one of the leading technologies to realize microsystem integration [1-3]. Through the stacking and packaging of multiple chips, the power density and functional density in SiP significantly improves [4-7]. With the development of advanced packaging technology, realizing the vertical interconnection of chips in the SiP packaging structure by TSV technology has become the mainstream trend [8-11]. This technology is one of the effective ways to continue Moore's Law [12-13]. TSV brings many advantages to microsystems [14-17], including effectively reducing interconnect length, power consumption, and latency, shortening development and production cycles, and improving performance.

The radiation problems of microsystems containing TSV structures have been studied at home and abroad. Zeng et al. conducted the effect of total dose irradiation on capacitance and leakage current between TSVs. The results show that total dose irradiation leads to an increase in the leakage current between TSVs and a decrease in the capacitance of the TSV array. The reason is that the radiation causes defects in the TSV structure, resulting in changes in the properties of the structure [18]. Kan et al. irradiated nMOS and pMOS FinTET devices fabricated using TSV technology. The results show that the total dose irradiation has little effect on the threshold voltage shift and maximum transconductance. It demonstrated that TSV integration technology does not significantly reduce the radiation resistance of the device [19]. Gouker et al. performed proton irradiation on a three-layer SRAM with a stacked structure and used a Monte Carlo method to simulate the irradiation process. In his study, no interlayer effect was found, which proved the feasibility of 3D structural space application [20]. Valerio et al. fabricated a two-layer CMOS image sensor using three-dimensional integration techniques. After irradiation with a cobalt source, they found that transistors fabricated using 3D integration techniques were less sensitive to noise voltages from ionizing radiation [21]. Cao et al. used Geant4 to simulate single-event inversion of multilayer SRAMs. Simulation results show that the inversion cross-section of each layer in the multilayer SRAM is the same, but the high-energy ions increase the inversion cross-section of the multilayer SRAM [22].

As discussed above, the research on the radiation effects of microsystems focuses on systems or devices. There are few studies on the radiation effects of interconnect structure in microsystems. The interconnection structure is the carrier of the signal transmission of the microsystem, and its radiation effect is of significance to the system structure. Therefore, in this work, a total dose irradiation experiment was carried out on the interconnect structure of the microsystem to study the effect of irradiation dose on the scattering parameters of the interconnect structure. Based on the experimental results, this work builds the equivalent model of the circuit and therefore studies the effect of total dose irradiation on the internal parasitic parameters of the interconnect structure.

2. Experiments and Results Discussion

2.1. Experimental Procedures

Fig. 1 shows the schematic diagram of the sample structure used in this study. The specimen consists of

TSV, RDL, Si, and polyimide layer. Among the three rows of TSVs in the figure, the two TSVs in the middle row are signal TSVs connected to the RDL. The others are the ground TSVs, which can prevent external radiation of TME waves, provide additional return paths for key signal TSVs, and make the transmitted RF signal TSVs in a good grounding environment.

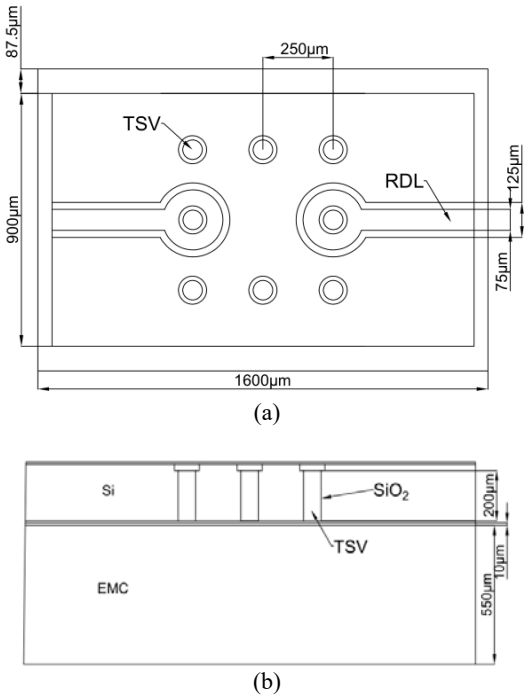


Fig. 1. Diagram of the structure of the microsystem specimen. (a) Top-view, and (b) Cross-sectional view.

Silicon is the filling material in the upper part of the whole structure, and polyimide is the support in the lower layer. The materials of TSV, RDL and Bump are all copper. The periphery of each copper pillar TSV is insulated with silicon dioxide, and the signal RDL and the ground RDL also use silicon dioxide as the insulating layer. S-parameter is the parameter to evaluate the signal transmission performance of the microsystem interconnect's structure. Fig. 2 presents the testing platform with a vector network analyzer and a probe station. Fig. 3 shows the magnified view of the probe station during a test.

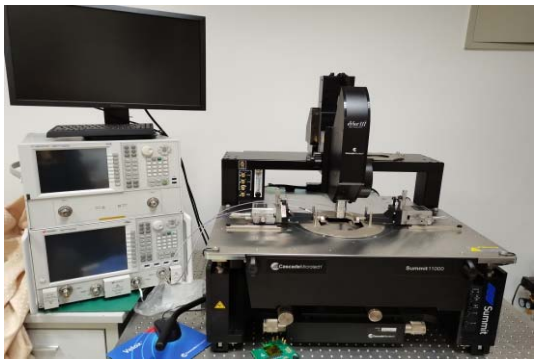


Fig. 2. Testing platform in the experiment.

First, install a pair of GSG-type 250 mm probes on the probe station, as shown in Fig. 3, and connect the high-frequency transmission cable with the vector network analyzer and the testing probe. Next, establish a network connection between the vector network analyzer and the probe station calibration software, set the test frequency band of the vector network analyzer to 0.1 GHz to 26.5 GHz, and perform calibration. After that, fix the specimen and test its S-parameters.

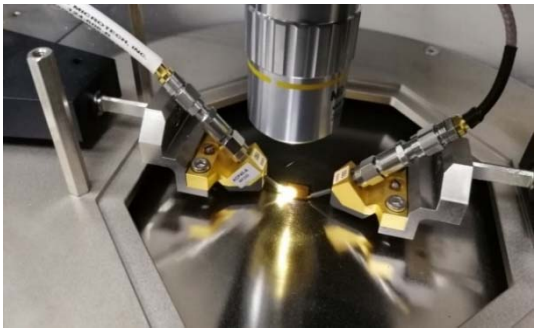


Fig. 3. Probe station in the platform.

The scattering parameters output by the vector network analyzer can be used to evaluate the signal transmission performance. Taking the two-port network as an example, the matrix equation of the S-parameter is defined as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (1)$$

Among them, a1 and a2 are the input signal from port1 and port2, while b1 and b2 are the output signal from port1 and port2. The S-parameters in the matrix equations represent the ratio of the outgoing wave to the incoming data at each port. Since the structure of this specimen is symmetrical, S11 equals S22 while S12 equals S21.

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2 = 0} = \frac{sine\ wave\ out\ from\ port\ 1}{sine\ wave\ into\ port\ 1}, \quad (2)$$

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2 = 0} = \frac{sine\ wave\ out\ from\ port\ 2}{sine\ wave\ into\ port\ 1} \quad (3)$$

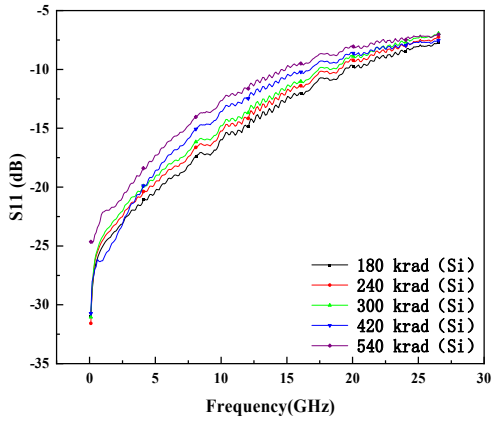
Since this structure is a passive device, the data of S11 and S21 are less than 0 in the S-parameter diagram. S11 close to 0 indicates that the port has more signals reflected than transmitted. In contrast, if the data of S21 is close to 0, the port shows good transmission performance. The irradiation test uses ^{60}Co with a dose rate of 50 rad(Si)/s as the source. The irradiation doses were 180 krad(Si), 240 krad(Si), 300 krad(Si), 420 krad(Si), and 540 krad(Si).

2.2. Analysis of Results

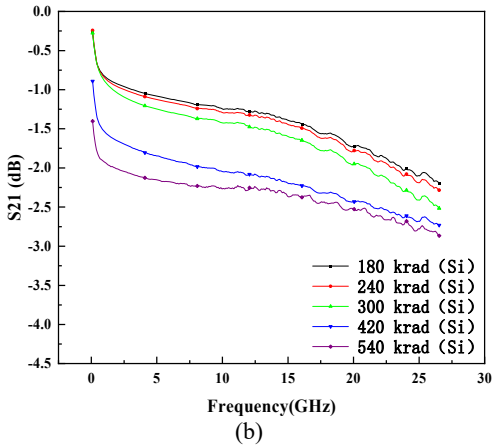
Fig. 4 (a) is the S11 curve at each dose point, and Fig. 4 (b) is the S21 curve at each dose point. As shown

in Fig. 4(a), S11 at each dose point increases with frequency, and each curve rises fast between 0.1 GHz-1 GHz. In the range from 25 GHz to 26.5 GHz, the curve ascends slowly and tends to be flat at the end. At the same frequency, S11 showed an upward trend with the increase in radiation dose. An increase in S11 represents an increase in the ratio of the reflected signal to the input signal, while the input to the vector network analyzer is constant, which means that in the curve at each dose point, the transmission performance of the interconnect structure gradually decreases with increasing frequency. With a fixed frequency, as the dose increases, the reflected signal at the input of the interconnect structure increases while the transmission performance decreases.

As shown in the S21 curve in Fig. 4(b), the S21 at each dose point decreases with frequency. Between 0.1 GHz and 1 GHz, the data drops fast, and then the rate of decrease was relatively constant. Under the same frequency, each S21 data shows a decreasing trend with the increase of irradiation dose. Decreasing S21 indicates that the ratio of the output signal to the input signal drops. It means that increasing the irradiation dose leads to the decrease of the signal at the output end of the interconnect structure and the transmission performance.



(a)



(b)

Fig. 4. S-parameters with different irradiation doses obtained in the experiment. (a) S11 curves, and (b) S21 curves.

There is a total dose effect in the three-dimensional interconnected structure of the microsystem. As the radiation dose changes, its signal transmission characteristics change. It is of significance to study the mechanism for such a phenomenon.

3. Equivalent Circuit Simulation and Radiation Effect Analysis

3.1. Equivalent Circuit Modeling

This work uses the method of equivalent circuit simulation to study the influence of the total dose effect on the internal parasitic parameters of the interconnect structure. The equivalent electric circuit is built by the parameter extraction formula and the physical design of the experimental sample. However, due to the complexity in the actual electric circuit, it is not conducive to simulation and optimization. It is necessary to simplify the equivalent circuit according to the principle of circuit simplification. Fig. 5 and Fig. 6 show the simplified equivalent electric circuits. Since RDL, bump, and TSV have the same circuit structure in the original electric circuit, they are equivalent to impedance Z_{RDL} and $Z_{TSV+Bump}$ as resistor and inductor in series.

$$Z_{RDL} = R_{RDL} + {jwL_{RDL}}/{2}, \tag{4}$$

$$Z_{TSV+Bump} = R_{TSV+Bump} + {jwL_{TSV+Bump}}/{2} \tag{5}$$

The circuit between RDL and the electric circuit between TSV and Bump can be equivalent to Y_{RDL} and Y_{TSV}. Specifically, the conductance and capacitance in the silicon substrate are first connected in parallel, then connected in series with the upper and lower capacitors, and finally embodied as a paralleled capacitor and conductance.

$$Y_{RDL} = jwC_{IMD} + \\ + \left({G_{RDLinSub}}/{2} + {jwC_{RDLinsub}}/{2}\right)^{-1} + \frac{6}{jwC_{TSVtosub}}, \tag{6}$$

$$Y_{TSV} = jwC_{underfill} + \left(jwC_{Bump} + \frac{jwC_{ox}}{2}\right)^{-1} + \\ + \left({G_{TSVinSub}}/{2} + {jwC_{TSVinsub}}/{2}\right)^{-1} + \\ + \left(jwC_{Bump} + \frac{jwC_{ox}}{4}\right)^{-1} \tag{7}$$

Among them, C_{IMD} is the equivalent capacitance between RDLs, $G_{RDLinsub}$ is the equivalent conductance of the RDL layer in silicon, $C_{RDLinsub}$ is the equivalent capacitance of the RDL layer in silicon, $C_{TSVtosub}$ is the equivalent capacitance of TSV in silicon, and $C_{underfill}$ is the Bump The equivalent capacitance between $G_{TSVinsub}$ is the equivalent conductance of TSV in silicon, C_{Bump} is the equivalent capacitance between

Bump and the insulating layer, and C_{ox} is the parasitic capacitance of TSV.

Based on the simplified circuit shown in Fig. 5, the equivalent circuit is further simplified, and the circuit structure is shown in Fig. 6.

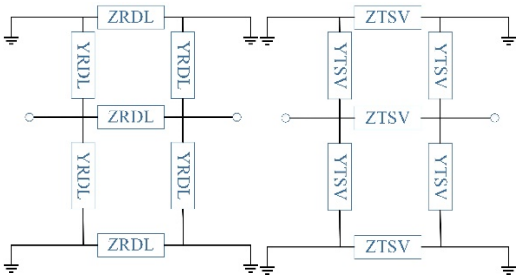


Fig. 5. Equivalent circuit after the first optimization.

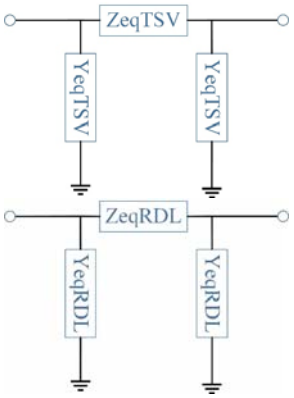


Fig. 6. Equivalent circuit after the second optimization.

Here, the relationship between the parameters is shown as below:

$$Z_{eqTSV} = \frac{3}{4}Z_{TSV}, \quad (8)$$

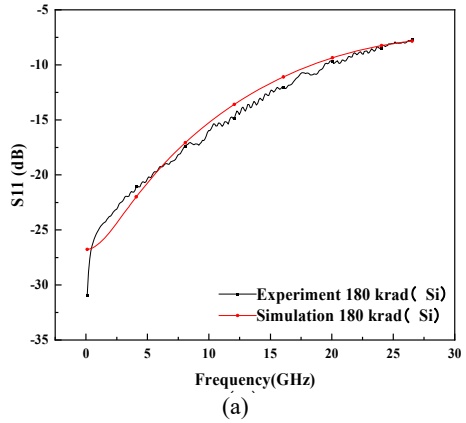
$$Y_{eqTSV} = 2Y_{TSV}, \quad (9)$$

$$Z_{eqRDL} = \frac{3}{4}Z_{RDL}, \quad (10)$$

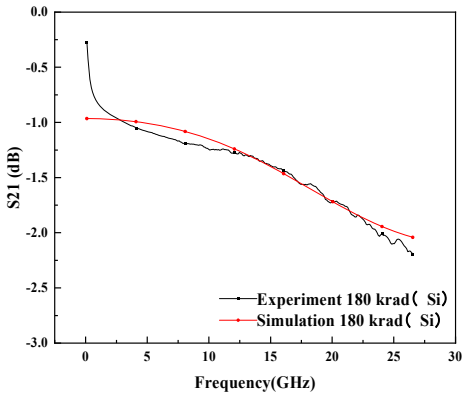
$$Y_{eqRDL} = 2Y_{RDL}, \quad (11)$$

3.2. Simulation Results and Analysis

This work use ADS software to build the above equivalent circuit and run a simulation process. The simulation conditions are the same as those of the vector network analyzer used in the experiment. Fig. 7 presents the S-parameters with an irradiation dose of 180 krad(Si) obtained from the experiments and simulation. According to the S11 curves shown in Fig. 7(a), the difference between the measured and simulated results is 5 dB at 0.1 GHz. However, as the frequency increases, the difference between the measured and simulated results decreases rapidly, and the difference is less than 2 dB. As shown in Fig. 7 (b), the difference of S21 between the measured and simulated results is 0.8 dB at 0.1 GHz. This data decreases rapidly to 0.2 dB with increasing frequency. Therefore, the simulated result of the equivalent circuit is slightly deviated from the measured curve and shows an acceptable consistency.



(a)



(b)

Fig. 7. S-parameters under 180 krad(Si) obtained from simulation and experiment. (a) S11 curves, and (b) S21 curves.

After confirming the accuracy of the equivalent circuit model, modifying the parameter values of the electrical components corresponding to the areas susceptible to irradiation in the structure. Reducing the TSV capacitance in the model and increasing the TSV resistance value can accurately simulate the change of S11 with the increase of irradiation dose during the experiment. Taking the test results of the irradiation dose of 240 krad(Si) as an example, Fig. 8 shows the measured and simulated curves by optimizing the TSV capacitance and TSV resistance in the equivalent circuit. It is clear from the figure that the simulation results are in good accordance with the experimental results.

Use the above method to simulate the equivalent circuit under different irradiation doses. Fig. 9 shows the relationship between the TSV capacitance, TSV resistance, and radiation dose obtained. It can be seen from the figure that as the irradiation dose increases, the TSV capacitance decreases, while the TSV

resistance shows an upward trend. According to the parameter extraction formula and equivalent circuit, the TSV capacitance refers to the parasitic capacitance between the TSV and the insulating layer SiO_2 and the silicon substrate. The influencing factors are the size of the TSV, the thickness, and the dielectric constant of the insulating layer. TSV resistance includes DC and AC resistance, where DC resistance depends on TSV size and resistivity. The AC resistance is more closely related to the skin depth, which depends on the permeability and conductivity of the material. Since the total dose irradiation does not change the geometric size of the specimen, the effect is mainly due to the internal defects of the material generated by the irradiation. According to the mechanism of total ionizing dose irradiation, the total dose irradiation will excite electron-hole pairs inside the material, which will affect the physical properties such as the dielectric constant of the material, and eventually lead to the decline of the transmission performance of the interconnect structure.

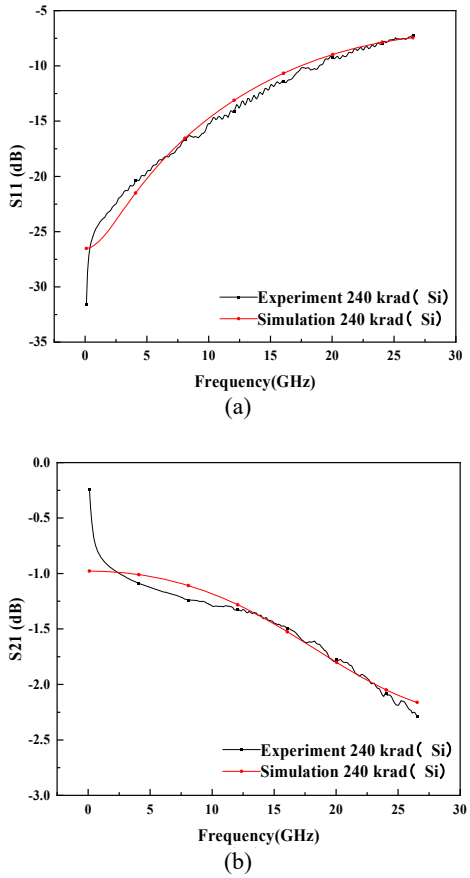


Fig. 8. S-parameters under 240 krad(Si) obtained from simulation and experiment. (a) S11 curves, and (b) S21 curves.

4. Conclusions

This study investigated the total dose effect on the electrical properties of microsystem 3D interconnect structures. The conclusions are as below:

1. As the irradiation dose increases, the high-frequency signal transmission performance of the microsystem decreases.

2. The simulation model based on the equivalent circuit method can accurately describe the variation law of the microsystem S-parameters with the irradiation dose.

3. The variation of parasitic capacitance and parasitic resistance in the equivalent circuit caused by the total dose effect is the main factor that induces the degradation of the signal transmission characteristics of the microsystem.

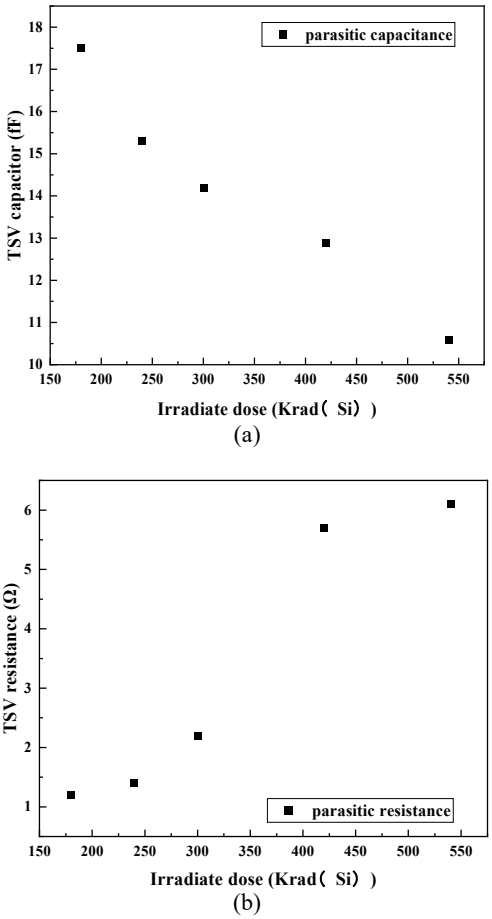


Fig. 9. The relationships between parasitic parameters and irradiation dose. (a) Parasitic capacitance, and (b) Parasitic resistance.

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Radiation Resistant Reinforcement Strategy for Three-dimensional Interconnection of Microsystems

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Summary: Concerning the radiation effects on the microsystem structure in a space environment, this work investigates the influence of the total dose effect on the transmission characteristics of high-frequency electrical signals using experimental and simulation methods. The experimental results demonstrate that the S21 curve of the microsystem decreases with the increase of the irradiation dose, indicating that the total dose effect leads to the decline of its signal transmission characteristics. A simulation model describing the total dose effect on microsystem structure was built based on the experimental test results. The simulation results show that the increase of the dielectric constant of Si during the irradiation process is the dominant factor that induces the variation of the S-parameters of the microsystem. On this basis, the radiation hardening design of the microsystem structure is proposed and evaluated by the simulation method. According to the simulation results, decreasing the height of the TSV, increasing the radius of the TSV, reducing the length of Si, and increasing the number of GTSVs have positive effects on improving the radiation resistance of the microsystem structure.

Keywords: Microsystem, TSV, Total dose effect, Simulation, Hardening design.

1. Introduction

In recent years, microsystem technology has received more and more attention [1-2]. Microsystems that combine micromachining technology and integrated circuit technology have the advantages of miniaturization, integration, high density, and low cost [3]. According to Moore's Law, integrated circuit technology must continue to shrink its feature size and improve integration [4]. However, with the increase in microsystem integration, the traditional interconnection method will cause the problem of signal crosstalk due to the increase in chip density [5]. The noise will cause the signal of the whole system to lose its logic and thus affects the entire system. At the same time, the increase in microsystem integration will lead to an increase in its power density, and the traditional interconnection method will make the reliability problems such as heat dissipation and stress more serious [6-7]. The emergence of TSV (through silicon via) can effectively solve the problems faced by traditional interconnect methods. Microsystems using TSV technology have the following advantages [8-10]: (1) Heterogeneous integration, TSV can realize the vertical connection of diverse chip electrical signals, which becomes a system with a high degree of heterogeneity; (2) Low power consumption, TSV technology uses vertical short interconnects between layers of chips, which significantly reduces the number and length of interconnections, thereby greatly reducing the power consumption of the system; (3) Low latency, TSV technology shortens the unit interconnection due to the length, thereby reducing the signal delay of the system.

With the rapid development of the aerospace industry, advanced electronic technology is gradually applied in the aerospace field [18], such as the microsystem technology in radar application. In the harsh space environment, microsystems and electronic components will be affected by various rays in space, and the radiation effect of the device must be concerned during structural design. The TSV, SiO_2, and Si layers construct a MOS (Metal-Oxide-Silicon) structure in the microsystem [19]. MOS structure will face total-dose effect, single event effect, and displacement damage effect in space [20]. The total-dose effect on the microsystem under the action of charged particles such as X-rays and γ-rays cannot be ignored [21-22]. Therefore, the 3D microsystem based on TSV technology faces severe challenges in the space environment, and it is necessary to carry out reinforcement design for its radiation effect.

The research of space radiation on 3D microsystems at home and abroad mainly focuses on the influence of the space environment on the electrical properties of TSVs. Qinghua Zeng et al. characterized the leakage current between adjacent TSVs and the coupling capacitance of array TSVs by experimental methods. The results showed that the leakage current of TSVs increased while the coupling capacitance decreased under the influence of the total dose effect. Wenchao Tian et al. summarized the research on silicon doping technology and TSV technology in recent years. The paper discusses the mechanism of high-energy heavy ions on semiconductor materials and analyzes the effect of high-energy heavy ions on TSV. Kan Li et al. studied the effect of total dose on TSV in FinFETs devices and found that TSV technology enhances the signal transmission capability of the chip and improves the radiation resistance performance of the chip. Jing Chen et al. studied the effect of space radiation on TSVs through experiments. The study found that the leakage current between adjacent TSVs increased, and the possibility

of SiO_2 layer breakdown increased due to the radiation effect. Therefore, it is necessary to study to improve the reliability of TSV in space environments.

To sum up, space radiation has a critical effect on the electrical characteristics of TSV. However, there are few domestic studies on improving the radiation resistance of the microsystems. Based on the experimental data and finite element simulation, this research builds a simulation model of the total dose effect of the microsystem structure and proposes a reinforcement strategy for radiation protection.

2. Experiments and Discussion

In this paper, a three-dimensional interconnected microsystem using TSV technology is designed according to the requirements, as shown in Fig. 1. The overall size of the microsystem is 2300 μm × 1075 μm × 700 μm. The bottom layer is made of EMC material with a height of 550 μm to support the entire microsystem. Above the EMC is a layer of PI with a thickness of 10 μm. Above the Pi is the RDL layer on the back of the microsystem. Its thickness is 7.5 μm, and above the RDL layer is Si with a thickness of 200 μm to facilitate the production of TSV and to support the TSV. TSV with a radius of 35 μm is used as a bridge to connect the upper and lower RDL layers. A 0.5 μm thick SiO_2 layer is used to insulate the signal between the TSV material and the Si material, and the uppermost layer of the entire microsystem is the front RDL. To analyze the signal transmission capability of the microsystem, the GSG-type feeding method is adopted, so the functions of TSV and RDL of the whole micro-system are divided into two types, namely communication and grounding, to prevent the signal RDL layer from being shorted to the ground RDL layer. Signal and ground RDL layers on the same plane are isolated by EMC.

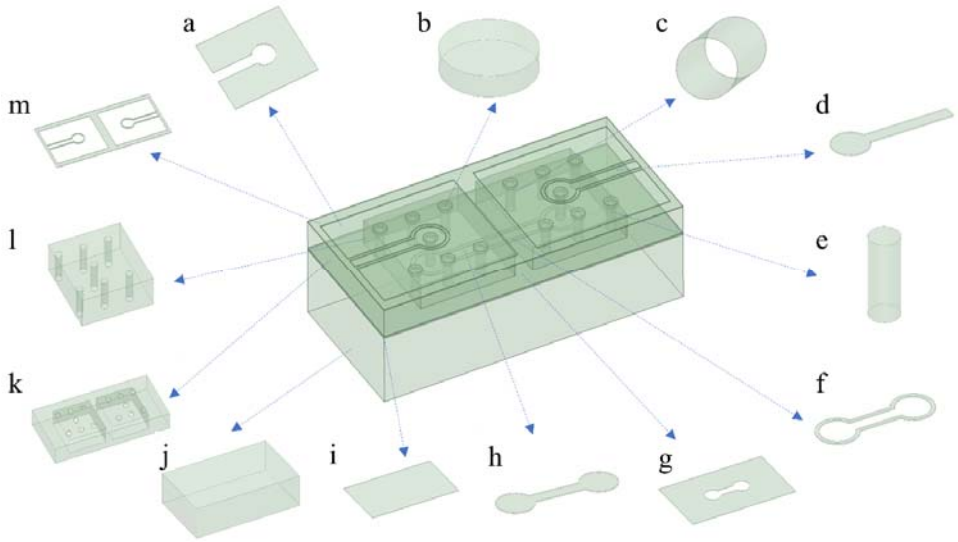

Fig. 1. Schematic diagram of microsystem structure (a, g: grounding RDL; b: bumps; c: SiO_2; d, h: signal RDL; e: TSV; f, j, k, m: EMC; i: polyimide; l: Si).

^{60}Co was used as the irradiation source in the experiments. Table 1 presents the dose rate and irradiation time of the irradiation source. A vector network analyzer is used in this paper to measure the S21 of the microsystem after irradiation at different dose points, where S21 is the forward transmission coefficient in the scattering parameters, which represent the quality of signal transmission in the microsystem. The test steps of S21 are as follows: First, install a pair of GSG-type probes on the needle seat of the probe station, and connect it with the vector network analyzer with a high-frequency transmission cable. Second, set the test frequency band of the vector network analyzer to 0.1 GHz ~ 25 GHz, and then calibrate the vector network analyzer with the built-in calibration software of the system. Finally, put the microsystem sample on the stage and conduct the test using the probe. As shown in Fig. 2, the S21 signal of the specimens is all descending curves as the test frequency increases. When the irradiation dose is 240 krad(Si), the S21 curve of the sample is similar to that of the unirradiated one, indicating that the total dose effect has little influence on the electrical signal transmission characteristics of the specimen. As the irradiation dose increased to 300, 420, and 540 krad(Si), respectively, the S21 curve of the sample shifted downward, indicating that the irradiation had a significant total dose effect on the specimen and reduced the signal transmission characteristics of the TSV structure.

Table 1. Irradiation dose and irradiation time.

Source and dose rate	Dose (krad(Si))	Time (min)
^{60}Co source 50 rad(Si)/s	240	80
	300	100
	420	140
	540	180

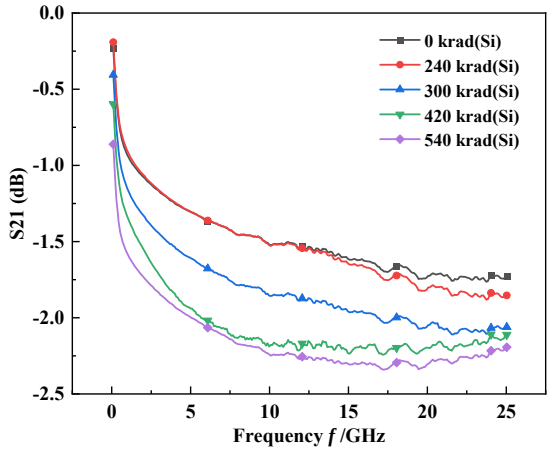

Fig. 2. S21 curves with different irradiation doses.

3. Simulation and Analysis

To investigate the total dose effect mechanism, this study uses HFSS finite element software for modeling and simulation. First, build the 3D model shown in Fig. 1 in HFSS software and define the material properties. Table 2 shows the physical property parameters of each material in the microsystem. Then define the boundary conditions and excitation conditions, and establish a vacuum interval of 3750 μm outside of the model as the simulation boundary conditions. At the same time, create a plane connecting the signal RDL and ground RDL on both sides of the RDL layer on the front of the simulation model, set the plane as the excitation mode of the lumped port, and define the integral line of the signal RDL, as shown in Fig. 3. In the simulation, the fast sweep frequency range is 0.1 GHz ~ 25 GHz, the step size is 100 MHz, the Pass is 12, and the maximum delta S is 0.01.

Fig. 4 is a comparison diagram of the S21 curve simulation results of the unirradiated samples and the experimental test results. As shown in the figure, the S21 curves of both decrease with the increasing frequency. And the simulated and measured S21 values are similar at each frequency point, indicating that the simulation model can reflect the characteristics of the actual electrical three-dimensional microsystem. During the irradiation process, the geometric size of the sample does not change, so the influence of the total dose effect on the electrical performance parameters of the specimen is mainly induced by the change of material parameters caused by irradiation. According to the research on related materials, the radiation effect affects the dielectric constant of Si material. At the same time, this paper studies the influence of irradiation effect on the scattering parameters of 3D microsystems through simulation. The dielectric constant of Si material in 3D microsystems is the most sensitive under an irradiation environment, which is consistent with the reports in related literature. Therefore, in this paper, the dielectric constant of Si was used as the variable parameter in the HFSS software. The simulated S21 was fitted with the experimental results with different irradiation doses by varying the dielectric constant of Si. Fig. 5 shows the S21 of the 3D microsystem at irradiation dose points of 240 krad(Si), 300 krad(Si), 420 krad(Si), and 540 krad(Si). It can be seen from the figure that by changing the dielectric constant of Si, the simulated S21 can fit well with S21 at each irradiation dose point.

Table 2. Physical parameters of the materials in the model.

Material	Relative permittivity	Relative permeability	Conductivity (siemens/m)
Si	11.9	1	0
EMC	3.7	1	0
Cu	1	0.999991	58000000
SiO_2	3.9	1	0
pi	3.2	1	0

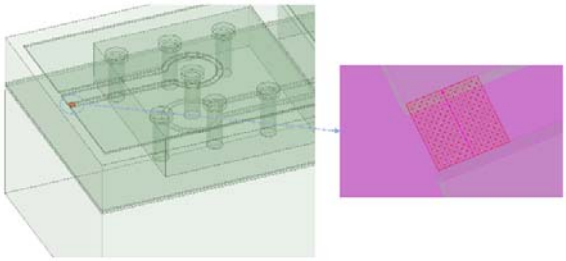

Fig. 3. Schematic diagram of the excitation conditions and integral line direction in the model.

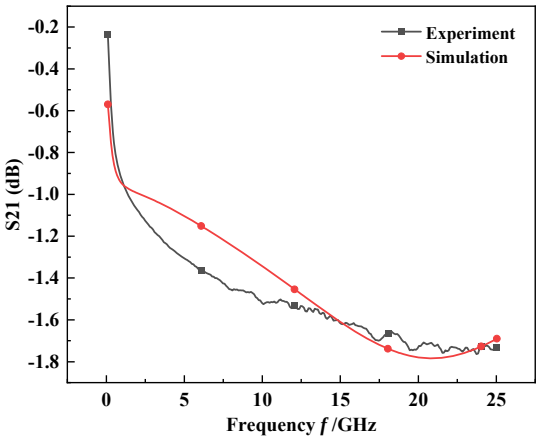

Fig. 4. S21 curves from experiment and simulation.

It is clear that by changing the dielectric constant of Si in the simulation model, the output S21 simulation results accurately match the test results under different irradiation doses. Consequently, the variation of the dielectric constant of Si during the irradiation process is the dominant factor that induces the change in the electrical signal transmission performance of the microsystem. Fig. 6 shows the dielectric constant of Si under different irradiation doses obtained based on the simulation and experimental data fitting method. It is clear that with the increase in the irradiation dose, the dielectric constant of Si shows a logarithmic growth trend. When the irradiation dose increased from 0 to 540 krad(Si), the dielectric constant of Si varied from 11.9 to 13.4.

Based on the theory of particle-material interaction, charged particles will interact with Si materials and cause ionization damage to Si materials. The dielectric constant describes its ability to hold an electric charge. With the increase of the irradiation dose, the number of holes formed in Si due to the ionization of charged particles increases, which improves the ability to retain charges. Therefore, the variation of the dielectric constant of Si is the dominant factor leading to the decrease of the electrical signal transmission capability of the microsystem with the increase of the irradiation dose.

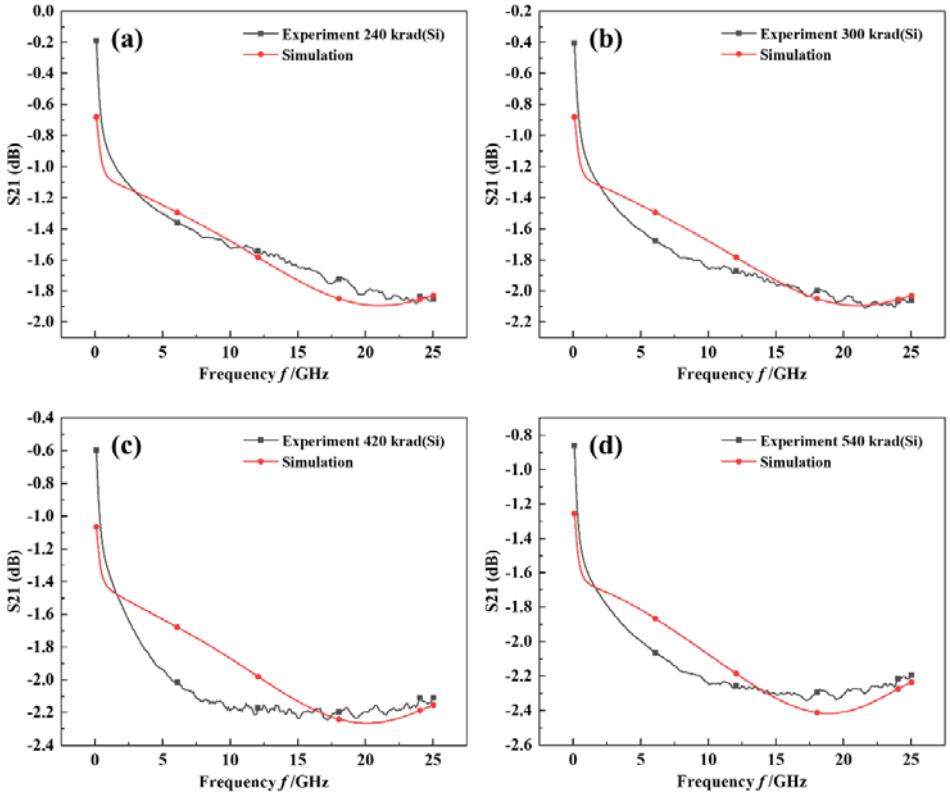

Fig. 5. S21 curves from experiment and simulation with the irradiation dose of (a) 240 krad(Si), (b) 300 krad(Si), (c) 420 krad(Si), and (d) 540 krad(Si).

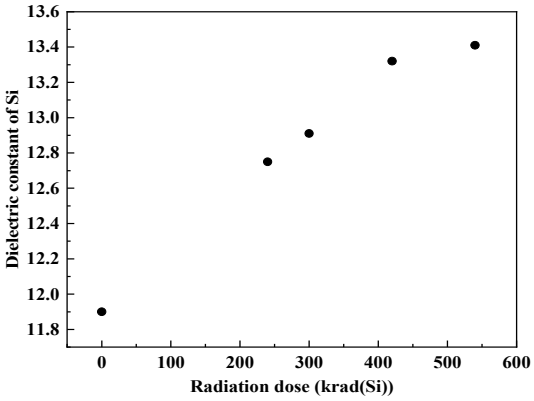

Fig. 6. Relationship between irradiation dose and the dielectric constant of Si.

4. Radiation Hardening Design and Evaluation

The above research work has built a simulation model describing the total dose effect of the microsystem. This model is helpful in the radiation hardening design of the microsystem structure. Previous research results indicated that the change of the dielectric constant of Si under the total dose effect is the main factor leading to the decrease in the signal transmission capability of the microsystem. Therefore, decreasing the volume of Si by reducing the height of the TSV, increasing the radius of the TSV, reducing the length of Si, and increasing the number of GTSVs is considered in the radiation hardening design.

To evaluate the hardening efficiency, |ΔS21| is introduced as an index. This data is the absolute value of the difference in S21 before and after irradiation. For example, Fig. 7(a) shows the simulation results of the S21 curve of the microsystem under different irradiation doses. Select S21 irradiated at 540 krad(Si), subtract S21 of the unirradiated microsystem at the same frequency point, and take the absolute value of the difference to obtain |ΔS21| under this condition, as shown in Fig. 7(b). In the following work, modify the geometry in the model, such as reducing the TSV height, increasing the TSV radius, reducing the Si length, and increasing the number of GTSVs, and obtain the S21 curve and |ΔS21| after 540 krad(Si) irradiation through simulation.

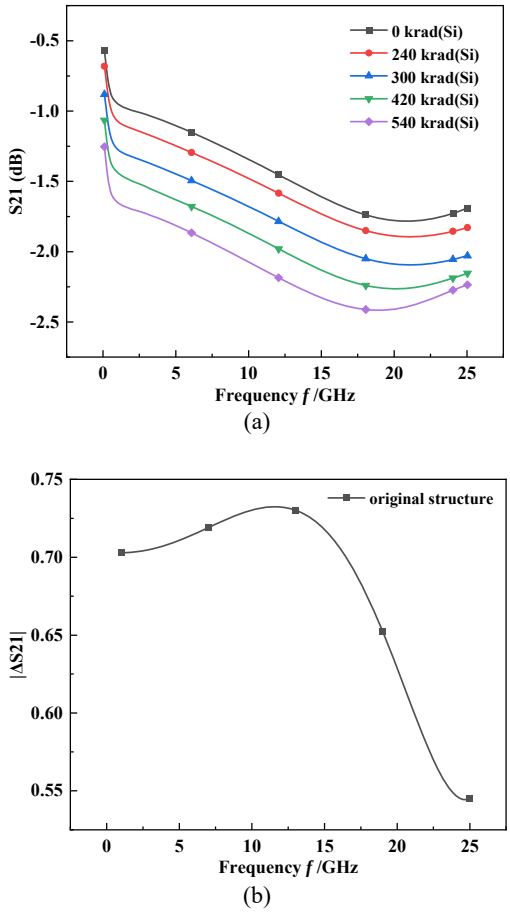

Fig. 7. S21 and |△S21| curves. (a) S21 of the specimen with various irradiation doses, (b) |△S21| obtained from (a).

Fig. 8 shows the |△S21| obtained by simulation under different structural designs when the irradiation dose is 540 krad(Si). It can be seen from the figure that in the frequency range of 0.1 GHz ~25 GHz, by reducing the height of TSV, increasing the radius of TSV, reducing the length of Si, and increasing the number of GTSV, |△S21| can be reduced. It shows that the above structure optimization can improve the radiation resistance of the electrical signal transmission of the microsystem. Among them, the most significant reduction of |ΔS21| is to reduce the length of Si. Previous findings suggest that Si is the most sensitive to the total dose effect. Reducing the volume of Si can reduce the cross-section of the reaction between the radiation particles and Si, thereby weakening the influence of the irradiation effect on the electrical signal transmission of the microsystem. In addition, reducing the height of the TSV and increasing the radius of the TSV and bump can improve the radiation resistance of the microsystem. The transmission properties of high-frequency electrical signals are related to these parameters. Decreasing the height of TSV and increasing the radius of TSV and bump can enhance the signal transmission and reduces the interface reflection. These improvements mitigate the effects of environmental factors such as radiation on its performance. In addition, the above-mentioned structural design indirectly reduces the volume ratio of Si in the structure, which also has some effects on the radiation resistance reinforcement of the microsystem.

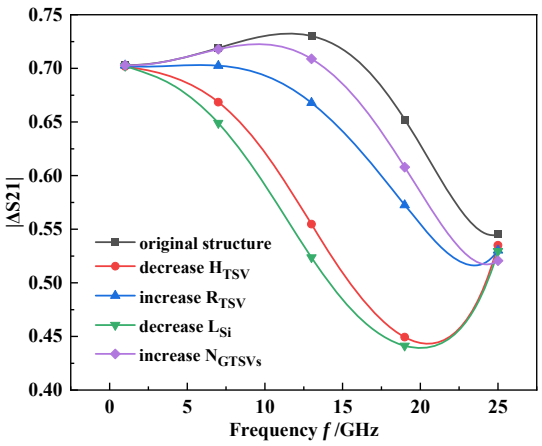

Fig. 8. |△S21| curves with various radiation hardening designs.

5. Conclusions

This study investigated the effects of irradiation on 3D microsystem structure using experiments and simulation methods. Based on the simulation models built in this work, some hardening designs were proposed and evaluated. The results obtained are as follows:

1. There is a total dose effect on the microsystem structure in the irradiation environment, resulting in a decrease in the S21 curve under the irradiation test.
2. Based on the experimental results, a simulation model is constructed, which describes the total dose effect on the microsystem structure.
3. Irradiation leads to an increase in the dielectric constant of Si, which is the dominant factor in reducing the signal transmission ability.
4. Decreasing the height of the TSV, increasing the radius of the TSV, decreasing the length of Si, and increasing the number of GTSVs is beneficial to improve the radiation resistance of the electrical signal transmission of the microsystem.

Acknowledgements

The authors would like to thank Postgraduate Research & Practice Innovation Program of Jiangsu Province under Grant No. SJCX21_1574.

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(025)

A Compact E-shaped Millimeter-wave Antenna with Bandwidth Enhancement Based on Through Glass Vias (TGV)

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Summary: In order to improve the shortcoming of microstrip antenna bandwidth, a compact E-shaped millimeter-wave antenna with bandwidth enhancement based on Through Glass Vias (TGV) is proposed. The antenna unit adopts a single layer E-shaped microstrip antenna patch and fed by TGV probe. Porous are prepared on the glass substrate by TGV and filled with metal by electroplating to form a method like coaxial feed, which achieve bandwidth enhancement and antenna miniaturization. Besides, by loading two symmetrical slots on the rectangular microstrip antenna to obtain double resonance points, further realization of broadband characteristics. Ultimately the proposed antenna acquires 20 % bandwidth (from 32.52 to 38.98 GHz), the gain is stable with a maximum of 6.4 dB and the radiation efficiency can reach a maximum of 94 % in the operation band. Moreover, the half-power beam width of the antenna is 98°, 101° and 86°at 34 GHz, 36 GHz and 38 GHz, respectively. And the cross-polarization level below -40 dB. The size of the antenna is 0.52 λ_0 × 0.35 λ_0 × 0.052 λ_0, which realized miniaturized package antenna.

Keywords: Millimeter-wave, Microstrip antenna, E-shaped; Bandwidth enhancement, TGV probe, Package antenna.

1. Introduction

Millimeter wave meets the requirements of small size target detection, high resolution imaging and space target recognition [1]. Meanwhile, various new applications put forward higher requirements for advanced packaging [2-4]. Through Silicon Via (TSV) based silicon material is a semiconductor material. When the transmission line transmits the signal, the signal and the substrate material have strong electromagnetic coupling effect, and eddy current phenomenon occurs in the substrate, resulting in poor signal integrity [2-4]. TGV based glass converter board are often used in 2.5D, 3D integrated circuit packaging design due to high thermal expansion coefficient, low dielectric constant, and ultra-thin processing manufacturability [2-4]. A large number of researchers have carried out relevant TGV technology research, such as glass-based integrated waveguide, filters, RF module, etc. [2-4].

Millimeter wave microstrip antenna has outstanding advantages in integration: small size, light weight, low profile, easy conformation, and easy to integrate with active devices and microwave circuits as an integrated RF front-end [2-5]. The common microstrip patch antenna can be divided into probe feed, aperture coupling feed and microstrip line coplanar feed [5]. In the aperture coupling feeding mode, the feeder network is separated from the radiation patch by ground, which weakens the disturbance of the feed network to the antenna radiation pattern. The pattern has good stability in the whole frequency band, but this feeding mode adopts the form of multi-layer microstrip, which increases the complexity of the structure [5, 6]. The microstrip line coplanar feed structure is simple, and easy to realize the integrated design of feed network and radiation unit, meanwhile the cross-polarization performance is not high, but the feed network also produces radiation that affects the overall radiation pattern of the antenna [7]. The application of traditional coaxial feed is severely limited by the antenna size [7].

In this communication, a single layer E-shaped microstrip patch antenna based on TGV-fed, which effectively broadens the impedance bandwidth. By loading two symmetrical slots on the rectangular microstrip antenna to obtain double resonance points, further realization of broadband characteristics.

2. Antenna Design

Fig. 1 illustrates the configuration of the proposed E-shaped antenna, which consists of a rectangular radiating patch with two symmetrical slots. BF33 (BOROFLOAT, SCHOTTAG) denoted ***Substrate*** is utilized directly. BF33 glass wafer has a relative permittivity of 4.8 and a dielectric loss tangent of 0.01, thickness of single-layer glass is 0.15 mm, and substrate is stacked with three layers of glass to increase antenna bandwidth. The antenna radiator is E-shaped microstrip patch and fed by TGV probe. The seed layer pattern (the thickness is ~20 nm) is obtained by photolithography and magnetron sputtering, and

then the thickness of 0.02 mm microstrip antenna patch is obtained by electroplating [3, 4]. The back of the substrate also adopts the method to form a large area of ground surface. The TGV probe was formed by laser induced and wet etching with an aperture of 0.03 mm [3, 4]. The copper seed layer was prepared by magnetron sputtering and then filled by electroplating. The optimized size is shown in Table 1.

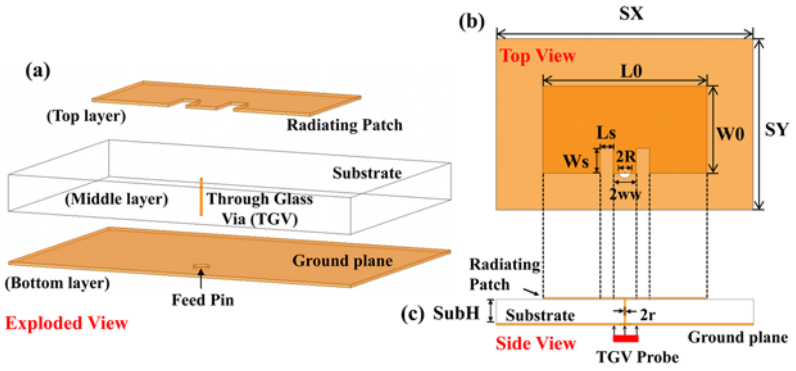

Fig. 1. Geometry of the E-shaped antenna.

Table 1. Parameters of the E-shaped antenna.

Relative Permittivity	Dielectric Loss Tangent	Parameoters	SX	SY	L0	W0	SubH	Ws	Ls	ww	R	r
4.8	0.01	Value (mm)	4.5	3	2.87	1.53	0.45	0.23	0.44	0.15	0.175	0.026

3. Simulation Results and Analysis

Two symmetrical slots on the E-shaped microstrip antenna change the resonance characteristics of the original rectangular microstrip antenna. Specifically, the slots elongate the current path of the upper and lower edges of the microstrip antenna. Making the antenna change from the original single resonance circuit to double resonance circuit, so as to meet the requirements of expanding the bandwidth. Fig. 2(a) illustrates the impedance bandwidth of the E-shaped patch antenna. Through the simulation result of reflection coefficient (|*S11*|) and VSWR curve, the impedance bandwidth is significantly enhanced due to the existence of double resonant points. Ultimately acquires 20 % bandwidth (from 32.52 to 38.98 GHz). Compared with the traditional rectangular patch (microstrip line coplanar feed), the improvement is about 2 times. Fig. 2(b) illustrates the simulation of the antenna gain and radiation efficiency of antenna. With the increase of frequency, the equivalent aperture surface of antenna increases, and the gain shows a trend of first rising and then falling. In the range of 32.52~38.98 GHz, the gain variation is less than 2 dB and meets the requirements of broadband applications. In the operation band, the radiation efficiency is above 88 % and reaches the highest 94.7 % at 35.2 GHz. The antenna is compared with a conventional rectangular radiation patch, as shown in Fig. 3(a) and Fig. 3(b). Compared with the Re_Ant.1, the Pro_Antenna has wider bandwidth and better signal pass ability, which verifies the rationality and reliability of the design. Fig. 4 shows the main polarization and cross-polarization directions at 34 GHz. It is obvious that the cross-polarization values of E-plane and H-plane keeps below -40 dB with the increase of frequency. In addition, at 34 GHz, the half-power beam width of the antenna is 98°.

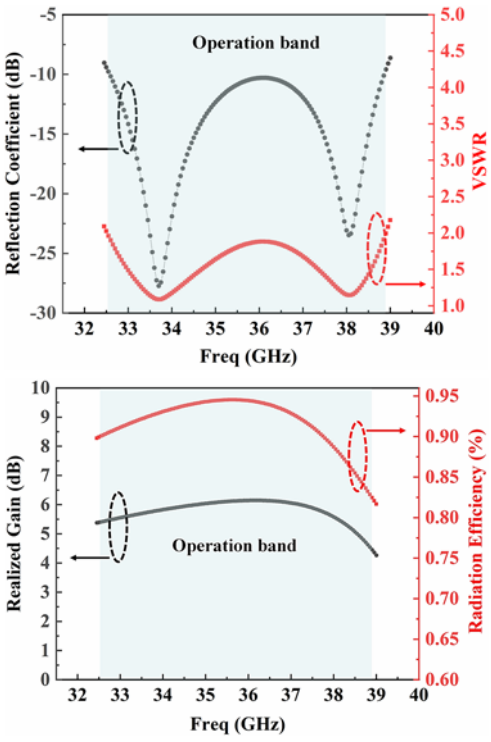

Fig. 2. E-shaped antenna simulated result of reflection coefficient and VSWR curve (left), Realized Gain and Radiation Efficiency (right) in boresight direction.

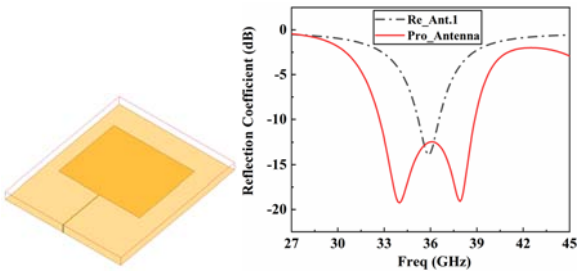

Fig. 3. Re_Ant.1: conventional patch antenna (left). Pro_Antenna: E-shaped antenna (right).

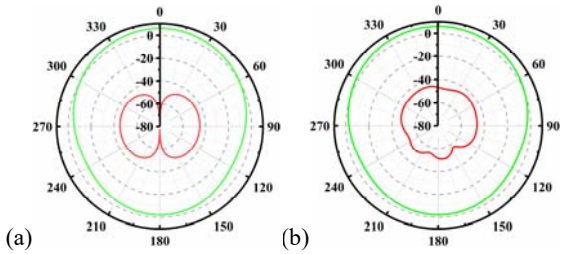

Fig. 4. Simulated radiation pattern of E-shaped antenna at 34 GHz (a) E-plane (b) H-plane.

3. Conclusions

In this communication, a glass substrate-based millimeter wave microstrip E-shaped patch antenna is proposed. Through the characteristics of double resonant frequency points, we got the impedance bandwidth is 20 % (32.52 ~ 38.98 GHz) and the cross-polarization remains very low (< -40 dB).

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(026)

Microsystem Thermal Intelligent Optimization Based on Particle Swarm Algorithm

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Summary: A particle swarm optimization algorithm-based design method was established, which is used to improve the optimization efficiency of the TSV array thermal problem in the 3D microsystem. The relationship between the design and performance parameters is obtained by finite element method simulation model. The neural network is built and trained to get the mapping relationship. Then the design parameters are iteratively optimized using the PSO algorithm, and the FEM results are used to verify the effectiveness of the algorithm. As a result, the maximum temperature is 97.90 ℃, the bump temperature is 56.01 ℃, and the TSV temperature is 31.52 ℃. The difference of optimization results between the PSO method and the FEM method is about 3 %.

Keywords: TSV, Optimization, Particle swarm optimization algorithm, Microsystem.

1. Introduction

Microsystem technology is widely used in various fields, due to its advantages of miniaturization, integration, intelligence, low cost, high performance, mass production, and so on [1, 2]. In a high-power density microsystem, Heat build -up is a growing problem [3, 4], thermal problems could affect the circuit adversely, and cause degradation of circuit performance. The main ways proposed to optimize the thermal problem in microsystems include changing TSV size, floorplan, filling materials, and adopting new structures [5, 6]. Chen Z et al. [7] simulated the thermo-mechanical reliability of TSV-based stacked packaging by means of finite element method (FEM) analysis, and analyzed the data to optimize structural parameters by the Design of Experiment (DOE) method. Hanjie Yang [8] established a multi-field coupling analysis model to study the influence of SiO_2 insulation layer, structural parameters, and insulation layer materials on the thermal stress of TSV. Traditional methods like the FEM method are mostly used for optimization problems, they are too complicated and depend on expert experience, and waste a lot of time and human resources [9, 10]. The artificial intelligence algorithm has the advantages of fast calculation speed and high calculation accuracy which is widely used in electronics, automation, management, and other industries to improve work efficiency [11, 12].

An intelligent optimization method was developed to solve complex thermal problems in microsystem by changing the structural parameters of TSV arrays. The COMSOL software is used to obtain the data of TSV arrays and performance parameters of the microsystem. Then the neural network models are trained to characterize the relationship between TSV arrays and the performance parameters of microsystem. According to the established optimization criteria, the PSO algorithm is utilized to optimize the TSV structure parameters. Finally, the effectiveness of the algorithm is demonstrated by the FEM simulation results.

2. Intelligent Optimization Method

The particle swarm optimization (PSO) method is shown in Fig. 1.

2.1. FEM Simulation

The data was obtained through FEM simulation by COMSOL software, which included TSV structure parameters and performance parameters.

The FEM software COMSOL was used to complete the 4×4 TSV FEM model, and the solid heat transfer analysis was conducted. 81 sets of data were obtained through orthogonal design, and the established neural network model was trained through the obtained data. The obtained data includes the TSV radius R, the pitch P and the insulating layer thickness t_{ox}, and the optimization targets were considered as the overall maximum temperature, bump temperature and TSV temperature [13, 14]. The research object is a 4×4 TSV array, a 20 μm thick buffer layer is additionally set (400 W/(mk)). A 50 μm × 50 μm × 10 μm chip was placed in the center of the model top; the heat dissipation rate is 1 W [15]. The bottom surface of the model was set as a fixed constraint, the temperature was 293.15 K at room temperature, and the surfaces except for the above-mentioned top surface and bottom surface were set as thermal

insulation. The specific structures of the array are shown in Fig. 2.

Referring to the manufacturing process of the TSV structure, 9 different groups of values are selected for the above three factors as their factor levels radius varies from 3 μm – 11 μm; TSV pitch varies from 25 μm – 65 μm; SiO_2 thickness varies from 0.1 μm – 0.9 μm.

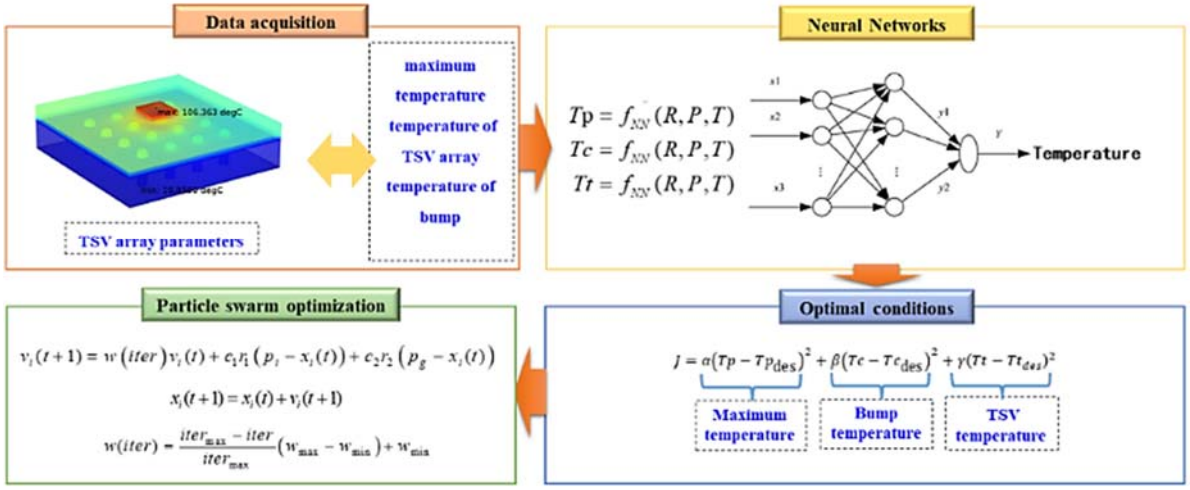

Fig. 1. Flowchart of the developed intelligent optimization.

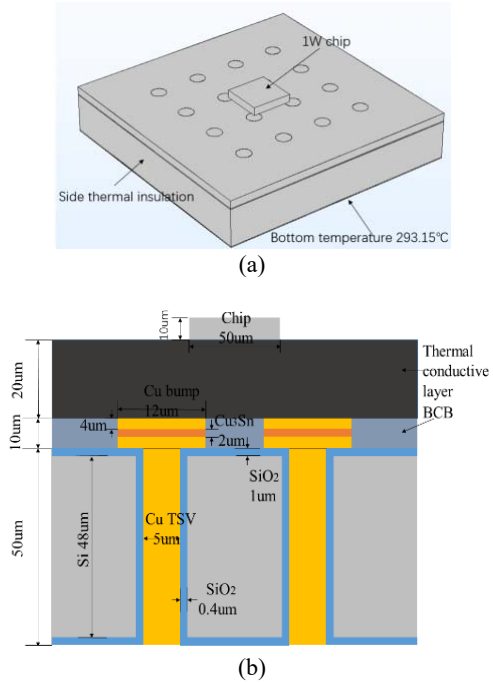

Fig. 2. Schematic diagram of TSV structure parameters: (a) Overall picture; (b) profile picture.

2.2. Neural Network Models and Optimization Criteria

The Neural Network Models were established for TSV optimal design and trained by the obtained data. The inputs of neural network were the radius of TSV, the pitches of TSV, and the thicknesses of SiO_2, while the outputs were the maximum temperature and the temperature of the TSV array and bump. Based on database training, the TSV design parameters and optimization target mapping relationship models were established.

The optimization criteria were established based on the performance parameters, including T_p, T_c and T_t. The optimization criteria J can be mathematically expressed as,

$$J = \alpha(T_p - T_{p_{des}})^2 + \\ +\beta(T_c - T_{c_{des}})^2 + \gamma(T_t - T_{t_{des}})^2, \quad (1)$$

where des is the abbreviation of design, the values of the optimization goals were as follows, the values of $T_{p_{des}}$, $T_{p_{des}}$ and $T_{p_{des}}$ are 95, 55, and 35. α, β and γ are the weight coefficients of T_p, T_c and T_t, T_p are the peak temperature, T_c is the bump temperature, and T_t is the TSV temperature.

2.3. The Structure Parameters Were Optimized by PSO Algorithm

The PSO algorithm with linear decreasing inertial weight had the excellent global and local searching ability. It was adopted in the developed method, and was expressed as,

$$v_i(t+1) = w(iter)v_i(t) + \\ +c_1r_1(p_i - x_i(t)) + c_2r_2\left(p_g - x_i(t)\right), \quad (2)$$

$$x_i(t+1) = x_i(t) + v_i(t+1), \quad (3)$$

$$w(iter) = \\ = \frac{iter_{max} - iter}{iter_{max}}(w_{max} - w_{min}) + w_{\min}, \quad (4)$$

where w is the criteria weight; p_i and p_g are the best previous positions of its particles and global particles. r_1 and r_2 are random numbers between [0,1];c_1 and c_2 are the weights of p_i and p_g; $iter$ and $iter_{max}$ are the numbers and the maximum number of iterations; w_{min} and $w_{\max}$ are the minimum and maximum of the inertia weight. The process of using the PSO algorithm with linearly decreasing inertia weight to optimize the design parameters of the TSV array in the microsystem is shown in Table 1.

In the final optimization design, the radius of TSV was 10.28 μm, the pitch of TSV was 65.00 μm, and the thickness of SiO_2 was 0.83 μm. The optimization result is shown in Table 2.

Table 1. Parameters in the PSO algorithm.

Constant parameters	Inertia weight	maximum iterations	Population size	Range of particle position	Range of particle velocity
$c_1 = 2$, $c_2 = 2$	$w \in [0.4,0.9]$	$iter_{max} = 50$	$N = 30$	$x_1 \in [3,11]$ $x_2 \in [25,65]$ $x_3 \in [0.1,0.9]$	$v_1 \in [-1,1]$ $v_2 \in [-5,5]$ $v_3 \in [-0.1,0.1]$

Table 2. Intelligent optimization and COMSOL optimization results.

Method	maximum temperature (℃)	temperature of bump (℃)	temperature of TSV (℃)
PSO	97.90	56.01	31.52
COMSOL	97.98	57.22	31.49

2.4. Verification and Discussion

COMSOL has been widely used in TSV array optimization design, and its effectiveness and accuracy have been verified. In the FEM simulation by COMSOL, the peak temperature is 97.98 ℃, the bump and TSV temperature are 57.22 ℃ and 31.49 ℃. From Table 2, the error of the maximum temperature is about 0.82 %, and the error of the bump and TSV temperature are about 2.1 % and 0.95 %, which can verify the reliability of the optimization algorithm. The main sources of errors are model errors and data measurement errors. On the one hand, in FEM simulation, lots of time and memory will be wasted because of too fine mesh division. On the other hand, the data obtained usually retain two decimal places, and errors in model building and data measurement are unavoidable. The difference in optimization results between the PSO method and the FEM method is about 3 %. The time taken for a single simulation changed from an hour to 70 s, and the efficiency has increased thousands of times.

3. Conclusions

An intelligent optimization method is proposed based on AI methods to optimize the structure parameters for microsystem with high performance. The main conclusions can be summarized as follows: Based on the data simulated by COMSOL software, the neural network models are established to characterize the relationship between the design parameters and performance parameters. The PSOalgorithm is used to optimize the radius of TSV, the pitch of TSV, and the thickness of the insulating layer. The optimized parameters are output.

The difference in optimization results between the PSO method and the FEM method is about 3 %, and the overall efficiency has increased thousands of times. So, the method proposed in this paper is an efficient and accurate TSV array optimization method, and has great inspiration for the research and design of microsystem.

Acknowledgements

This work was supported in part by the National High Technology Research and Development Program of China (no 2019YFB2204402).

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(028)

Application and Prospect of Artificial Intelligence Method in Signal Integrity Design of Microsystem

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Summary: Microsystems are widely used in 5G, Internet of Things, smart electronic devices, etc., and signal integrity determines their performance. It is vital and critical to establish fast and accurate optimization design methods for Signal integrity (SI) in the microsystem. Recently, fast and effective optimization design methods based on artificial intelligence (AI) models have drawn wide attention. In this paper, the AI methods applied in the SI design of microsystems are presented. According to different application scenarios, AI optimization design methods with different benefits are applied, which can effectively improve design efficiency and reduce the cost of optimization design. The characteristics and application fields of the presented methods are compared and discussed. Finally, the optimization design methods for SI are concluded, and their future perspectives are discussed.

Keywords: Microsystem, Optimization design, AI method, Data-driven model.

1. Introduction

The computing frequency and integration density of electronic systems used in 5G, Internet of Things (IoT), and smart electronic devices are gradually increasing. [1, 2] Microsystem technology based on three-dimensional integrated circuits (3D ICs) is considered to be one of the most promising technologies, and SI is crucial to the performance of microsystems. In the traditional SI analysis method, although the equivalent circuit model method is fast, but has a poor accuracy. The finite element method (FEM) is accurate, but it takes a long time. The SI of microsystems are influenced by multiple parameters in a small volume, and it is difficult to handle the trade-off relationship of multiple parameters using empirical and manual methods efficiently. Then, it poses new challenges to modeling and optimization-related designs. Therefore, a fast, accurate, and efficient SI model for microsystems is crucial. In recent years, AI methods have been widely concerned by many researchers and have been applied to SI design of microsystems. This paper systematically reviews the latest progress in the application of AI methods in the optimal design of microsystems, as shown in Fig. 1. The application of AI methods in the signal integrity design of microsystem interconnect structures and passive devices is introduced. The characteristics of optimization methods are systematically compared and discussed. Finally, the future development direction of the microsystem signal integrity optimization design is proposed.

2. AI in Interconnect Structure Design Optimization

In high-performance microsystems, the optimization of interconnect structure design parameters is an important guarantee for high-quality signal transmission. Frequency response characteristics and time-domain (TD) responses are important indicators for evaluating the transmission performance of interconnect structures. The design parameters of interconnect structures have complex dependencies with balanced effects on reflections, insertion loss, crosstalk, and eye diagrams of the interconnect structure. There are the following problems when using traditional optimization methods: (1) To optimize the frequency response and time-domain characteristics, a large number of electromagnetic simulations are often required, resulting in low optimization efficiency and long time; (2) As the number of design parameters to be optimized simultaneously increases, the trade-off relationship between design parameters becomes more complicated, which greatly increases the design cost and makes it difficult to achieve the overall best transmission performance. Therefore, under the mutual constraints of multiple parameters, it is necessary to use an efficient and accurate method to optimize the signal transmission structure. AI methods have received extensive attention due to their unique advantages in multi-parameter optimal design and nonlinear fitting, providing new opportunities for efficient and accurate optimal design. At present, many AI methods have been applied to the high-speed interconnect structure of microsystems, providing an efficient and accurate multi-parameter compromise design and optimization method, which shortens the design cycle to a certain extent.

In order to optimize the high-speed channel structure quickly and accurately, an artificial neural network (ANN) is applied to the optimal design of the channel RLGC matrix [3], as shown in Fig. 2(a). The neural network is trained on the training data obtained by LHS and then replaces the original slow and accurate EM model with the trained fast and accurate model. Finally, the simulated annealing algorithm is

used to optimize the structural parameters of the high-speed channel. However, as the number of design parameters affecting performance and simultaneously optimized performance parameters increases, more complex networks are required to represent the mapping relationship between design parameters and performance metrics, which requires more hidden layers. Therefore, a deep neural network (DNN) is used to construct a mapping between high-speed channel design parameters and eye diagram performance [4], as shown in Fig. 2(b). In order to ensure the accuracy of DNN, a large amount of data needs to be obtained, and the additional time cost limits the application of DNN. Then, Chen et al. [5] proposed a fast-training semi-supervised learning method based on a Hybrid Neural Network (HNN) for predicting the eye diagram of high-speed channels, as shown in Fig. 2(c). When [4] proposes the same accuracy as DNN, the proposed HNN-based method reduces the training data by 50 % and improves the eye diagram performance by 32.29 %. The number of simulations required to converge increases exponentially as the dimensionality of design parameters and performance parameters increases. Deep Partition Tree Based Bayesian Optimization (DPT-BO) [6] is proposed to optimize SI in high-speed lanes, as shown in Fig. 2(d). When constructing a neural network model for interconnect structure, the usual methods pay more attention to the nonlinear relationship between input and output and usually ignore the physical properties of interconnect structure themselves, which will lead to certain errors. Therefore, it is very important to take the physical knowledge of interconnect structure as a priori condition to build neural network models for passive devices. In order to solve the above problems, a Spectral Transposed Convolutional Neural Network (S-TCNN) combining causal enforcement layer (CEL) and passive enforcement layer (PEL) [7] is proposed and applied to the S-parameter prediction of differential PTH pair and differential Ball Grid Array (BGA) pair, and causality and passivity are improved 100 %, as shown in Fig. 2(e).

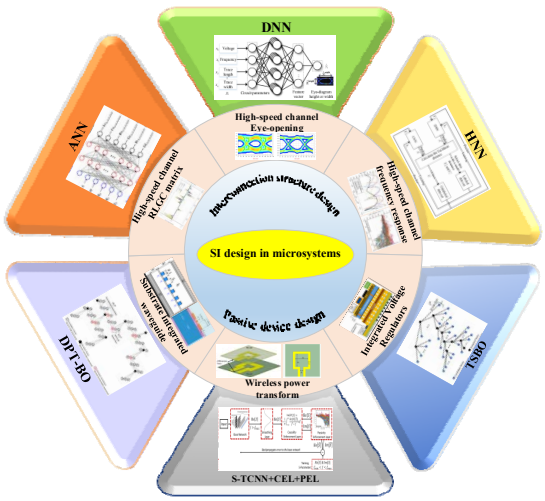

Fig. 1. AI methods of SI design in microsystem.

3. AI in Passive Device Design Optimization

Passive devices are more complex microsystem components than high-speed channels, and the increased system complexity makes them more capable of taking advantage of AI approach. Its time-domain characteristics and frequency response are a concern to many designers. Therefore, a variety of AI methods with different characteristics are applied to passive device optimization.

Wireless power transfer (WPT) is widely used in radio frequency systems. The various parts of WPT are coupled with each other, and there are conflicting design compromises in the design. It is difficult to optimize a certain stage and then cascade it, which is difficult to meet the design between each stage. It is also difficult to optimize the overall performance of the system as a whole. Therefore, two-stage BO (TSBO) is applied to the co-optimization of the system-level electromagnetic circuit of the WPT structure, as shown in Fig. 2(f), resulting in a 2.7 % increase in the end-to-end radio frequency-direct current conversion efficiency and a 52.7 % reduction in the RX coil area. [8]

Furthermore, in an integrated voltage regulator (IVR) using a solenoid inductance, the frequency characteristics of the solenoid inductance play a crucial role in the transmission efficiency of the entire IVR system. The shape structure of a solenoid inductor is determined by several geometric parameters, and the shape structure of a solenoid inductor determines its performance. When using the traditional method to optimize the performance of the solenoid inductance, it is necessary to determine the maximum density of the inductance and the optimal switching frequency in two stages. This method is difficult to guarantee the performance parameters of the solenoid inductance in terms of area, settling time, voltage drop, and conversion efficiency for the best overall performance. Aiming at the above problems, a method based on TSBO was proposed and applied to the IVR performance optimization of toroidal inductors, as shown in Fig. 2(g). The area of the toroidal inductor was reduced by 56.1 %, and the peak efficiency reached 85.1 %. [9]

When optimizing the frequency characteristics of the inductor, on the one hand, using multiple frequency points as input to train the network consumes a lot of memory, resulting in a decrease in learning efficiency. On the other hand, when using multiple frequency bins as output, this puts an additional burden on the learned weights, which can lead to overfitting. Therefore, the S-TCNN [10] method exploits the spatial correlation of points in the frequency domain to address the above challenges and is applied to the frequency characteristic optimization and co-optimization of toroidal inductors in IVR, as shown in Fig. 2(h). Compared with the traditional optimization method, the area is reduced by 51.56 % and the voltage drop is increased by 40.9 % using S-TCNN.

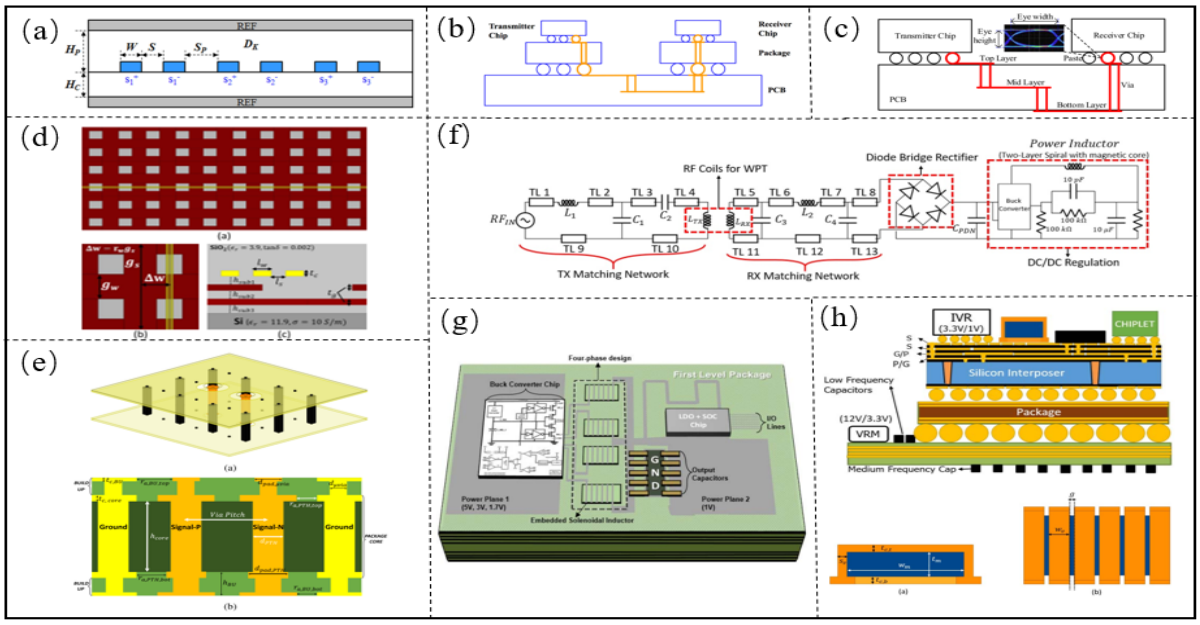

Fig. 2. (a) Three differential pairs of striplines. (Reprinted from [3]); (b) The topology of a high-speed channel. (Reprinted from [4]); (c) The structure of chip-to-chip connections. (Reprinted from [5]); (d) Structure of the high-speed channel. (Reprinted from [6]); (e) Geometry of the differential PTH structure in package core. (Reprinted from [7]). (f) Schematic of the WPT. (Reprinted from [8]); (g) Two-chip SiP IVR Architecture. (Reprinted from [9]); (h) Stack-up of the considered 2.5D integrated system and Geometry of the solenoidal inductor. (Reprinted from [10]);

4. Comparisons and Discussions

At present, many AI methods are used in the signal integrity optimization of microsystems. According to the different optimization requirements of SI in microsystems, various AI methods have different advantages and disadvantages. The application scenarios and advantages and disadvantages of AI methods for microsystem signal integrity optimization are shown in Table 1.

Table. 1. Comparison of optimization design methods for SI of microsystems.

Ref	Application fields	Design variables	Methods	Advantage	Deficiency
[3]	Optimate channel loss and crosstalk	5	ANN+GA	High speed and accuracy	Requiring a large amount of data and fewer design variables
[4]	Predict the eye-opening	8	DNN	High accuracy	Requiring a large amount of data
[5]	Predict the eye-opening	10	HNN	High accuracy, better predictive performance, and require less data	Lower speed
[6]	Optimate SI in high-speed channels, losses of SIW with air cavity, and efficiency of WPT	9-32	ADD-GP+DPT-BO	More design variables and speed	Requiring a large amount of data
[7]	Optimate the frequency response of PTH pair and BGA pair	8-13	S-TCNN +CEL+PEL	High accuracy, physical consistency, and requiring a small amount of data	Lower speed
[8]	Optimate the efficiency and area of WPT	12	TSBO	Fast convergence speed	Requiring a large amount of data
[9]	Optimization of IVR with the goal of maximizing power efficiency and minimizing area of embedded inductor.	10	TSBO	Fast convergence speed	Requiring a large amount of data
[10]	Perform multi-objective co-optimization of IVR & inductor	8	S-TCNN	High speed, accuracy, and require less data	Poor physical consistency

ANN is used in the eye diagram optimization of high-speed channels of microsystems. This method has a faster calculation speed and higher accuracy and has fewer parameters that can be optimized at the same time. It is suitable for optimization scenarios with fewer parameter dimensions. In order to improve the accuracy of high-speed channel prediction, DNN is applied to the prediction of high-speed channel eye diagrams. Since DNN has more hidden layers, it has higher accuracy and calculation speed, and it is suitable for scenarios that require high accuracy. In addition, it requires a large amount of data to ensure accuracy. HNN is used in the optimization of high-speed channels. Compared with DNN, its prediction performance is better, and the amount of data required to train the model is greatly reduced, so it is more suitable for scenarios where it is difficult to obtain original data. DPT-BO is applied to eye diagram optimization of high-speed channels, structure optimization of Substrate integrated waveguide (SIW), and transmission efficiency optimization of WPT. This method can optimize the high dimension of data at the same time, but requires a large amount of training data, and is suitable for collaborative optimization of high-dimensional design parameters Scenes. TSBO is used in the eye diagram optimization of high-speed channels. This method has a fast convergence speed and fast calculation speed and is suitable for scenarios with high-speed requirements. S-TCNN and S-TCNN+CEL+PEL are applied to S-parameter optimization of solenoid inductor coils, differential vias, and BGA pairs. S-TCNN combined with the spatial correlation of S-parameters reduces the need for training the amount of data, S-TCNN+CEL+PEL has a great advantage in expressing the passivity and causality of the optimization target. These two methods are suitable for frequency-domain optimization scenarios where the design parameters are strongly correlated and need to ensure their own physical characteristics.

5. Conclusion and Prospect

This paper summarizes and compares the application of various AI methods in microsystem signal integrity. The AI method is mainly used in the time domain and frequency domain response of high-speed channels, coplanar waveguides, spiral inductors for IVR, WPT, and frequency domain response of microwave devices, which can effectively reduce time-consuming and a large number of electromagnetic simulations caused by long time and low efficiency.

With the gradual development of microsystems towards high performance and miniaturization, AI-based multi-parameter, small-volume, high-efficiency, multi-objective compromise optimization design methods are promising. In the future, the development prospect of microsystem optimization design based on AI method is broad. The outlook should include the following aspects:

1. The generalization ability of AI methods needs to be improved.

2. Reverse design based on AI methods is more important for how to design high-performance microsystems.

3. The amount of data required to train the neural network should be reduced.

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(029)

Distributed Neural Network for Electrothermal Circuit Model of SiC Power MOSFET

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Summary: This paper presents distributed neural network (NN) for calibration of the electrothermal circuit model of power SiC MOSFET. The proposed method provides higher accuracy of nonlinear electrothermal behavior at the whole current range compared to the standard simple NN. The calibrated electrothermal circuit model is validated experimentally. Very good agreement between simulations and measurements confirms the validity of the proposed method.

Keywords: Neural network, Neural network training, Electrothermal circuit model, SiC Power MOSFET, Model calibration.

1. Introduction

Circuit simulations are powerful tools for design, analysis, and optimization of electrical circuits. However, well calibrated models are required for accurate simulation results. A lot of previous works utilize artificial neural network (NN) for electrothermal circuit modeling of power transistors [1-4]. NN for model of drain-source current I_D is created by artificial neurons connected by artificial synapses w (see Fig. 1a). Input neurons receive input values of drain-source voltage V_{DS}, gate-source voltage V_{GS}, and temperature T_j. Output neuron describes I_D current. The training of NN is performed using measured output (I_DV_D) and transfer (I_DV_G) characteristics (Fig. 1b). However, the presented models are calibrated only for the high current operation. Mid and low currents are overlooked and can cause considerable deviations.

2. Distributed Neural Network

This work introduces our proposed distributed neural network for calibration of the electrothermal circuit model of power MOSFET. The designed distributed NN provides the capability to approximate nonlinear electrothermal behavior at the whole current range with very high accuracy. The proposed model consists of two neural networks NN_1 and NN_2 (Fig. 2a). NN_1 models the shape of normalized I_DV_D curves for all combinations of V_{GS} and T_j parameters. NN_2 represents transfer characteristics of logarithm I_D at constant drain voltage V_{DSnorm} and different temperatures T_j. The logarithm of I_D allows NN_2 to fit the wide current range.

Finally, I_D is calculated as a multiple of NN_1 and the natural exponential of NN_2. NN_1 and NN_2 are created and trained in MATLAB. NN_1 consists of three inputs (V_{DS}, V_{GS}, and T_j) and one output (I_{Dnorm}).

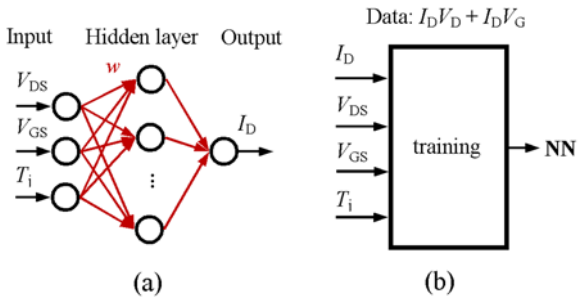

Fig. 1. (a) Schematic diagram of single neural network. (b) The training process for single NN.

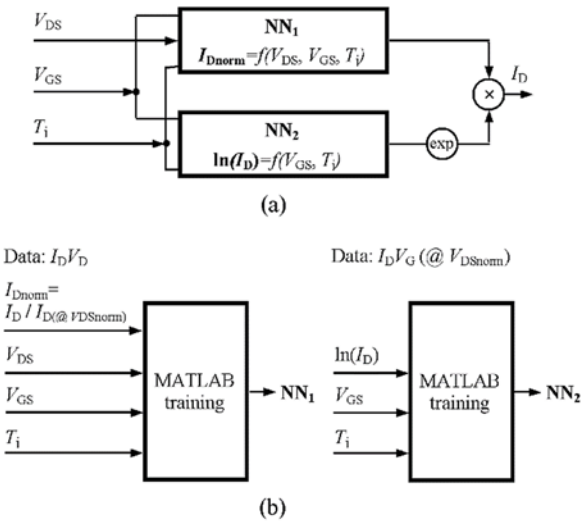

Fig. 2. (a) Distributed neural network for electrothermal circuit model of SiC power MOSFET; (b) The training process for distributed NN.

NN_2 consists of two inputs (V_{GS} and T_j) and one output ($\ln(I_D)$). The training of NN_1 is performed using measured output characteristics data. Before training each I_DV_D characteristic is normalized to I_D current at drain voltage V_{DSnorm} ($I_{D(@\ VDSnorm)}$) (Fig. 2b). Subsequently, the NN_1 is trained as a function $I_{Dnorm} = f(V_{DS}, V_{GS}, T_j)$. Measured transfer characteristics data at V_{DSnorm} is used for training of NN_2. NN_2 is trained as a function $\ln(I_D) = f(V_{GS}, T_j)$ (Fig. 2b).

3. Model Validation

The designed approach is validated on SiC power MOSFET. The device is 650 V, 100 A, SiC power transistor developed by STMicroelectronics technology [5]. Fig. 3 and Fig. 4 show the measured and simulated output and transfer characteristics of SiC power MOSFET for standard single NN and our proposed distributed NN. Very good agreement between measurement and simulation using both methods is observed for high I_D currents. A bit lower accuracy for distributed NN is caused by the multiple of NN_1 and NN_2. However, the single NN does not provide reasonable results for low currents due to the low range of sigmoid function in hidden layer neurons. The distributed NN approach gives a very good correlation. The calculated average deviation of distributed NN is about 2 %. Good agreement between simulations and measurements at low and high I_D currents operation confirms the validity of the proposed electrothermal circuit model of SiC power MOSFET and methodology for model calibration using distributed NN.

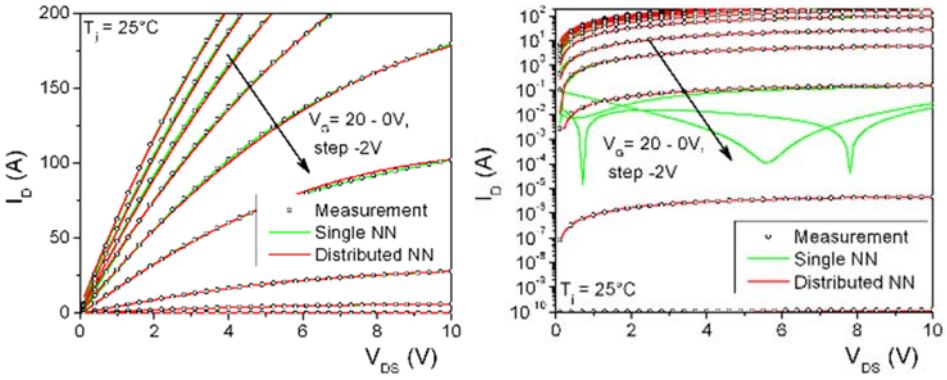

Fig. 3. Measured and simulated output characteristics of SiC power MOSFET for standard single NN and distributed NN.

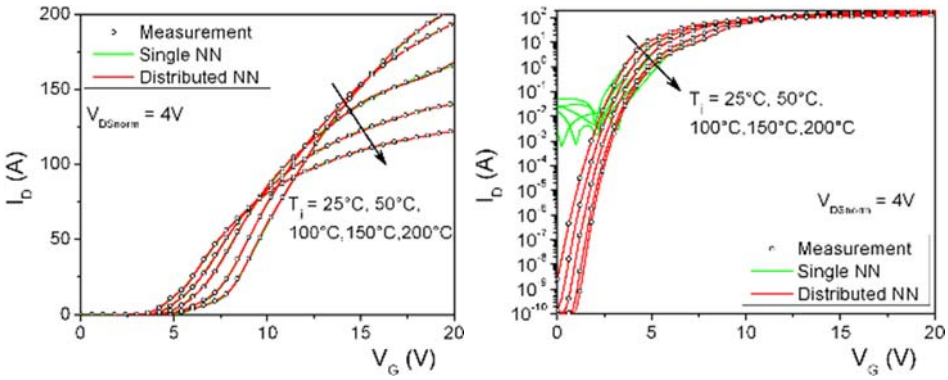

Fig. 4. Measured and simulated transfer characteristics of SiC power MOSFET for standard single NN and distributed NN.

4. Conclusions

Distributed neural network for calibration of the electrothermal circuit model of power SiC MOSFET was presented. The proposed distributed neural network provides higher accuracy of the model compared to the standard simple NN mainly for the whole current range of the device operation. The advantages of the proposed methodology are simple implementation, high model accuracy and automated model calibration of complex devices.

Acknowledgements

This project has received funding from the ECSEL Joint Undertaking (JU) under grant agreement REACTION No 783158. The JU receives support from the European Union's Horizon 2020 research and innovation program and Italy, Germany, Belgium, Sweden, Austria, Romania, Slovakia, France, Poland, Spain Ireland, Switzerland, Israel. This work was also supported by the Slovak Research and Development Agency under contract No. APVV-20-0266 and Grant

VEGA 1/0727/19 supported by Ministry of Education, Science, Research, and Sport of Slovakia is kindly acknowledged.

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(030)

Synthesis and Thermal Stabilization Properties of Phase Change Materials and Their Application in the Composite with $LiCuPO_4$

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Summary: The article presents the usage of innovative phase-change material (PCM) for thermal stabilization of a LTCC (low temperature co-fired ceramics) substrate for the application in microwave frequencies. The PCMs were obtained by encapsulating paraffin nanoparticles in SiO_2 capsules. To confirm the synthesized composite, FT-IR and DSC analysis were performed. The material was also tested by TG analysis. Experimental $LiCuPO_4$ based LTCC tape was used as a multilayer substrate with drilled channels and vias, which were filled with phase-change material after firing. The dielectric properties of the substrate were characterized in the range 10 kHz – 2 MHz ($\varepsilon_R \sim 5.3$). The increased thermal stabilization of the substrate was examined with the use of a Peltier module and a thermal imaging camera. For comparison, the tests were carried out for AlN substrates with and without PCM filling.

Keywords: LTCC technology, Phase-change materials (PCM), Paraffin, Thermal stabilization.

1. Introduction

Dynamically developing modern technologies require miniaturized electronic devices, which simultaneously assembles a need for unique substrate materials that can stabilize the temperature of electronic circuits. The heat dissipation problem in microelectronic packaging is becoming increasingly important as demands in denser and faster circuits intensify [1]. AlN is the substrate with high thermal conductivity (170 W/mK), but because of the price it is necessary to search the alternatives. Different composite materials are developed, among them LTCC (low temperature co-fired ceramics) substrates.

The possibility of miniaturization and integration of elements in a multi-layer module, flexibility in the selection of the geometry of the substrate and the reduction of its production costs is ensured by the use of LTCC technology. Moreover, the increase of the operating system frequency, as same as the speed and quality of signal transmission is required which is possible due to the densification of signal lines and the reduction of cross-line crosstalk. LTCC substrates, despite of good thermal stability can ensure low dielectric permittivity as well.

1.1. Phase Change Materials

Phase-change materials can be used to store thermal energy [2, 3]. Their encapsulation limits the leakage and thus improve their work. The key factor in encapsulating of phase-change materials is the minimization of capsule diameter, which increases the ratio of the active surface area of the PCM material to the volume of the composite, and thus stimulates the course of thermodynamic processes. Silica as a coating material has gained popularity due to its structure stability, large surface area, controlled pore size, well-defined surface properties, and non-toxic nature. Moreover, silica coatings show good thermal conductivity, which is very important for the correct operation at stabilized temperature conditions.

1.2. LTCC Technology

The aim of this study was to fabricate LTCC substrate with vertical and horizontal channels, filled with a phase-change material, which by changes of state, accumulates thermal energy, supporting the thermal stabilization of the structure. An additional advantage of the developed substrate is the possibility of folding it into a multi-layer structure with buried elements and metallization with a high coefficient of thermal conductivity. Based material for LTCC substrate i.e., $LiCuPO_4$ was chosen because of relatively low value of dielectric constant, which makes this substrate attractive for the implementation of systems operating at microwave frequencies.

2. Methodology

2.1. PCM Material Preparation

The synthesis of the paraffin-SiO_2 composite was based on the successive centrifugation processes at 70 °C of paraffin with the addition of water, SDS, then TEOS, EtOH 96 % and NH_3 (aq). Subsequent steps included cooling, filtration, sludge separation and vacuum drying for 48 hours.

2.2. LTCC Substrate Preparation

For the experiment, a tape based on $LiCuPO_4$ (synthesized at 720 °C, with initial calcination at 350 °C) was prepared. The effectiveness of the synthesis was confirmed by the thermodifractogram analysis (Fig. 1). The obtained $LiCuPO_4$ powder was used for slurry preparation. After addition of organic ingredients: isopropanol and toluene as solvents, ethylene glycol and benzyl phthalate as a plasticizer, PVB as a binder and solvent free wetting and dispersing additive – copolymer with acidic groups as dispersant, the slurry was cast in tape caster to a thickness of 450 microns. The selection of inorganic materials for the LTCC tapes was aimed at low dielectric constant and a stable value of thermal conductivity (by limiting the interfacial boundaries). For comparison purposes AlN substrate was used. The dielectric parameters of the material were characterized using LCR QuadTech meter.

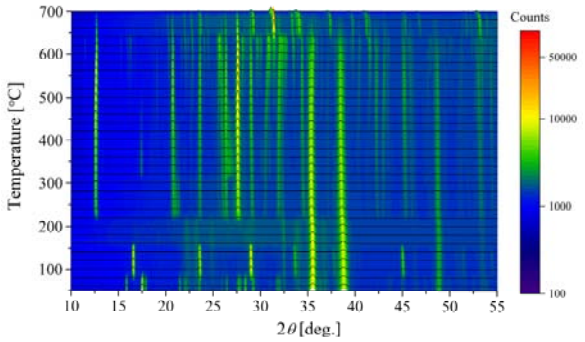

Fig. 1. X-ray thermodiffractogram of $LiCuPO_4$.

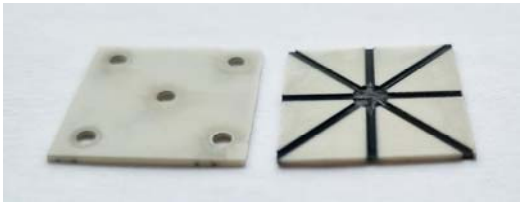

Fig. 2. Exemplary photo of AlN substrate with channels and vias arrangement (laser processing).

After drying, vias and channels were made in a multilayer $LiCuPO_4$ and AlN substrates (Fig. 2) by laser processing. The multilayer laminates were fired at 720 °C, thus obtaining a solid substrate with holes, into which PCM and epoxy resin mixture was introduced. For comparison, the same channels and vias were made in AlN ceramics.

Heat dissipation from the substrates with and without the PCM-filled channels was observed in thermal imaging camera. The samples were heated using Peltier module. As it is known from the literature the substrate modification to introduce thermal vias is limited by substrate properties such as fracture toughness. The proportion of vias should not exceed 30-50 % of the substrate volume [4].

3. Results

The FT-IR analysis shows that the spectrum of the synthesized paraffin-SiO_2 composes from pure paraffin and silica, which proves the presence of a SiO_2 capsules with immobilized paraffin inside (Fig. 3). Thermogravimetric tests revealed as well the stability of the capsules at 200 °C. Above this temperature, a slow decrease in the mass of the sample related to its decomposition begun.

The IR camera shows that the PCM-enriched LTCC substrate heats up with a delay and gradually loses heat, preventing the substrate thermal shocks (Fig. 4).

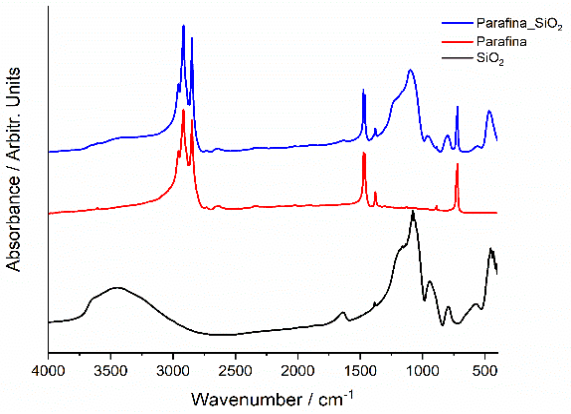

Fig. 3. FT-IR spectra of the paraffin-SiO_2 composite.

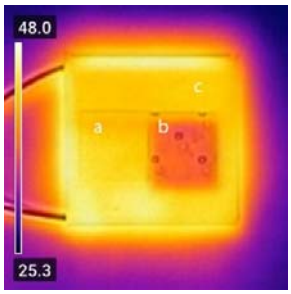

Fig. 4. Exemplary IR image: a) LTCC-substrate without PCM, b) LTCC-substrate with PCM filling, c) Peltier cell.

Additionally, measured dielectric constant of $LiCuPO_4$ LTCC material is stable and amounts to 5-6 in the frequency range 10 kHz – 2 MHz.

4. Conclusions

A new LTCC substrate based on $LiCuPO_4$ was obtained. The material was characterized by high elasticity and a smooth surface. The LTCC substrate with channels and vias filled with encapsulated PCMs shows significantly greater temperature stability during heating compared to the reference substrate and AlN, having simultaneously low dielectric constant.

Acknowledgements

The work was partially financed by the National Science Centre (project no. TECHMATSTRATEG-III/0026/2019-00).

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(031)

Study of Total Ionizing Dose on RF Microsystem

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Summary: With the increasing of chip integration level, Radio Frequency (RF) system combines more and stricter with 3D-IC, in which Through Silicon Via (TSV) plays an indispensable role. Most researchers focus on the radiation-harden technology of RF system, while ignore the impact of performance change of TSV, which affects the performance of RF system strongly. In this paper, we present a simulation methodology for the emulation of different total dose of radiation based on a simple 1D TSV capacitance model with the COMSOL Multiphysics software, which could save a lot of time and costs on irradiation experiments. In simulation, both low-frequency and high-frequency C-V curves are computed, to verify the simulation results, irradiation experiment based on three types of TSV chips designed is made. At the irradiation dose of 30 Krad, 90 Krad, 150 Krad, S21 parameters after irradiation degrade for 0.2 dB, 0.6 dB and 0.8 dB respectively. In irradiation environment, the C-V characteristic curve of TSV drifts to the left, the capacitance value of TSV under the same bias voltage reduces after irradiation, meanwhile the transition performance of TSV degrades. The simulation methodology and irradiation experiment prove a relatively accurate method for assessing performance of RF system under irradiation environment, which could also assess the effect of TID effect on structures similar to TSV in RF system, like TSC (Through-Silicon Capacitor).

Keywords: Total Ionizing Dose (TID) effect, Fixed oxide charge, TSV capacitance model, TSV chip, COMSOL simulation.

1. Introduction

Radio Frequency (RF) circuit is a significant part in RF system, which have been widely used in wireless corresponding area and RF identification, including 5th generation wireless systems (5G), artificial intelligence (AI), aerospace research and so on. RF chip plays an important role in wireless corresponding, take RF transceivers for example, which definitely minimize the Radio system, even the almost conservative space industry identifies the benefits of RF chip. With the growing demands and progress of circuit manufacture, new technology such as three-dimension integration technology have been being applied in RF chip, using three-dimension integration technology, the delay and power of RF system decrease definitely, thus SOC with complex functions could be realized.

In the aerospace industry and nuclear industry, the effect of irradiation on RF system cannot be ignored. In 2020, a new Radiation-Tolerant-IC design method was proposed, the proposed device based on I-gate structure could be fabricated in the standard CMOS process. The proposed RTIC full custom design is an efficient solution for ASIC design than the conventional procedure, a highly reliable RTIC can be easily implemented. [1] In 2021, J. Feng studied the effects of total ionizing dose (TID) radiation on an 8-transister global shutter exposure complementary metal-oxide semiconductor image sensor (CIS) within a star sensor, revealed the transfer mechanism of CIS parameter degradation to star sensor parameter degradation. [2] In 2014, TID effect on partially depleted (PD) SOI nMOSFETs is investigated, researchers observed the radiation-induced coupling effect due to the metamorphosis of PD device. To suppress the radiation-induced coupling effect, the back-channel implantation is introduced as an effective way. [3] In 2020, J. Budroweit investigated TID effects on a highly-integrated radio frequency (RF) agile transceiver to ultra-high dose levels, especially the irradiation dose malfunctions occur on the digital interface of DUT, and the annealing effect. [4] Most researches on radiation effect are based on nMOSFETs, CMOS-IC or the whole system, while few studies on the radiation resistance reliability of TSV, a critical part of RF system utilized 3-D integration technology.

When it comes to the research on TSV, Li Yanruoyue and his team [5] used finite element method to determine the effects of thickness of SiO2 layer on the distribution of thermal stress. Zao Liu [6] have proposed a simple yet accurate physics-based analytical thermal resistance model for lateral TSV thermal resistance. Their research shows that lateral TSV model is not only a function of the geometry of the TSV such as radius and thickness of liner, but also strongly depends on the space between TSVs because of changes in the isothermal curves when TSVs are placed at different locations with respect to each other. Gudi Chen [7] analyzed the effect regular of pulse frequency, oxide thickness and radius of TSV size on thermal stress. The simulation results show that, under the same pulse frequency, the thermal stress of poly-silicon materials are better than that of tungsten and copper materials in conical TSV. According to some researchers, the SiO2 thickness may influence the thermal conductivity of TSV [8]. To sum up, when studying TSV, most researchers focus on the electrical, thermal and stress aspects of TSV. As a critical structure in RF circuit utilized 3-D integration technology, especially which holds the potential to be

widely used in the aerospace industry and nuclear industry, studying the radiation resistance reliability of TSV becomes necessary.

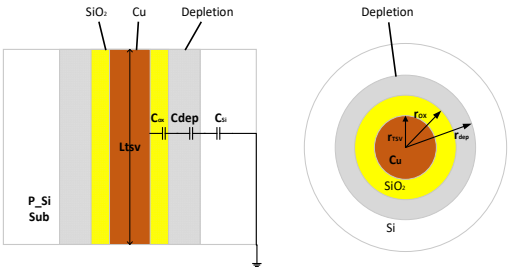
In this paper, we propose a simulation methodology for the emulation of different total dose of radiation and different insulator thickness, and verify the TID effect on the capacitance characteristics of TSV based on manufactured conventional TSVs.

Firstly, structure and characteristics of TSV is introduced. Secondly, finite element analysis method utilized in the investigation is recommended and TSV model are established in this part. Thirdly, three types of TSV are designed and manufactured, meanwhile, the irradiation experiment based on the above TSVs is designed. After radiation, the S parameter of TSVs is measured. Finally, the results of the simulations and tested are analyzed and discussed. Some conclusions are drawn based on the research.

2. Theoretical Analysis

2.1. Structure of TSV

With the development of 3D integration technology, as the most important part of 3D-IC, new types of TSV are invented, level of TSV manufacture keeps growing, the conventional TSV is widely used, thus the research based on conventional TSV is still significant currently. Fig. 1(a) and (b) shows the longitudinal section of a conventional TSV and the cross sections of a TSV biased in the depletion regions, respectively. The material used for TSV's core is Cu, with an annular dielectric barrier typically of silicon dioxide (SiO_2) surrounding the copper cylinder. And the whole structure is built on p-type silicon substrate. The above three parts are consistent with the traditional TSV structure, and the coaxial TSV is formed by wrapping another layer of copper on the outside of the traditional TSV structure.



(a) Longitudinal section (b) Cross sections

Fig. 1. TSV Architecture.

2.2. Total Ionizing Dose Effect in SiO_2

Total ionizing dose affects TSV in the following ways. Radiation induces excess electron hole pairs in the insulators. Equation (1) shows the number of pairs generated per unit dose in a given oxide volume. The electrons are more mobile. And they exit, leaving hole charges. The hole charge is trapped in the oxide in deep level traps, and then moves very slowly by hopping from trap to trap.

$$g\left[\frac{ehp}{cm^3 rad}\right] = 100\left[\frac{erg}{g}\right]\left[\frac{1}{rad}\right]\cdot\frac{1}{q}\left[\frac{eV}{erg}\right]\cdot\frac{1}{E_p}\left[\frac{ehp}{eV}\right]\cdot\rho\left[\frac{g}{cm^3}\right] \quad (1)$$

In the equation, $q = 1.6\times1012eV\bullet erg^{-1}$, refers to the elementary charge, $E_p = 17eV^{-1}$, refers to the mean ionization energy of the SiO_2, $\rho = 2.2g\bullet cm^{-3}$, refers to the material density of SiO_2.

Trapped holes, basically they get trapped in deep traps, very close to the interface, alter the surface carrier concentrations in silicon. And holes and protons that move to the interface create additional defects at the interface. This trapped charge and interface defect change the local carrier population and reduce carrier life-time near the surface of the SiO_2 silicon interface.

The total density of positive fixed charge accumulated in the oxide can be calculated as a function of the total dose (D) by means of equation (2).

$$\Delta N_{ot} = D\cdot g\cdot f_{ot}\cdot f_y\cdot t_{ox} \quad (2)$$

In the equation, t_{ox} is the thickness of oxide layer. f_{ot} is the hole trapping efficiency, and it can be assumed as a fitting parameter that should be empirically determined. (E_{ox}) is the fractional yield. It depends on the electric field in the oxide at the moment of irradiation, and can be calculated by means of equation (3).

$$f_Y\left(E_{ox}\right) = \left(\frac{|E|+E_0}{|E|+E_1}\right)\cdot m, \quad (3)$$

where $E_0 = 0.1\ V/cm$, $m = 0.7$ and $E_1 = 0.55\ MV/cm$, for gamma ray Co-60 sources [9]. As can be seen from Equation (3), $\triangle N_{ot}$ is proportional to the thickness of the oxide layer. Therefore, for TSV structures with thick oxide layers, the total density of interface trap (Nit) caused by radiation can be ignored.

The charge in the oxide can be calculated by means of equation (4).

$$Q_{ot} = q\cdot\Delta N_{ot} \quad (4)$$

2.3. The Capacitance of TSV after Radiation

For a TSV with length h, Cox can be expressed by the cylindrical capacitor formula (5):

$$C_{ox} = \frac{2\pi\varepsilon_{ox}h}{\ln\left(\frac{r_{ox}}{r_{TSV}}\right)}, \quad (5)$$

where ε_{ox} is the permittivity of SiO_2; r_{TSV} is the radius of the TSV conductor; r_{ox} is the radius of the outer surface of the TSV oxide liner.

The depletion capacitance of a single TSV can be obtained by formula (6)

$$C_{dep} = \frac{dQ_s}{d\varphi(r_{ox})}, \quad (6)$$

where $\phi(r_{ox})$ is the surface potential at Si-SiO_2 interface (r = r_{ox}), could be calculated with N_a, r_{dep} and r_{ox}.

Then the total capacitance of TSV C_{TSV} is the series combination of the oxide and depletion capacitance, and it can be expressed as

$$C_{TSV} = \left(\frac{1}{C_{ox}} + \frac{1}{C_{dep}} \right) \quad (7)$$

TSV is a kind of MOS structure, which works at a different area, as accumulation, depletion, and inversion regions, with different bias voltage and frequency of signals.

3. Simulation Methodology

3.1. Characteristics of TSV and Modeling

Finite element analysis (FEA) uses mathematical approximations to simulate real physical systems. By using simple but interacting elements, a finite number of unknowns can be used to approximate the real system of infinite unknowns. COMSOL Multiphysics, a FEA software, is widely used because of its ability to combine multiple physical fields and simulate results close to reality. Therefore, the model of TSV capacitance was established by COMSOL Multiphysics.

As mentioned in the previous section, we choose a structure of conventional TSV as the research object. The main structure consists of three basic parts: a conductive filling layer, the oxide insulating layer, p-type silicon substrate and the outermost shielding copper layer. They will be introduced in detail as follows. The diameter of TSV is 5 microns, and the inner insulation layer thickness is 0.5 micron.

In steady state, it is assumed that the charge density is equal within the lamellar at the same height. Therefore, we can take a plane perpendicular to the axial direction of the TSV for simulation to simplify the model. Furthermore, it can be considered that the capacitance between the TSV core layer and p-type substrate is equal everywhere along the radial direction. Therefore, the part along any radial direction can be modeled to further simplify the model. Then, we built a 1D modeling of TSV (the p-type) in COMSOL, as shown in Fig. 2. In the model, we chose the semiconductor interface in COMSOL. First, we established a line segment and two endpoints to represent the structure of the inner core layer. The left endpoint was set as a thin insulating gate, whose thickness was d_{ox}, the surface charge density was rhos_ox, and the right endpoint represented the ideal Ohmic contact.

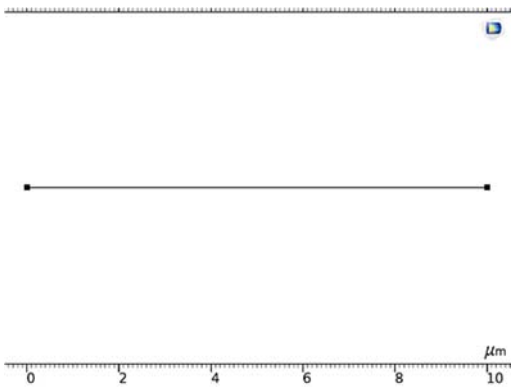


Fig. 2. 1D modeling of TSV (the p-type) in COMSOL.

3.2. Simulation

In order to analyze the effect of irradiation on the capacitance, firstly, we simulated different radiation doses to TSV at low and high frequency when the thickness of the oxide layer and the doping concentration of the substrate were constant, so as to study the effect of irradiation dose on the capacitance of TSV.

4. Analysis of Simulation

First, we simulated the C-V characteristic curves of TSV capacitance with p-type substrate concentration of $5 \times 10^4\ cm^{-3}$, oxide thickness of 200 nm, frequency of 0.0001 Hz and 1e7 Hz, and total radiation dose of $0\ rad$, $1 \times 10^5\ rad$ and $3 \times 10^5\ rad$, respectively.

As shown in Fig. 3(a) and Fig. 3(b), after TSV is irradiated, the c-v characteristic curve of TSV capacitor drifts to the left. The higher the radiation dose, the more the curve drifts to the left.

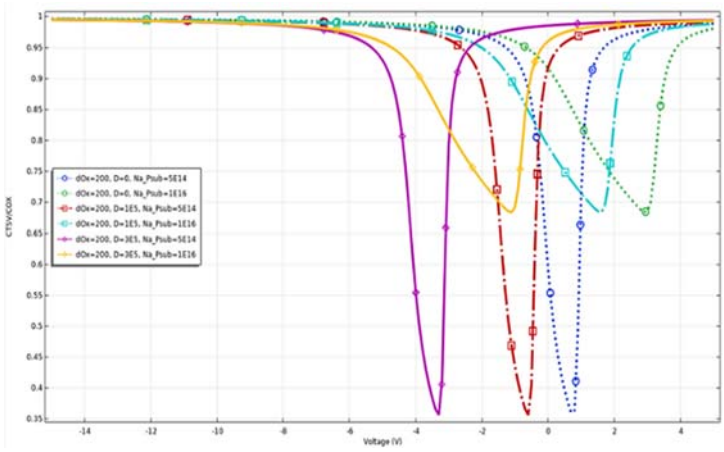
TSV is usually biased at the accumulation zone, to avoid the volatility of capacitance value when it is used in RF chip. After radiation, the TSV capacitance enters the inverse zone at lower voltage at low frequency. Also at high frequency, at the same voltage, the capacitance of TSV decrease with the increase of irradiation dose, and enters the depletion zone at lower voltage.

5. Experiment and Analysis

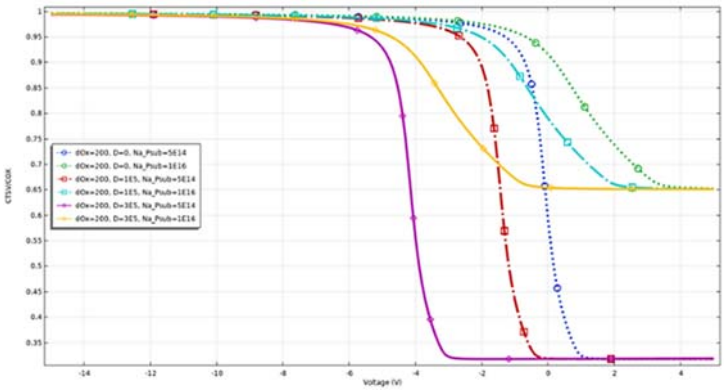
5.1. Design of Irradiation Experiment

In RF chips utilized 3-D integration technology, the arrangement of TSV position affects transmission

performance of TSV, furthermore affecting the performance of RF chips. Two adjacent TSVs which both transmit signals and two adjacent TSVs, one transmits signals, the other connects to GND, the performance of them and the performance change caused by the irradiation experiment might be different because of TSV positioning issue.



(a) Low frequency;



(b) High frequency

Fig. 3. C-V curve of TSV capacitance after irradiation.

To overcome the uncertainty brought into experiment by TSV positioning, three types of TSVs are designed, modeled in HFSS and manufactured. Figs. 4(a), (b) and (c) show three types of TSVs.

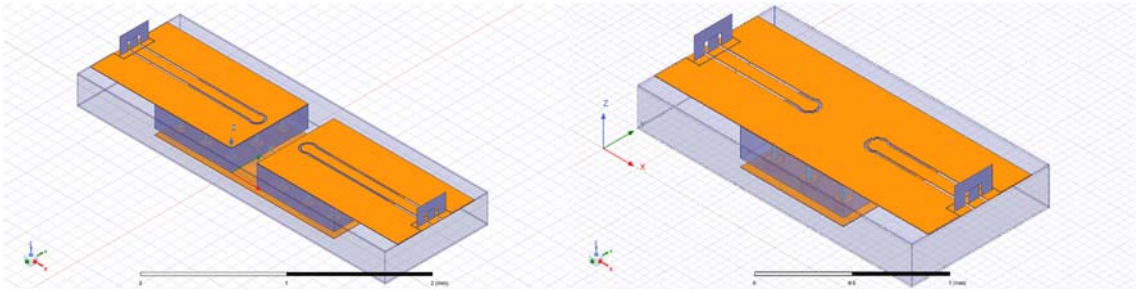
As shown in Fig. 4, there are two main differences between those three types, one is the number of redundant TSVs connected to GND, the other is whether the two copper layers connected to GND are combined together. For type A which owns twelve redundant TSVs, the copper layers connected to GND are separated. For type B which owns six redundant TSVs, the copper layers are combined. For type C which owns fourteen redundant TSVs, the copper layers are separated.

Nine pieces of TSV chip of each type are manufactured, to prevent the contingency of irradiation experiments on TSV chips. In the irradiation experiment, three levels of irradiation dose are set, which are 30 Krad, 90 Krad and 150 Krad. The settings of irradiation experiment are as shown in Table 1.

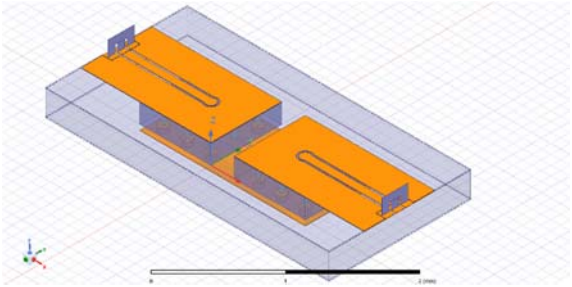
Table 1. Irradiation experiment conditions.

Irradiation dose	Experiment conditions	
	Irradiation rate(rad/s)	Irradiation time(min)
30 Krad	50	10
90 Krad	50	30
150 Krad	50	50

In the irradiation experiment, the effect of annealing affects testing results after irradiation strongly, considering the time between experiment and test, we put chips into the irradiation environment according to the order. For each type, first, three TSV chips to be irradiated in the dose of 150 Krad are exposed to irradiation, then three chips under 90 Krad after 20 minutes, at last, three chips under 30 Krad are exposed after 20 minutes, 10 minutes later, all chips are taken from the irradiation environment to test.



(a) Type A (b) Type B



(c) Type C

Fig. 4. The designed and manufactured three types of TSV.

5.2. The Results Tested Before and After Irradiation

The testing environment is as shown in Fig. 5.

S parameters reflects transmission coefficients, reflects the transition performance of TSV, can be measured on the above equipment. For two-port system, S_{21} and S_{12} represent the transmitting loss in channel, which means TSV in this research, the bigger S_{21} and S_{12} parameters are, the worse the transmission performance of TSV is, also S_{21} equals S_{12} because of the symmetrical structure of TSV chips shown in Fig. 4.

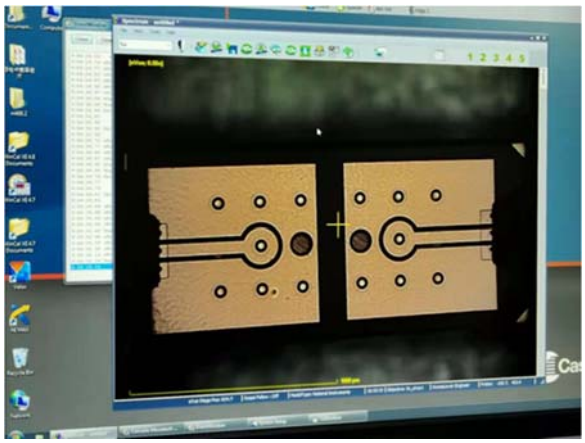


Fig. 5. The testing environment of TSVs.

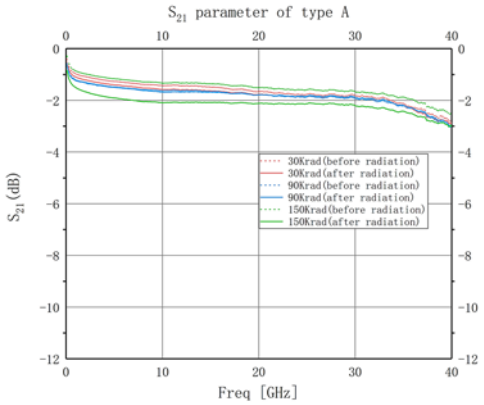
The S parameters measured are as shown in Fig. 6 (a), (b) and (c). The dot lines are S_{21} parameters measured before irradiation, and the solid lines are S_{21} parameters measured after irradiation.

5.3. Analysis Based on Experiment and Measured Data

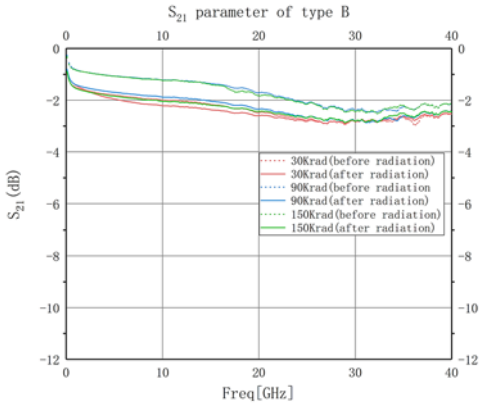
In the experiment, nine of each type of TSV chips for a total of 27 chips. In measurement after experiment under the same irradiation dose, some S_{21} parameters of same TSV chips are inconsistent. For example, at 10 GHz, S_{21} parameters of TSV chips (type A) under the irradiation dose of 30 Krad are measured after radiation, they degrade for 1.85 dB, 0.14 dB and 0.44 dB respectively, under the irradiation dose of 90 Krad, S_{21} parameters of TSV chips (type A) degrade for 0.86 dB, 0.06 dB and 0.41 dB respectively. Comparing S_{21} parameters measured, 1.85 dB and 0.06 dB is apparently wrong, the data need to be removed. The errors in measurement makes it hard to get accurate S parameters and furthermore calculate how much irradiation dose affects TSV capacitance, and analyses how much TID effect would affect RF system.

As the interpretation of Fig. 3, because of TID effect on TSV capacitance, the fixed charge accumulated in oxide layer would increase the capacity value at inverse region, which makes C-V curves drift to the left at both low and high frequency. In Fig. 6, red curves are S_{21} parameter tested after irradiation of 30 Krad, blue curves are results after irradiation of 90 Krad and green curves are results after irradiation of 150 Krad. As can be seen in Fig. 6, after irradiation, the S_{21} parameter deteriorates, according to the S_{21} parameter simulated based on the model built in HFSS, the S_{21} parameter curves behave the same trend after irradiation, both deteriorate badly. Though experimental error makes it harder to proceed with further quantitative analysis, the conclusion is definite: irradiation affects TSV capacitance strongly. S parameter of TSVs degrades because of irradiation,

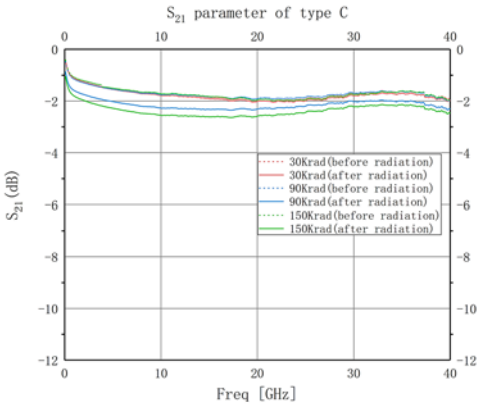
furthermore reflects the degradation of performance of TSV capacitance.



(a) Type A



(b) Type B



(c) Type C

Fig. 6. S parameters of 3 types of TSV chips before and after irradiation experiment.

6. Conclusion

In this paper, we found RF system utilized 3D integration technology would be widely used, while the TID effect on it has been neglected, which hinders the application in space and nuclear industry. To study the TID effect on RF system, a simulation methodology of TID effect on it is proposed, and three types of TSV is designed and manufactured, experiment based on them verifies the simulation methodology. In simulation based on the model in COMSOL, we found after irradiation, the C-V characteristic curve of TSV chips drift to the left, the bigger the irradiation dose is, the more c-v curve drifts. In order to ensure the stability of the whole system, it is necessary to set the working point of the TSV capacitor in the accumulation zone, and leave a certain margin for the left drift of the irradiated characteristic curve to ensure the stability of the TSV capacitor. And as the data measured after irradiation experiment based on the three types of TSV, though interfered by the experimental error, we could get the conclusion, the performance of TSV degrades, with the increasing of irradiation dose, the S_{21} parameters of TSV chips degrade more. The above research work lays the foundation for RF system with TSV to be used in irradiation environment.

Acknowledgements

This work was supported in part by the National Natural Science Foundation of China (NSFC) under Grant 62074121, and in part by the National High Technology Research and Development Program of China (no 2019YFB2204402).

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Electromigration-aware Instruction Execution for Modern Microprocessors

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Summary: Reliability is a fundamental requirement in microprocessors to guarantee correct execution over their lifetime. The reliability-related design rules depend on the process technology and operating conditions. To meet reliability requirements, advanced technologies impose challenging design rules on VLSI implementation flows. This paper focuses on electromigration (EM), which is one of the influential factors affecting semiconductor reliability. EM is the aging process of on-die wires and can severely damage nets in integrated circuits. Traditionally, EM issues have been handled by the physical-design flows that enforce reliability rules using worst-case scenario analysis to detect and solve violations. In this paper we offer architectural solutions that exploit architectural characteristics to reduce EM impact on modern microprocessors execution units. The use of architectural methods can simplify EM solutions and also be incorporated in conjunction with standard physical-design-based solutions. Our physical simulations show that, with minimal area, power, and performance overhead, the proposed solution can relax EM design efforts and significantly extend microprocessor lifetime.

Keywords: Electromigration, Reliability, RMS-Electromigration, Joule heating.

1. Introduction

Reliability is an essential design requirement and is crucial to assure the correct functionality of a semiconductor integrated circuit (IC). The requirement for reliability has been further heightened given the use of new computation-intensive applications such as autonomous vehicles, data centers and life-support systems. To meet reliability requirements, design-for-reliability flows have been developed by foundries and IC vendors [1-3] that, unfortunately, are highly complicated since they depend on the workload, the process technology, the operating conditions (voltage and temperature).

The shrinking dimensions of VLSI technology, the increasing density of logical elements, and the challenging voltage and temperature operating conditions combine today to make electromigration (EM) one of the most influential factors affecting the reliability of modern systems. EM is a phenomenon related to the aging of wires and vias in ICs. Three current models exist that are used to represent electromigration: (1) maximum [1], (2) average [2, 4] and (3) root-mean-square (RMS) currents [2]. These current models are further discussed in Section 2. In this work, we focus on the impact of the RMS current model (also known as RMS-EM). The RMS current model is based on Joule-heating [5, 6], which is induced by alternating current. This effect leads to thermal oscillations that generate metal deformation, in turn resulting in fatigue, voids and ratcheting metal failures. The RMS-EM is dependent on the signal toggle rate where higher toggle rate encourages a higher rate of thermal oscillation.

To date, the design community has focused on enhancing chip-design implementation flow [1, 2, 7-13] to solve EM issues, whereas few works have proposed architectural solutions. In this study, we propose a new architecture that significantly improves reliability by reducing RMS-EM impact while relaxing the physical design efforts and extending microprocessor execution units lifetime. This study is based on the observation that EM reliability concerns can occur due to an excessive utilization of computational elements and non-uniform signal toggling. This observation calls to develop an EM-aware resource-allocation scheme that uniformly distribute resource utilization and smoothen toggle rate. Such an approach can minimize RMS-EM hotspots induced by singular elements and extend the overall IC reliability. In addition, it can also help electronic-design-automation (EDA) tools which suffer from lack of information on the toggle rate and often assume a worst-case activity rate that may result in over design and shorter device lifetime. This study focuses on a microprocessor instruction execution as a case study; however, the concepts can be applied to other ICs and applications. The contribution of this paper is summarized as follows:

1. We offer architectural solutions that exploit architectural characteristics to reduce the impact of RMS-EM on microprocessors execution units;
2. The proposed methods exploit functional building blocks characteristics such as toggle rate, hot spots and resource allocation policies;
3. The architectural method can be incorporated in conjunction with physical-design-based

solutions where it offers a complementary enhancement to the current methods;
4. The proposed solution incurs minimal cost in terms of power, performance and silicon-area overhead;
5. Our new proposed approach requires no compromise on reliability or IC lifetime;
6. Our experimental analysis combines architectural and EM physical simulations, which both validate the proposed architectural solution.

The remainder of this paper is organized as follows: Section 2 introduces EM reliability challenges and reviews EM and previous works. Section 3 introduces the limitations of modern microprocessors to deal with EM, Section 4 describes the proposed EM-aware microarchitecture. Section 5 presents both micro-architectural and physical simulation results. Finally, Section 6 summarizes our conclusions.

2. IC Reliability

IC reliability has become a crucial discipline in VLSI chip design. The need for highly reliable systems has existed from the early days of computing and was mainly driven in the past by "special systems" such as mission-critical embedded systems. However, given the vulnerability of the new process technology and the appearance of new applications that require safe and reliable processing such as autonomous cars, large-scale computing-intensive systems, and life-support systems, reliability today is a fundamental requirement for most systems.

Over the past decade, as advanced process technologies have been introduced, the susceptibility to reliability-related issues has grown dramatically. Starting at 28 nm process technology and below, the design efforts dedicated to reliability have substantially increased. The design community has mainly tried to enhance the synthesis and place-and-route flows to handle reliability-related issues. Such flows involve substantial design efforts and, in many cases, required multiple iterations to make the IC comply with the design rules (also known as the "sign-off process"). We start by providing an overview of the EM phenomenon followed by a summary of previous related studies.

2.1. Electromigration

Electromigration (EM) is a physical phenomenon related to the reliability of wires and vias in ICs. EM causes shorts and voids in metal interconnects and decreased the median time to failure (MTF) of ICs. The occurrence of EM failure, even on a single wire, may result in overall chip failure. EM became a major concern in advanced process technologies when the geometrical dimension of wires and vias has shrunk to very small dimensions ([11]), making them highly susceptible to reliability issues. Black's equation [14] has been commonly used to model single interconnect segment median time to failure (MTF):

$$MTF = \frac{A}{J^n} e^{\frac{E_a}{K_B T}}, \quad (1)$$

where A is a constant, J is the current density, E_a is the activation energy, n is a scaling factor, K_B is the Boltzmann constant, and T is the absolute temperature. The MTF depends exponentially on temperature; in fact, higher temperature accelerates the negative effect of EM.

EM involves three electrical current models: (1) peak, (2) average and (3) root-mean-square (RMS) currents [2]. To meet the EM reliability requirements, special design-rule constraints are imposed by foundries on all the three current ([15]).

When peak current is applied, even for a short duration, it induces stress through the force of conduction electrons and metal ions. When the force of conduction electrons reaches a certain strength level, it may tear atoms from the boundary of the metal and transport them in the direction of the current flow. If such current force is maintained for a long time or if current flows frequently, the wire may become malformed. Such damage to a metal wire may result in reduced wire conductivity or in the formation of voids and hillocks (i.e., short circuits) [1], all of which lead to major reliability concerns. In the peak current model, which enforces limitations on every unidirectional current flow, the current density, J, can be expressed as [9, 15]:

$$J = \frac{CV_{DD}}{WH} pf, \quad (2)$$

where C is the wire capacitance, W and H are the metal width and height, respectively, V_{DD} is the operating voltage, f is the clock frequency, and p is the switching probability, also known as the toggle rate.

In the average current model, alternating current induces material backflow [2], which reduces overall material migration. This phenomenon, known as self-healing [4], is quite common in digital circuits that operate by charging and discharging metal interconnects. When the alternating current is symmetric, the impact of the average current on EM is relatively small. While EM in the peak and average current models is governed by the mobility of conduction electrons which accelerates the atomic diffusion (referred as current-induced EM), in the RMS current model [5, 6, 15], the alternating current produces thermal oscillations that deforms the metal and result in fatigue, voids, and ratcheting metal failures. This phenomenon, which is also known as the Joule-heating effect (or RMS-EM), cannot be compensated by self-healing [2]. In addition, thermal oscillations propagate to neighboring areas, with the result that nearby metals may also be degraded. RMS-EM signoff rules enforce maximum RMS current, $I_{RMS\text{-}max}$, for every net given a nominal median time to failure, $MTF_{Technology}$ (typically 10 years). Both

$MTF_{Technology}$ and $I_{RMS\text{-}max}$ are specified for every process technology by the foundries ([16]). The RMS current can be relaxed if the median time to failure is compromised as indicated by Equation (3) ([15]):

$$I_{RMS-reduced} = = I_{RMS-max}\sqrt{\frac{MTF_{Technology}}{MTF_{reduced}}} \quad (3)$$

The MTF in the RMS current model can be calculated by the following equation ([15]):

$$MTF = \left(\left(\frac{K_1}{K_2}\right)^2 \cdot \frac{1}{C^2 V_{DD}^2} \cdot \frac{1}{F_{max} \cdot p}\right)^{\frac{n}{2}} \quad (4)$$

where C represents the capacitance load, F_{max} is the maximum frequency, p is the switching probability, K_1 and K_2 are given by the following equations:

$$K_1 = A \cdot (W \cdot H)^n \cdot e^{\frac{E_a}{K_B T}}, \quad (5)$$

$$K_2 = \sqrt{\frac{1}{t_r} + \frac{1}{t_f}}, \quad (6)$$

where t_r is the rise time and t_f is the fall time. Our study is motivated by Equation (4) which indicates that MTF is inversely proportional to the switching activity ratio. Thereby, any relaxation on switching probability will result MTF extension. In Section 4 we propose a new architectural solution that exploits the relationship between RMS-EM and toggle rate in modern microprocessor execution units to reduce RMS-EM impact and extend MTF.

The process of handling EM in advanced process nodes relies on complex EDA tools that enforce EM-related design rules. For the maximum-current constraints, EDA tools typically assure that the driving cells will not exceed the maximum-current limitation and by employing other physical design means [15]. With respect to the RMS current, EM analysis tools simulate switching activity patterns extracted from functional simulations representing real applications. When the worst-case switching patterns cannot be determined, designers often use a statistical analysis. This may often lead to an over-design process and multiple fix iterations and trials. Some of the trials involve the use of wider metals and vias and, in several cases, may even limit the clock frequency, the switching rate, and the computational workload. The combination of all these limitations may result in degraded IC performance.

2.2. Prior Works on Electromigration

Prior studies consist of both physical design-based solutions architectural approaches that are summarized in the following subsections.

2.2.1. Prior Works Based on Physical Design

EM phenomena have been broadly studied from the physical design point of view. Various studies [7, 10, 17] examined different interconnects usage such as copper or aluminum under different process, voltage, and temperature conditions. From a physical point of view, the most common solution for EM is to widen the wires, however, it may increase the die area and introduce timing issues. A study by Dasgupta et al. [10] introduced a methodology for synthesizing the design and scheduling data transfer from the control data flow graph to the hardware buses in an EM-aware manner. Their algorithm requires that the activity be determined in advance, so it becomes tightly coupled to each specific computational use that it targets. A broad survey of additional physical-design-based techniques to mitigate EM impact is available in Ref. [13].

2.2.2. Prior Works Based Architectural Approach

Only a limited number of prior works have suggested architecture-based solutions to mitigate EM. Srinivasan et al. [9] suggested structural duplication and graceful performance degradation techniques. Structural duplication adds spare design structures to the IC and turns them on when the original structures fail. Graceful performance degradation, however, shuts down failing structures but keeps the IC functional while degrading its performance. This approach seems to incur a major hardware overhead related to the dedicated mechanisms to detect EM degradation through normal IC operation and the need for special circuits to switch on the redundant logic. In addition, it introduces extra power and performance overhead due to the addition of redundant hardware. A similar approach to handle EM by adding redundant elements has been introduced by [18].

Abella et al. suggested [11] a novel architectural approach for “refueling” bi-directional busses by monitoring the current-flow direction each time data is transferred on the bus and suggested a mechanism that triggers current compensation whenever an imbalance occurs between the current flowing in each direction. Such a scheme could relieve EM impact induced by peak current; however, it may encourage RMS-EM in the form of thermal oscillations. In addition, given their design complexity, modern VLSI circuits do not commonly use bidirectional buses. The refueling mechanism also disrupts bus operation and may introduce a dynamic power overhead due to the reversal current.

Srinivasan et al. [8, 19] suggested a dynamic reliability management approach where the processor dynamically maintains its lifetime reliability target by responding to the changing behavior of the application. This approach allows a processor with lower reliability to run correctly while compromising performance or operating conditions.

3. Distribution of RMS-EM Hotspots in Microprocessor Execution Units

Based on our previous discussion in Section 2, our main focus in this paper is on the switching probability, p. This factor is tightly coupled to micro-architectural assumptions and application workload while all other arguments are mainly related to physical operating conditions or to the process technology: The junction temperature indeed makes a major contribution to RMS-EM MTF; however, since it also depends on the workload and system cooling solution, common design flows usually consider the worst-case scenario of 105 or 125 °C in the sign-off process. As for metal width and height, the ALU execution units that we examine already utilize lower metal layers (typically metal 1-3), which are highly suspectable to RMS-EM. We also assume operating at nominal voltage and do not assume power saving modes, such as DVS (dynamic voltage scaling), which can save power and decrease RMS-EM impact while reducing performance. Finally, the capacitance parameter depends on process intrinsic capacitance and wire length.

Since RMS-EM design rules are limited by the weakest net, we start by examining the distribution of the switching probability over microprocessor execution units. It should be noted that the EM impact on metal wires that are part of the IC power grid is out of the scope of this paper. Subsection 3.1 describes our experimental environment, and Subsection 3.2 presents our observations on RMS-EM switching probability hotspots.

3.1. Experimental Environment

Our experiments use the sniper x86-64 simulator [20]. The simulation environment includes a detailed cycle-level x86 core model based on the Intel Gainestown core [21]. The clock frequency of the core runs at 2.66 GHz, the pipeline dispatch width of up to 4 instructions. The execution units consist of 3 ALUs, 1 FP add/sub unit, 1 FP mul/div unit, 1 branch unit, 1 load unit and 1 store unit. The Spec2017 benchmark suite, which has been used for the simulation process, contains applications from many domains such as: artificial intelligence, physics, compression and document processing. Every benchmark is run for 10 billion instructions.

3.2. RMS-EM Hotspots in Execution Units

We start our analysis by examining switching probability hotspots which may accelerate RMS-EM in ALU execution units. Fig. 1 shows the distribution of instruction execution among different ALUs when using the FIFO selection mechanism among all ready-to-execute instructions.

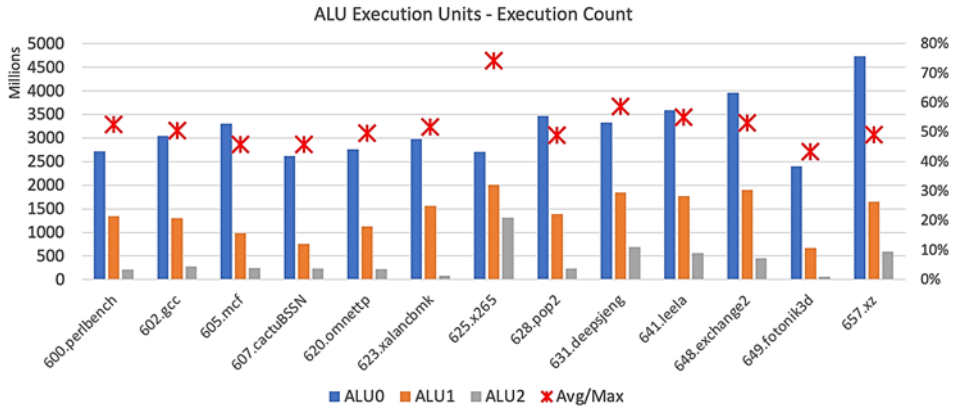

Fig. 1. Distribution of ALU execution count.

We observe that ALU0 is the most-used ALU of the three available, and ALU2 is the least used, which is attributed to the fixed allocation policy of the available ALUs, whereby a higher priority is given to an ALU with a lower index. Since ALU execution time is 1 clock cycle, all ALUs become available every cycle. For example, for a program that provides exactly one instruction per cycle, we expect only ALU0 to be used. Fig. 1 supports this claim and shows that ALU0 is used at over twice the rate than ALU1, and nearly ten times the rate than ALU2 for most benchmarks. In such a logical implementation, the worst-case switching factor of ALU0 dictates the worst-case RMS-EM scenario to be taken into account and applied to all ALUs. Such behavior leads to an over-design condition for RMS-EM that can degrade overall performance and increase IC area.

4. RMS-EM-Aware Instruction Execution Architecture

This section introduces our architecture solutions to eliminate switching probability hotspots and thereby

relax RMS-EM sign-off conditions. The idea is based on switching probability aware resource allocation scheme that smoothens the utilization of the available computational resources uniformly. Based on this principle, our RMS-EM-aware architecture can eliminate RMS-EM switching probability hotspots on ALU execution units.

We introduce two alternatives schemes that implement the same basic principle in different ways. The aim of both solutions is to start allocating the resources from a different leading point each time. The first simple solution is to have a counter (e.g., 32-bit counter) that is incremented each clock cycle and wraps around when expired so that the leading resource number to use is calculated as counter value modulo the number of physical resources. Thus, for our simulated environment, we assume N = 3. When the counter expires, we reset its content and continue with the allocation in the next cycle.

The second solution is illustrated in Algorithm 1; here, we assign each resource with a single bit counter (Ex_counter) and maintain a single bit global counter (Global_counter) for the overall management of the allocation. All counters are initialized to zero. The algorithm selects execution units whose corresponding counter state equals the global counter (denoted by the set M). If the number of available execution units that satisfy this condition exceeds the required number of instructions to be issued (k < |M|), then the needed subset, Q ⊂ M, of those execution units is selected, and all their corresponding counters are switched. Otherwise, the set M of all execution units with their counter state equal to the global counter are selected while the rest of the execution units are selected from the set of other pool of ALUs, Q ⊆ U\M (such that |Q| = k-|M|), whose counter is not equal to the global counter. In this case, only the global counter and the Ex_counters which are equal to the global counter are incremented.

Algorithm 1. EM-aware execution-unit allocation:

Input: k<N number of execution units to be allocated.

Output: Vector E = (e_0, e_1, …, e_{n-1}), for every 0≤ i ≤ n−1, only if e_i = 1 execution unit i to be allocated, otherwise not allocated.

Initialization: Ex_counter[i] = 0 for every 0≤ i ≤ n−1, Global_counter = 0

1. M = {0≤ i ≤ n−1 | Ex_counter[i] = Global_counter}
2. **if** k< |M| **then**
3. let Q⊂M such that |Q| = k
4. e_i = 1 for every i∈Q, otherwise e_i = 0
5. Ex_counter[i]++ for every i∈Q
6. **end if**
7. **else** // k≥ |M|
8. let Q ⊆ U\M such that |Q| = k-|M|
9. e_i = 1 for every i∈Q∪M, otherwise e_i = 0
10. Ex_counter[i]++ for every i∈ Q∪M
11. Global_counter++
12. **end else**
13. **return** E

Table 1 shows an example of the algorithm output for three ALUs.

The implementation of the first solution is straightforward and may perform well given a large number of execution units. The implementation of the second solution is little more complicated, but our implementation trial indicates that it can be done with negligible overhead. Table 2 summarizes power, timing, and area overhead for a 28 nm process. It should be noted that the proposed solution does not affect timing since the counters are updated in parallel to ALUs execution cycle.

Table 1. Example of EM-aware ALU scheduling.

Clock cycle	0	1	2	3
Number of instructions executed	0	2	2	3
Ex_counter [2:0]	000	011	110	001
Global counter	0	0	1	0
Selected ALU(s)	n/a	0,1	2,0	1,2,0

Table 2. ALU scheduling overhead.

Option	**Orig. Area [mm²]**	**Area Overhead [um²]/[%]**	**Orig. Power [uW]**	**Power Overhead [uW]/[%]**	**Timing impact**
1	0.200	316 / 0.15 %	641.79	0.031 / 0.004 %	None
2	0.200	85.9 / 0.04 %	641.79	0.026 /0.004 %	None

5. Experimental Analysis

In this section we present the experimental results for the proposed architecture solutions to reduce the impact of RMS-EM. The metric of MTF improvement is defined as the increase in the RMS EM-aware MTF with respect to the original MTF. By applying Equation (4) the following equation is obtained:

$$MTF\ improveme = \frac{MTF_{RMS\ EM-aware}}{MTF_{original}} - 1 = \\ = \frac{p_{max\ original}}{p_{max\ RMS\ EM-aware}} - 1, \quad (7)$$

where $p_{max\ \text{RMS EM-aware}}$ and $p_{max\ original}$ are the maximum toggle rates of a module with RMS EM-aware architecture and the original architecture respectively. Our microprocessor performance experimental analysis indicates that our proposed techniques did not experience performance overhead. Therefore, we focus our experimental analysis on examining the improvement of RMS-EM MTF. This is also validated via physical RMS-EM simulations that consider the Joule-heating effect through dynamic high-resolution thermal analyses.

5.1. Toggle Rate Based Experimental Analysis for RMS-EM MTF Improvement

We first examine an RMS EM-aware solution for ALU execution units. Fig. 2 shows how the solution describes in Algorithm 1 affects the RMS-EM MTF

for the SPEC2017 benchmarks. Examination of the two solutions introduced in previous section indicates that they behave very similarly. The results show that the proposed algorithm efficiently eliminates ALU usage hotspots and can potentially improve RMS-EM MTF by approximately 100 % on average. The results vary from nearly 34 % potential MTF improvement up to 130 % improvement. This result is because the proposed scheme distributes ALU use uniformly and reduces the RMS-EM hotspots.

In the last part of our experimental analysis, we present extensive physical simulations that consider both the toggle rate and the Joule-heating effect through a dynamic, high-resolution thermal analysis. The simulations were implemented in the Cadence® Voltus™ simulation environment [22], which performs detailed RMS EM analysis of the Joule-heating effect and self-heating under different toggle rates. The simulation environment takes into account the parameters of transistors that contribute to the RMS current, such as drive strength (fins, number of fingers), channel length, and channel width. The tool makes detailed RMS current calculations to analyze the Joule-heating effect and self-heating on all signal wires while taking into account metal dimensions and type and the toggle rate obtained from the functional simulations. As part of the simulation process, the tool also certifies that the calculated RMS current of every net does not exceed the maximum RMS current, which is considered a mandatory reliability criterion and is specified in the foundry technology file ([16]). We have run a full synthesis using Cadence® Genus™ and place-and-route flow using Cadence® Innovus™ on the examined ALU execution units which was used for the Voltus™ simulations. The implementation was done on 28 nm process node with core voltage of 0.9 V and junction temperature of 105 ºC. The clock frequency was 2.6 GHz.

Fig. 3 summarizes the reduction of the ratio of I_{RMS} to I_{RMS_MAX} in the design with the EM-aware architecture versus the original design for each benchmark that we use. In addition, it presents the percentage of metal nets that can leverage such RMS current reduction. Nearly all nets in the ALU execution units can leverage a reduction of approximately 30 % in RMS current. Note that the metal nets that do not leverage a reduction in the RMS current, already exhibited very small RMS current, so their overall improvement is not noticeable by the tool. The extended MTF as a result of I_{RMS} reduction can be calculated using Equation (3). The extended MTF is proportional to the ratio of I_{RMS_MAX} to the reduced I_{RMS} to the power of two. Thus, the observed RMS current reduction offers at least ×2 lifetime extension for the ALU execution units. One may note that these experimental results are similar to the MTF improvement prediction provided by the experimental results provided by figure (based on the switching probability reduction).

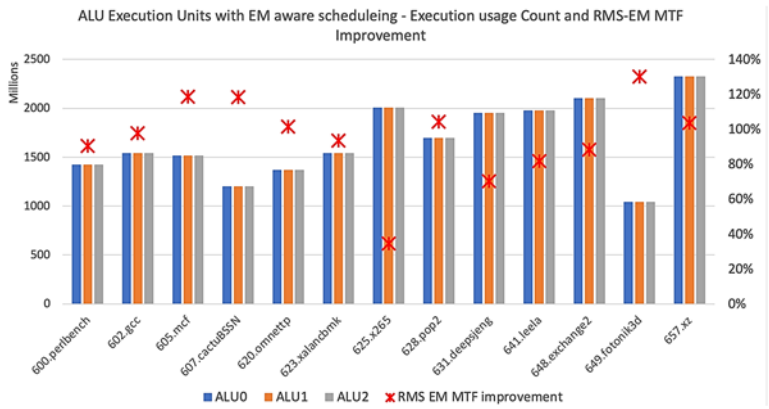

Fig. 2. Distribution of ALU execution usage count and MTF improvement with RMS EM-aware allocation.

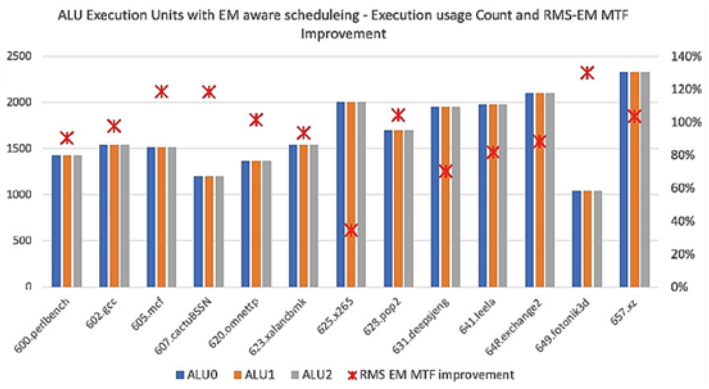

Fig. 3. IRMS/IRMS-Max ratio reduction of the EM-aware architecture with respect to the original design measurements.

6. Conclusions

This paper indicates that microprocessors can be highly susceptible to RMS-EM because they process highly variable dynamic workloads on non-EM-aware microarchitectures. We introduce herein architectural solutions that take into account the RMS-EM effect and reduce excess use of execution units. The principal of the proposed solutions is based on RMS EM-aware resource allocation that attempts to uniformly distribute the use of computational elements over all available resources. This solution can be incorporated into physical-design-based approaches where it offers a complementary enhancement to existing methods. Our analysis shows that the proposed solution incurs minor area and power overhead and negligible performance degradation with respect to prior studies. In addition, our experimental results indicate that the proposed architecture significantly relaxes the RMS-EM switching probability sign-off conditions by 50 % for ALUs. Our RMS EM physical simulations indicate that such toggle rate relaxation leads to a reduction in I_{RMS} of 30 % for ALUs. Such a reduction translates into lifetime extension of at least ×2 for ALUs.

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Design of a Novel Low Power Memory Controller: Challenges and Efficient Techniques for Reducing Active Energy in Non-volatile Memory

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Summary: A direct consequence of Moore's law is that the power density of integrated circuit increases exponentially with advent of every technology generation. Despite the concern on increased power density in high throughput, computationally intensive circuits, low power became mainstream requirement for circuits in memory domain. This paper discusses this concern and presents a usage of low leakage devices along with other techniques to lower active power demand in memory controller by presenting simulation data on component memory products. Along with data, different established design methodologies such as power gating of unused block, clock gating, reduction of frequency and operating voltages used to lower demand for active power have been described and their respective percentage contribution presented. For the first time the paper provides a quantitative percentage impact of each technique on lowering power of a memory controller. Also, the paper highlights the advantage of platform level memory power projection using statistical power data.

Keywords: Non-volatile memory component, Low power memory, Clock gating, Power gating.

1. Introduction

It has been well documented that 3D integrated circuits [ICs] provide more transistor density and better performance at smaller area as compared to traditional 2D ICs. Going vertical as in 3D design is more appealing to memory components compared to 2D design as it provides higher number of transistors resulting in increased memory size. Moore's law [1] states that the number of transistors that can be placed inexpensively on an integrated circuit will double approximately every two years. A direct consequence of Moore's law is that the power density of the integrated circuit increases exponentially with every technology generation. Despite this concern on increased power density, low power became a norm for memory circuits in most applications. Major driving factor behind this trend is the growing class of personal computing devices including all kinds of portable computational products and wireless communications systems, all using high density memories. These devices not only demand high-speed computations and complex functionalities, but also low power consumption. Another driving factor for low power logic circuit is that excessive power consumption is becoming the limiting factor in integrating more transistors on a single chip or on a multiple-chip module. Unless active power consumption from logic circuit is reduced significantly, the resulting heat will limit packaging feasibility and negatively impact performance of circuits and systems.

It has been observed that the most significant power savings can usually be achieved at high levels of abstraction, during early phases of micro-architecture and design process by conceptualization and implementation of low power architecture. However, an effective design flow should always be power conscious in its entirety and energy efficiency should be pursued at every level of the design, from conception of circuit generation down to physical design. As the level of abstraction lowers, the number of design elements grows, and design automation is required to manage complexity. Hence, power optimization at the logic level cannot rely on human ingenuity alone, it also critically depends on computer-aided design (CAD) tools.

The organization of the rest of the paper is follow. Section 2 presents a deeper insight into state-of-the-art techniques of lowering power dissipation in a component memory. In Section 3, techniques and challenges of low power memory have been presented and discussed. Section 4 describes different components of logic power. Section 5 presents generalized contribution of each component of the logic power at a component memory like NAND Flash for the first time. Section 6 lists and discusses techniques of lowering power dissipation. Section 7 presents proposed methods along with the known state-of-the-art techniques of lowering power dissipation along with savings achieved by using those techniques.

2. Literature Review: Techniques and Challenges to Reduce Active, Idle and Standby Power

Continued growth of processing speed in personal computing naturally demands significant power dissipation on the system-on-chip (S oC) especially on the memory element. Academia researchers and industry engineers have proposed and implemented

different techniques to reduce and mitigate excessive power dissipation inside memory elements. As we keep scaling down the transistors, power dissipation becomes priority on the design merit [2, 3]. Frequency scaling is one of the many options for lowering active power. Sometimes, parts of circuits don't need to operate at high frequency. Main performing path and frequency of those blocks can be reduced by addition of clock dividers and synchronizers. For example, some power up circuits within controller and loading up of register values don't need to be fast operation requiring significant performance. Also, introduction to manual and automated clock gating through backend tools are ways to further reduce active power significantly. Manual clock gating requires significant architectural knowledge and should be addressed during conception phase of the design. Additional to clock gating and lowering of operating frequency of slow performing blocks; introduction of low leakage library for lower performance paths additionally reduces standby and idle power of the controller. Even in fast performing blocks, not all devices within the block needs to operate in a single clock cycle. Low leakage library can be utilized for those devices through backend tools. In house 3D NAND-Flash experimental setup for a non-volatile memory controller, it was found that about 60 % of total transistors within the controller could be converted to low leakage library. Fig. 1 shows a percentage list of fast and low performance transistors in in-house 3D NAND-Flash memory controller. To save power a low leakage library can be achieved through different sets of transistors or by increasing device lengths. However, introduction of a new mask for new transistor development increases development cost along with process fabrication time whereas increasing channel length of devices might increase area of the device causing area penalty as well as active power due to increased loading capacitance for design.

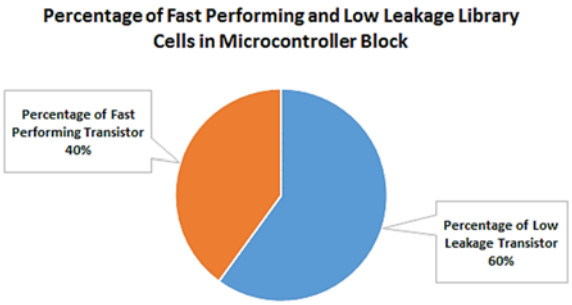


Fig. 2. Percentage of fast performance and low performance transistors in memory controller under discussion.

One other popular technique for standby, idle, and active power reduction is through targeted power gating of blocks based on usage of the blocks. This requires architectural attention from the concept phase of design along with introduction of isolation gates and power gates. Most of modern controllers use power gating architecture these days to meet stingy power criteria at component level.

Sometimes, changing transistor type enables usage of lower supply voltage delivered through regulated supply. Voltage has the most significant impact on active power reduction with active power being $P_{switch} = f\frac{(C_L V_{DD}^2)}{2}$ with C_L being the load capacitance, V_{DD} being the supply voltage and f being the operating frequency. Hence, two methods namely scaling of operating frequency and supply voltage were used for power reduction within the memory controller under discussion.

3. Literature Review: Techniques and Challenges for SRAM Power

SRAM used for storage of firmware in non-volatile memory is usually a big consumer of power like in most other computationally intensive applications. Hence, reduction of SRAM power attracted a lot of research efforts as transistors scaled down. To achieve this low power in SRAM, the memory architecture has been redesigned, altered, or even completely dropped. Listed are few recent works on low power memory covering from old techniques to more updated versions [2-7]. Nag et al. [3] presents a design change of SRAM cell to get lower power dissipation. This paper proposes an SRAM cell to facilitate a highly integrated variation tolerance memory with low power consumption for near-threshold operation. The authors utilized the concept behind power-gating PMOSs in a 22-nm FinFET-based SRAM cell solely for dynamic power saving during read and write operations [3]. In addition to this, the authors claim write disturbance of the cell can be eliminated by cutting off the power gating PMOS of the SRAM during write operation [3]. This potentially facilitates more reliable write operation without write-back scheme and write assist circuit. A detail description of power-gating usage has been presented in different SRAM cells such as 8T, 10T, DAW9T and PG9T SRAM cell [3].

Power-gate application for lowering a power in 3D IC is presented and discussed in [8]. Study of low power design and power saving work is also presented [9-15]. Similar work of ultra-low power application in memory component is presented in [16]. Adaptive voltage scaling and dynamic power gating working is covered in [17]. Reference [18-22], mainly focused on leakage current analysis. Reference [23-25] are focused on voltage-scaling and low-power applications on embedded and CUP and GPU. The authors of reference [4] considered using manual implementation of power gating technique for power reduction of as much as 50 % in 45-nm SRAM-based look-up table (LUT) [4]. The main objective of this work is to reduce power leakage of the SRAM. The concept behind this is to shut down the inactive block of the LUT during runtime. As part of the study, power and ground bounce noise in a conventional power gate have been discussed. Reference [4], presents

power-gated 9T SRAM cell for low-energy operation. With the increase usage of portable devices and excessive power dissipation in single/multi-chip integrated circuits, low power consumption becomes one of the most important design features of a system-on-chip, particularly low power consumption of a memory is critical as a significant portion of the system-on-chip is occupied by SRAM [4]. Keep scaling power supply as means to reduce power consumption have its own limit. Environmental and device mismatches become significant which have a direct impact on read and write stability of the SRAM. The proposed SRAM tried to save power by cutting off the path from the power sources to the storage nodes leaving bit-line as the only driver node of the storage cell [4]. By doing this, the SRAM manages to have better noise immunity while reducing the energy consumption. The work presented in [5] uses probability-driven multi-bit Flip-Flop along with a known power-reduction technique, clock gating. Other methods such as current profile generated by using gating logic to reduce power supply noise of integrated CPU chip have also been studied in [6].

4. Components of Logic Power

Total power in logic circuit is comprised of switching power, internal power, and leakage power. Switching power is the power that is consumed when signals through CMOS circuits change their logic states, resulting in charging and discharging of load capacitors. Only half of the energy drawn from the power supply is stored in the load capacitance; the rest is dissipated as heat [2]. This energy stored in the output capacitance is released during the discharging of the load capacitance. The load capacitance of CMOS logic gate C_L consists of the output node capacitance of the logic gate, effective capacitance of interconnects and the input node capacitance of the driven gate. Hence,

$$P_{switch} = t_R \frac{(C_L V_{DD}^2)}{2}, \quad (1)$$

where t_R is the toggle rate of the signal indicating number of transitions (0→1 or 1→0) per unit time. Toggle rate can be derived from number of toggles within a duration of measurement, i.e.

$$t_R = \frac{t_c}{measurement\ duration}, \quad (2)$$

where t_c is toggle count. For example, in Fig. 2, signal A has 4 toggles within measurement duration of 40 ps. The associated toggle rate is $t_R = \frac{4}{40}$ toggle/ps = 0.10 toggle/ps.

Internal power is comprised of short circuit power along with switching power internal to the circuit. Thus,

$$P_{internal} = P_{short\ circuit} + P_{intsw}, \quad (3)$$

where P_{intsw} is the switching power internal to the circuit where as $P_{short\ circuit}$ is short circuit power, which can be seen in Fig. 3. Because of finite non-zero rise and fall times of signals to the transistors, a direct current path between supply and ground is created causing short circuit power. This power component is usually not significant internal to logic blocks. However, it may appear as significant component for transistors used to drive large capacitances, such as bus wires. However, the number of such drivers is limited in logic controller. Usually switching power internal to the circuit is the major component of internal power within logic circuits.

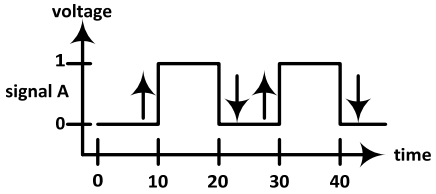


Fig. 3. Calculation of toggle rate.

Even though a transistor is in a stable logic state, it continues to leak small amounts of power at almost all junctions due to various effects like (a) reverse biased diode leakage, (b) gate induced drain leakage, (c) gate oxide tunneling, and (d) sub-threshold leakage. Majority of leakage current from logic circuit is due to sub-threshold leakage current. Leakage power in a logic circuit can be calculated using the following:

$$P_{leakage} = S_{p,A} * \text{leakage power}(A) + \\ +(1 - S_{p,A}) * \text{leakage power}(!A) \quad (4)$$

where $S_{p,A}$ = probability of node A in Fig. 4 being logic '1'. Similarly, from Fig. 4, $S_{p,CK}$ = is the probability of CK being logic '1'. Where CK stands for Clock, D for Data, and RB for Reset-bar (Active-low Reset). As can been seen from equation (4) leakage power is also a function of node A being logic '1' and logic '0' and their probability. For more complex gates like a flop whose symbol is shown in Fig. 4 below with reference to equation (5), leakage power is calculated using:

$$P_{leakage} = (1 - S_{p,CK}) * (1 - S_{p,D}) * \\ * (1 - S_{p,RB}) * leakage_{power} * \\ * (!CK\&!D\&!RB) + S_{p,CK} * (1 - S_{p,D}) * \\ * (1 - S_{p,RB}) * leakage_{power} * \\ * (CK\&!D\&!RB) + \ldots \quad (5)$$

Logic operators shown in Equation (5) are explained below: '!' operator stands for an inversion logic operation. In this case, !CK stands for 'NOT of CK', means an inversion of CK. Similarly, !D, !RB

stands for inversion of RB (NOT of Reset-Bar) and inversion of D (NOT of Data) respectively.

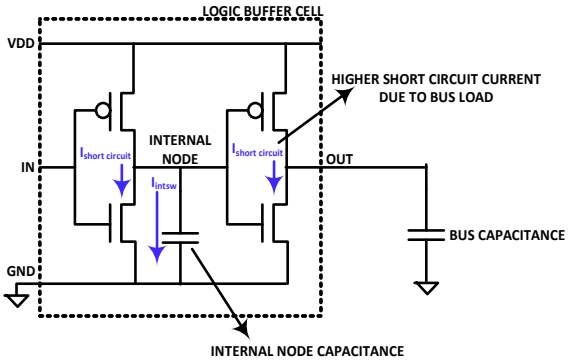


Fig. 4. Short-circuit component of power in a typical logic circuit.

Power consumed by logic circuits is quoted for the following three categories including (1) active power, (2) idle power and (3) power-mode power. Active power is the power consumed by logic circuit when it is in operation with clocks toggling. Usually, clock power is the most amount of power during active mode as clocks are routed to every flop within the design. In active mode, all three major components of power contribute to constitute total active power. Thus, active power is the sum of switching power, internal power as well as leakage power. Clock gating can be enabled to reduce active power in non-active part of logic circuit. Sometimes, power gating can be enabled for parts of logic circuits whose activity isn't required at all for execution of certain commands. Switching power and internal power together in equation (5) above are called dynamic power of the circuit. Leakage power is contributed by leakage from the logic gates along with clock power if not gated. Power mode power is all about leakage power. Fig. 5 shows percentage contribution of internal power components from a typical non-volatile memory controller in idle, write and read operation. As seen from Fig. 5, the switching power contribution goes up as the device gets more active, mainly due to clock activity along with toggling of interconnect signals between different blocks. Internal power component, already being the largest contributor to overall power, stays the largest contributor to overall power in all different power modes.

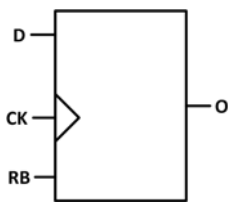
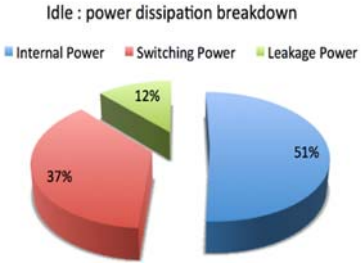


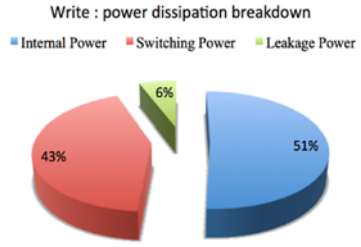
Fig. 5. Symbol of a FLOP whose leakage current calculation is shown in equation.

5. Techniques of Lowering Power Dissipation: Reviewing Simulation Data

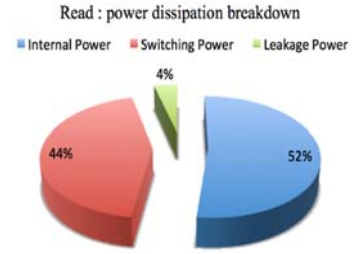
Clock gating is widely used procedure to reduce power dissipation during idle and active modes. Fig. 6 shows a percentage power reduction through clock gating in a non-volatile memory component. The figure summarizes that about 10 % and 14 % of power reduction can be achieved via clock gating for switching and internal powers respectively for the non-volatile controller under discussion.



(a) Typical power contribution in a memory controller at idle



(b) Typical power contribution in a memory controller during writing

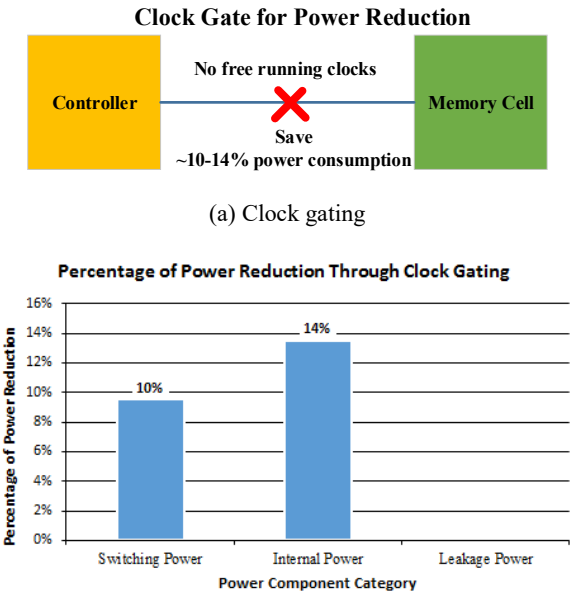


(c) Typical power contribution in a memory controller during read

Fig. 6. Typical power contribution in non-volatile memory controller at (a) idle (b) write and (c) read operation.

Other technique such as lowering power supply is also one of the practices among researchers and engineers when it comes to lowering active power dissipation in integrated circuit. Fig. 7 below shows a summary of percentage active power reduction by lowering the operating voltage. The result shows a typical case were reducing supply voltage by 52 % causing about 370 %, 370 % and 100 % reduction in switching, internal power, and leakage power respectively. However, the leakage power reduction is achieved by usage of a different kind of transistor due to the move from higher voltage to lower voltage

operation. This technique usually requires switching to different types of transistors for lower voltage operation. Similarly, Fig. 8 shows possible power reduction due to lower frequency and power supply. At block conversion number three, the power saving due to 50 % reduction in frequency and supply leads to ~25 % and ~40 % respectively. However, as the number of block conversion increase the power save are clearly higher than the percentage reduction of the frequency and supply. For example, at conversion rate of #4 and #5 the power saving due to frequency and supply are ~60 % & ~40 %, and ~78 % & ~45 % respectively.



(a) Clock gating

(b) Power reduction in bar-graph

Fig. 7. Typical power reduction in memory controller using clock gating.

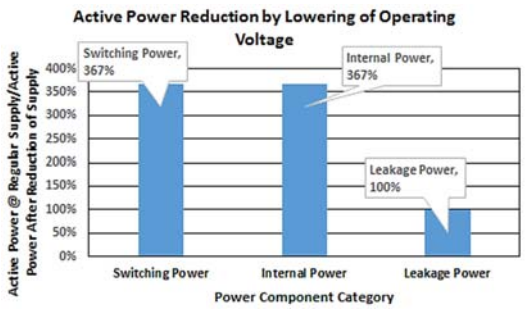


Fig. 8. Typical power reduction in memory controller by lowering operating voltage.

6. Proposed Techniques

The list of well-known techniques of lowering logic power dissipation ranges from lowering operating frequency, gate level implementation through manual clock gating, power gating of unused blocks all the way to reducing and regulating operating power supply have been implemented in non-volatile memory controller under discussion. Along with all these techniques we proposed to have separate libraries one targeting to meet the high-speed performance while the other targeting to reduce leakage power during idle and power-mode power phases. Fig. 9 below shows the impact of adding low voltage library on a NAND memory controller. The supply V_{cc} in Fig. 9 is the controller logic supply, while V_{ccq} is the supply of the data-path (blocks such as input receiver, output transmitter and FIFO (first-in-first-out)). To save active power within the chip, a low voltage library can be introduced using different sets of transistors. However, introduction of a new mask for new transistor development increases development cost along with process fabrication time. In this example, low voltage transistors used in data path circuits were utilized throughout the component memory to reduce power. Low voltage devices usually are leakier than regular transistors. To mitigate higher leakage from these low voltage devices, channel length of the device was increased in the library by active power versus area versus leakage power analyses increasing overall area of the device causing area penalty as well as a portion of active power due to increased loading capacitance for design. Figure shows that with a slight cost of area increase by 10 % with respect to regular library cell and 0.75x of leakage power increment, 40 % reduction of active power was possible.

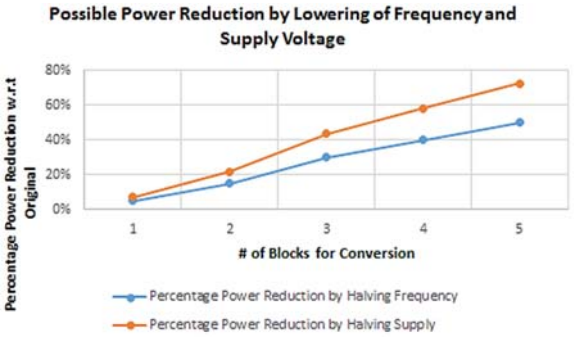


Fig. 9. Typical power reduction in memory controller by lowering frequency and supply voltage.

On top of this, computer aided design (CAD) tool capabilities were used to add other techniques including auto clock gating and implementation of power gating architecture. CAD tool support is widely required in this low-power abstraction throughout the design and implementation cycle of the memory controller. As number of design elements grow, the level of low power abstraction grows. Hence, design automation is required to manage this complex task in addition to addressing the problem through architectural and design flow. Thus, power optimization at the logic level cannot rely on human ingenuity alone, it critically depends on computer-aided design (CAD) tools.

7. Conclusion

The downside of the continuous transistor scaling is short channel effect, which result in drain-induced barrier lowering [flip drain], which leads to significant leakage current causing significant power dissipation in high performance semiconductor devices. Additionally, the constant need of speed results in higher active power if not addressed properly. Low power dissipation already became a priority among deep sub-micro high performance circuit designers. Usual practice is to come up with top-level low power abstract during design phase. However, design automation is an integral part of implementing the low power architecture at gate level. In summary, power optimization at the logic level critically depends on CAD tool capabilities along with designer and architect's ingenuity.

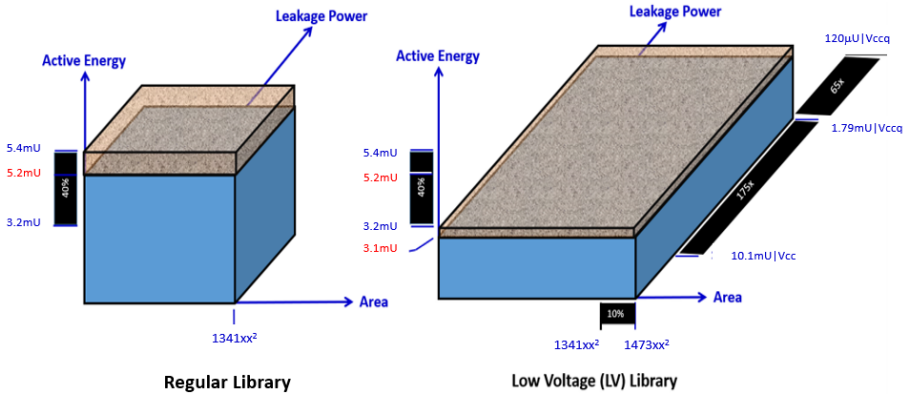


Fig. 10. Impact to area, active energy, and leakage power by utilizing low leakage library cells in NAND memory controller.

Acknowledgments

I would like to thank Bharat Pathak, Owen W. Jungroth and Ali Khakifirooz for supporting and encouraging the work.

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Study of Phonon-limited Electron Transport in Monolayer MoS_2

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Summary: A multi-valley Ensemble Monte Carlo simulator has been developed and applied to investigate the dependence of the energy separation ΔE_{QK} between the two conduction band minima (at the **K**- and **Q**-point of the Brillouin zone) on the phonon-limited electron transport in free-standing monolayer MoS_2. It has been shown that the mobility highly depends on this material property and can vary between 100 $cm^2/(Vs)$ and 300 $cm^2/(Vs)$ when ΔE_{QK} is varied within the values frequently encountered in literature. Even though the high-field drift velocity shows a lower dependence on the investigated property, a trend of decreasing high-field drift velocity with increasing ΔE_{QK} has been observed. Additionally, to obtain a better understanding of the wide span of different values for ΔE_{QK}, which can be found in the literature, multiple simulations of the band structure of monolayer MoS_2 using density functional theory were performed. It was observed that by including spin-orbit coupling, by varying the exchange correlation functional, and by applying different pseudopotentials the variations in the resulting ΔE_{QK} range from 104 meV to 266 meV.

Keywords: Monte Carlo, MoS_2, Mobility, Electron transport, High- and low-field transport, Density functional theory.

1. Introduction

Monolayer Molybdenum disulfide (ML-MoS_2) offers a theoretical direct bandgap of 1.8 eV [1], a high on/off current ratio (~10^8), and can withstand high elastic deformations. Due to these, and other beneficial properties of this two-dimensional (2D) material, it has gained traction in many fields including sensing, opto-electronics, and biochemistry [2].

For simulations of the intrinsic carrier transport of ML-MoS_2, characteristics of the band structure of the material have to be known. Due to advances in *ab-initio* calculations, especially in density functional theory (DFT), and gaps in experimental research, this property is mostly calculated with simulations from first principles [3].

The resulting band structures of different *ab-initio* simulations consistently show that the conduction band minimum is located at the **K**-point, while the second lowest conduction band minimum is at the **Q**-point (between the **K**- and **Γ**-points) of the first Brillouin zone, which is shown in Fig. 1 [4, 5]. However, for the resulting energy difference ΔE_{QK} between those minima, which is also sketched in Fig. 1, a spread from 60 meV to 300 meV can be found in literature [6]. This is a huge margin for a property, which can greatly influence the transport characteristics of electrons, as the onset energy of relevant scatter mechanisms depends on it.

The aim of this paper is to investigate the effect of the valley separation energy ΔE_{QK} on the phonon-limited electron transport. For this task, we have developed and applied a multi-valley Ensemble Monte Carlo simulator. Both low- and high-field characteristics are investigated by studying the dependence of the mobility, the drift velocity, and the valley population of ΔE_{QK}. Additionally, we used DFT to analyze how the investigated property is affected when various input parameters of those *ab-initio* simulations are varied.

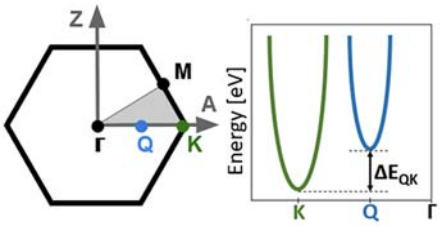

Fig. 1. Sketch of first Brillouin zone of ML-MoS_2, including the zigzag (Z) and the armchair (A) direction (left). Approximation of the conduction band with **K**- and **Q**-valleys (right).

2. Simulation Methodology

The simulations in this work are performed on free-standing ML-MoS_2, whose atomic structure can be seen in Fig. 2.

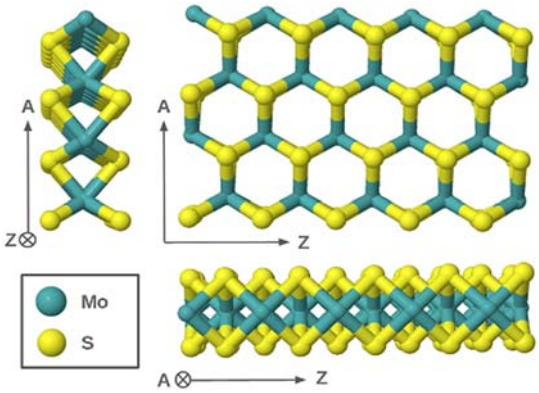

Fig. 2. Atomic structure of ML-MoS_2, including the zigzag (Z) and armchair (A) direction. Created using Jmol [7].

2.1. *Ab-initio* Calculations of the Band Structure

The simulations from first principles of the band structure of ML-MoS_2 are executed using DFT as implemented in the *QUANTUM ESPRESSO* (QE) package [8, 9]. The steps of all simulations include the relaxation of the system and the calculation of the band structure along the path **Γ**-**M**-**K**-**Γ**. Here, the symmetry point **Γ** is situated at the center, **M** at the edge midpoints and **K** at the edges of the hexagonal first Brillouin zone, which can be seen in Fig. 1.

The parameters, which are common to all performed simulations, are given in Table 1. Other specifications of the simulations, which are varied throughout different runs, like the application of spin-orbit coupling (SOC), the selected exchange-correlation functional V_{XC}, and the chosen pseudopotential will be stated for each presented result separately.

Overall, three different approximations are used for V_{XC}. The first one uses Linear Density Approximation (LDA), the other two approximate V_{XC} with the more general Generalized Gradient Approximation (GGA) based on the Perdew-Burke-Ernzerhof (PBE) functional, and the modified version of this functional for solids (PBESOL). Additionally, two different types of pseudopotentials are used: projector-augmented wave (PAW) and ultra-soft pseudopotentials (USPP).

All used pseudopotential files are taken from [11].

Table 1. Parameters used for all DFT-simulations.

Parameter	Value
k-points mesh	16×16×1
kinetic energy cutoff for wave functions	60 Ry
convergence threshold for self-consistency	10^{-12} Ry

2.2. Semi-classical Transport Simulations

An Ensemble Monte Carlo Approach is used to study the electron transport at room temperature. In the simulation a uniform electric field is applied along the Armchair-direction of the ML-MoS_2 film, which is shown in Fig. 1 and Fig. 2 in real- and k-space, respectively.

The conduction band of ML-MoS_2 is approximated using non-parabolic valleys around the band minima (**K**- and **Q**-valleys). In those valleys, the relation between the energy E and the wave-vector $\mathbf{k} = (k_l, k_t)$ of a particle is given by

$$E\,(1 + \alpha E) = \frac{\hbar^2 k_l^2}{2m_l} + \frac{\hbar^2 k_t^2}{2m_t}, \qquad (1)$$

where α is the non-parabolicity factor, while m_l and m_t are longitudinal and transverse effective masses, respectively. The applied values for the description of those valleys are given in Table 2 and are taken from [6]. It is noteworthy that the parameters for the valleys could have been extracted from our *ab-initio* calculations of the band structure (see Section 3.1), but we decided on using established values instead.

Table 2. Parameter for non-parabolic **K**- and **Q**-valleys [6].

Valley	m_l [m_0]	m_t [m_0]	α [eV^{-1}]
K	0.47	0.47	0.94
Q	1.14	0.54	1.16

To handle the ellipticity of the **Q**-valleys the Herring-Vogt transformation, which transforms the equienergetic surfaces to spheres, is used. This transformation of the wave-vector is performed with the density of states effective mass m_d and is given by [10]:

$$k_i' = k_i \sqrt{m_d / m_i}\ \forall i = l, t \qquad (2)$$

The scatter mechanisms, which are included in the simulations, are intrinsic acoustic and optical phonons, which are established as the primary conduction-limiting scatter-mechanisms in ML-MoS_2, as suggested in [5]. The calculation of the associated scatter rates, which apply effective deformation potentials, is performed as described in [5] and [6]. It is important to note that also the used deformation potentials and phonon dispersions are based on calculations from first principles, but since in this manuscript the effect of ΔE_{QK} is of interest, we again decided to use established values for those characteristics.

Furthermore, for the low-field characterization of the material, the mobility is calculated using two different approaches:

1. By calculating the slope of the drift velocity with changing electric fields at low fields, i.e., fields up to 2 kV/cm.
2. By calculating the diffusion coefficient at zero field via the velocity autocorrelation function. Afterwards, the Einstein relation is applied to derive the mobility from the calculated diffusion coefficient [10].

3. Simulation Results and Discussion

This section consists of two subsections: The first part describes the results of the band structure of ML-MoS_2 from *ab-initio* calculations with different input parameters and the resulting variations in ΔE_{QK}. In the second part the impact of changes in this valley separation energy on the intrinsic carrier transport is investigated.

3.1. *Ab-initio* Calculations of the Band Structure

In [3] various ‘flavors’ of the DFT, like the inclusion of SOC, the usage of different

exchange-correlation functionals and pseudopotentials, are identified as sources for discrepancies in the results of *ab-initio* calculations. Due to this observation, we also investigate the effect of all these 'flavors' of the DFT on the resulting band structure of ML-MoS_2, specifically on ΔE_{QK}.

First, different exchange-correlation functionals, which are described in Section 2.1., are applied in the simulations. The comparison of the resulting band structures and values for ΔE_{QK} are shown in Fig. 3. The minimal value for the valley separation energy, which is obtained using the PBE functional, is 122 meV and the maximal one is 262 meV, which occurs when LDA is used as an approximation for V_{XC}. Furthermore, Fig. 3 shows that the choice of the exchange-correlation functional also has an influence on the band gap and the effective masses of the valleys. The variations in those properties are not examined further in this paper, since our primary purpose is to observe the effect of changes in ΔE_{QK} and we apply established values for other characteristics.

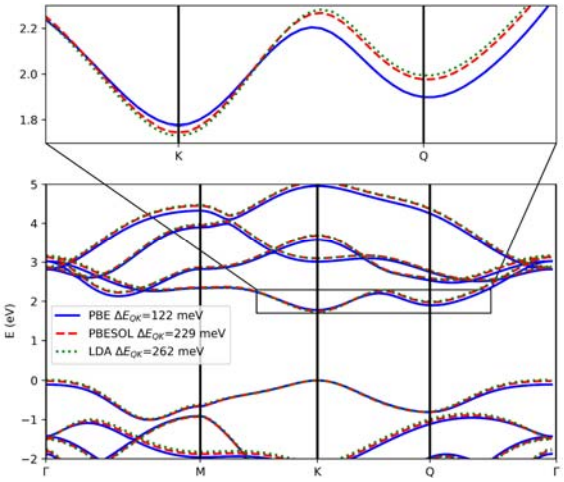

Fig. 3. Band structure of ML-MoS_2 using different approximations for V_{XC} (with USPP and without SOC).

Next, the impact of different pseudopotentials, which are also mentioned in Section 2.1, is tested and the results are shown in Fig. 4. One can see that the band structure and the resulting valley separation energy changes only slightly when the applied pseudopotential is changed.

Finally, the effect of the inclusion of SOC is investigated and the results are shown in Fig. 5. When SOC is included, band splitting can be observed, which has an influence on the band gap, the effective masses, and on the valley energy separation. Due to this splitting near the **Q**-point, the value of ΔE_{QK} reduces from 122 meV to 104 meV.

By only varying the three mentioned input parameters of simulations using DFT, the span of the resulting valley separation energy is 104 meV to 266 meV. This range is consistent with the one observed in literature, which is 60 meV to 300 meV [6]. The reason for the even bigger spread in the literature could be variations of other input parameters of the *ab-initio* calculations or the usage of different exchange-correlation functionals or pseudopotentials.

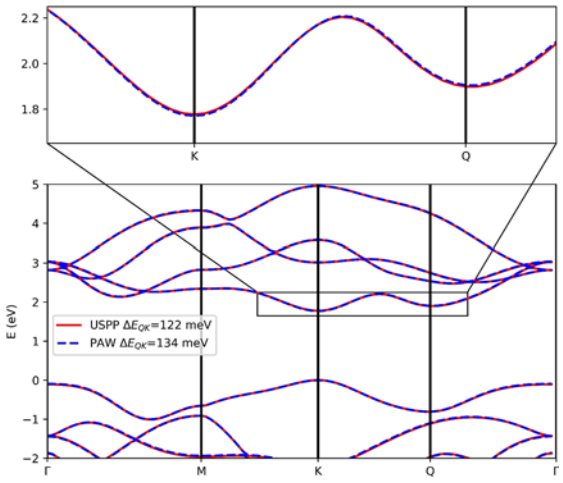

Fig. 4. Band structure of ML-MoS_2 using different pseudopotentials (with PBE and without SOC).

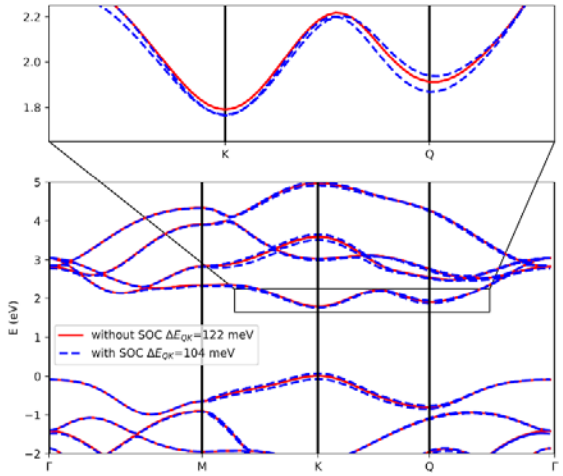

Fig. 5. Band structure ML-MoS_2 with and without SOC (using PBE and USPP).

3.2. Semi-classical Transport Simulations

Since the impact of variations in the input parameters of simulations using DFT on ΔE_{QK} has been explored, the effects of those variations on the electron transport characteristics are investigated in this section. Therefore, we vary the valley separation energy in our simulations within the range of the values observed in literature and discuss the effects of that variation.

To achieve a better understanding of the influence of the variation in ΔE_{QK} on the mobility, the mean **K**-valley population with different electric fields and varying ΔE_{QK} is shown in Fig. 6. With increasing energy separation of the valleys, the population of the **K**-valley also increases. This is expected as with growing ΔE_{QK} the energy onset of intervalley

scattering from the **K**- to the **Q**-valleys increases. This effectively means that the electrons need to be accelerated more to be able to scatter into higher valleys. In addition to the findings of this work Fig. 6 provides the results from [6], which assume a ΔE_{QK} of 160 meV and are in excellent agreement with our results.

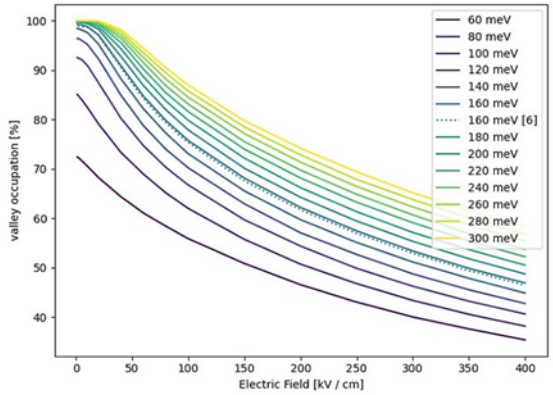

Fig. 6. K-valley occupation vs. electric field for varying ΔE_{QK} and comparison to the findings of [6] (dotted line).

Subsequently, the mobility due to varying ΔE_{QK} is provided in Fig. 7 and one can see that the resulting values vary between 100 $cm^2/(Vs)$ and 300 $cm^2/(Vs)$. At low valley separation energies, the mobility grows with increasing ΔE_{QK}. The reason for this increase is that with increasing valley separation energy, the onset energy for the scattering into the higher valleys also grows. Hence, a reduction of the importance and consequently of the limitation on the mobility of those scatter mechanisms at low fields is obtained. However, once ΔE_{QK} is sufficiently large, electrons at low-fields are not able to reach the onset energy for scattering into the **Q**-valleys. This leads to a mobility which is independent of the investigated property ΔE_{QK} as it then is only limited by the intra- and inter- valley scattering in the **K**-valleys. This behavior can be observed in Fig. 7 for cases when ΔE_{QK} is greater than 160 meV.

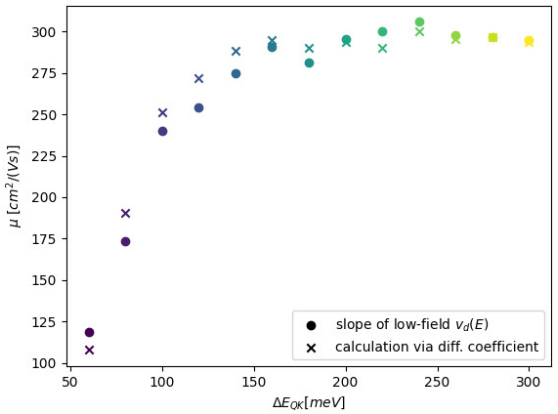

Fig. 7. Impact of varying ΔE_{QK} on the mobility.

For higher applied electric fields, Fig. 8 shows that the drift-velocity slightly decreases with increasing ΔE_{QK}. Moreover, for higher values of the valley separation energy the Gunn Effect [12], including the typical negative differential mobility, can be observed. This effect occurs in multi-valley semiconductors with lower and higher energy valleys, where the later ones also have higher effective masses [13], as is the case for ML-MoS_2. This effect is not observable for simulations with lower values of ΔE_{QK} since, in those cases, a significant percentage of the electrons already populate the **Q**-valleys at zero-field, as can be seen in Fig. 6. In addition to the findings of this work Fig. 8 also includes the results of [5] and [6], which assume ΔE_{QK} to be 70 meV and 160 meV, respectively, showing excellent agreement with our results.

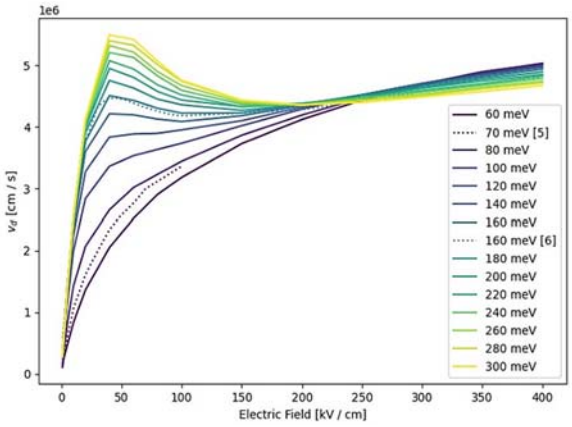

Fig. 8. Drift velocity vs. electric field with different ΔE_{QK} and comparison to findings of [5] and [6] (dotted lines).

4. Conclusions

Simulations using density functional theory were performed to observe and analyze the effect of the inclusion of spin-orbit coupling and of different pseudopotentials and exchange-correlation functionals on the resulting band structure of ML-MoS_2. It was observed that changes in those input parameters can lead to variations in the energy difference between the two conduction band minima of ML-MoS_2 in the range between 104 meV and 266 meV, which are consistent with the variations of the values that can be found in literature.

As the resulting band structure from *ab-initio* calculations is frequently used as a basis for intrinsic carrier transport, the impact of those changes in the valley separation energy on the phonon-limited electron transport was investigated. Therefore, we developed and applied a multi-valley Ensemble Monte Carlo Simulator. With this simulator it was shown that the mobility can vary between 100 $cm^2/(Vs)$ and 300 $cm^2/(Vs)$ with changing ΔE_{QK}. The observed effect of this property on the high-field drift velocities was smaller, but a decrease in the drift velocity was nevertheless observed with an increase in ΔE_{QK}.

Additionally, it was shown that with higher valley separation energies, the Gunn Effect can be observed.

Our investigation shows that the impact of the **Q**-valleys should be looked at in more detail and, even though this material is investigated heavily, still further investigations are necessary to obtain a physically realistic picture for the description of this material.

Acknowledgements

This work was supported in part by the Austrian Research Promotion Agency FFG (Bridge Young Scientists) under Project 878662 ”Process-Aware Structure Emulation for Device-Technology Co-Optimization”.

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(039)

Dielectric and Thermal Properties of $Zn_4B_6O_{13}$-Zn_2SiO_4 Substrates for Microwave and Terahertz Electronics

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Summary: In this study, new $Zn_4B_6O_{13}$-Zn_2SiO_4 substrates for microwave and terahertz applications were prepared by solid state synthesis and LTCC (low temperature cofired ceramics) procedure. Green tapes and test multilayer LTCC structures were obtained in the process comprising slurry preparation, tape casting, cutting, vias formation, screen printing, stacking, isostatic lamination and co-firing. The characterization of the fabricated ceramics encompassed the microstructure, elemental and phase composition, behavior during heating (20-1010 °C), specific heat and thermal conductivity (50-500 °C), and dielectric properties in the 90-140 GHz and in the 0.2-3.4 THz ranges. Scanning electron microscopy, energy dispersive spectroscopy, X-ray diffractometry, hot-stage microscopy, differential scanning calorimetry, laser flash analysis and time domain spectroscopy were used as the characterization methods. The substrates exhibited low sintering temperature, dense microstructure, compatibility with Ag-Pd conductors, low dielectric permittivity (6.2-6.4), low loss tangent (0.004-0.007) and thermal conductivity of about 6 W/mK, higher than that of conventional LTCC materials.

Keywords: Zinc borate, Zinc silicate, LTCC, Substrate, Thermal conductivity, Dielectric properties, Terahertz applications.

1. Introduction

Electrical, thermal and mechanical properties of the substrate material are pivotal for proper functioning of the electronic device. Low production cost, high integration and miniaturization scale, high reliability, high electrical resistivity and mechanical strength are the well-known benefits of substrates and packages manufactured using LTCC (low temperature cofired ceramics) technology. The important application area of LTCC are mobile and satellite communication systems, wireless networks, positioning and radar systems. For these applications, the crucial parameters of the substrate are low dielectric permittivity, high quality factor and low temperature coefficient of resonant frequency [1]. Low thermal conductivity is the greatest disadvantage of conventional LTCC substrates; thus, improvement of this property is a very important challenge. Among good candidates which can meet the requirements for the substrates suitable for high frequency microelectronic circuits are zinc silicate [2-6] and zinc borates [7-11]. This study is focused on fabrication of the $Zn_4B_6O_{13}$-Zn_2SiO_4 composite and characterization of its thermal properties and dielectric properties at microwave and terahertz frequencies.

2. Materials and Characterization Methods

$Zn_4B_6O_{13}$ and Zn_2SiO_4 were chosen due to their low dielectric permittivity, low thermal expansion and relatively high thermal conductivity. A low melting point of $Zn_4B_6O_{13}$ caused a desired decrease of the sintering temperature to the level of 930-950 °C required for cofiring with cheap Ag and AgPd thick film pastes.

$Zn_4B_6O_{13}$ and Zn_2SiO_4 were synthesized by solid state reaction at 900 and 1150 °C, respectively. The composition containing 60 wt.% $Zn_4B_6O_{13}$ and 40 wt.% Zn_2SiO_4 was prepared by ball milling (Pulverisette 5, Fritsch, Germany). The obtained fine powder was used for fabrication of pellets and slurries for tape casting.

Slurries for tape casting were prepared by ball milling of the ceramic powder with organic additives – fish oil as a dispersant, isopropyl alcohol-toluene mixture as a solvent, polyvinyl butyral as a binder and polyethylene glycol-dibutyl phthalate mixture as a plasticizer. Green tapes 80-100 μm thick were obtained by casting (TTC-1200, Mistler, US) and subsequent drying at room temperature and at 50 °C. Test multilayer substrates were fabricated in the LTCC process comprising cutting of green sheets and vias formation by laser treatment (E-355-3-G-OA Oxford Lasers, UK), screen printing of vias, internal and top conductors (Microtec MT-320TVC, Japan), stacking, isostatic lamination (IL-4008PC, Pacific Trinetics Corporation, US) and co-firing.

The microstructure of the ceramics and compatibility with commercial thick film conductors were analyzed by scanning electron microscopy and energy dispersive spectroscopy (Nova Nano SEM 200, FEI, US). The phase composition was examined by

X-ray diffraction method (Empyrean, PANalytical, Netherlands).

The behavior during heating from 20 to 1010 °C was studied using a hot stage microscope (Leitz, Germany). Specific heat c_p and thermal diffusivity a were studied in the temperature range 50-500 °C using differential scanning calorimetry and laser flash analysis (STA 449 F5 Jupiter and LFA 427, Netzsch, Germany). Thermal conductivity λ was calculated as $\lambda = a \cdot c_p \cdot \rho$, where ρ – density.

Dielectric properties were investigated in the 90-140 GHz band by the transmission method and in the 0.2-3.4 THz range by time domain spectroscopy (TPS Spectra 3000, Teraview, UK).

3. Results and Discussion

The XRD analysis revealed two crystalline phases – $Zn_4B_6O_{13}$ and Zn_2SiO_4 which confirmed the formation of a composite without any additional reaction products (Fig. 1).

SEM image (Fig. 2) illustrates dense microstructure of the ceramic layers and their good cooperation with AgPd thick films in the multilayer LTCC structure.

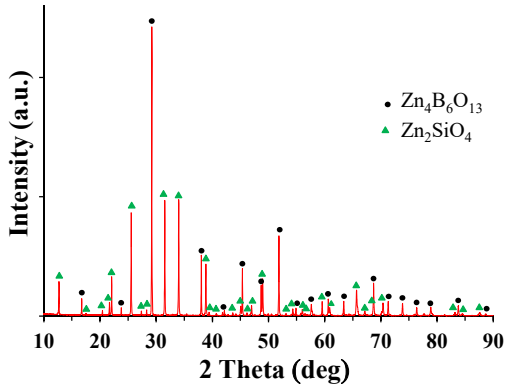

Fig. 1. Diffraction pattern of $Zn_4B_6O_{13}$-Zn_2SiO_4 powder.

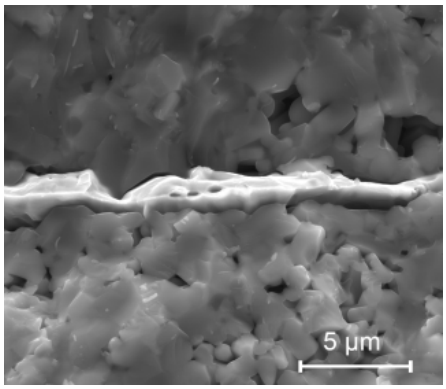

Fig. 2. SEM image of LTCC $Zn_4B_6O_{13}$-Zn_2SiO_4 structure.

The observation in a hot stage microscope of a sample during heating in the temperature range 20-1012 °C showed that the optimal sintering temperature of the composite is 930-950 °C. Its melting point is 1012 °C.

Figs. 3a and 3b show the temperature dependence of the specific heat and thermal conductivity of the fabricated ceramics. The thermal conductivity of the ceramics was found to be 6 W/mK at 50 °C which exceeds typical values for LTCC materials (2-3 W/mK).

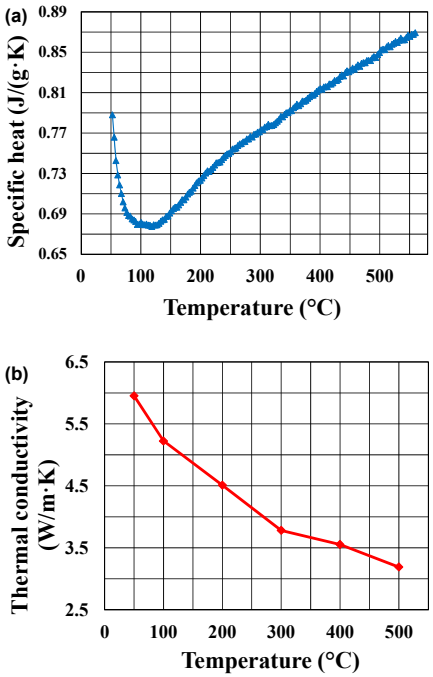

Fig. 3. Specific heat (a) and thermal conductivity (b) versus temperature for $Zn_4B_6O_{13}$-Zn_2SiO_4 ceramics.

Fig. 4 shows the dielectric properties of the substrates versus frequency in the 0.2-3.4 THz range. The dielectric permittivity is low (6.2-6.4) and increases slightly up to 1.5 THz. The loss tangent in this range is relatively low (0.004-0.007). At frequencies exceeding 2 THz, a more rapid increase and some local maxima are observed in both plots. These maxima can be attributed to phonon absorption modes.

In the 90-140 GHz range, the dielectric permittivity (6.3) and loss tangent (≤0.007) are similar to the values at THz frequencies.

4. Conclusions

The substrates based on $Zn_4B_6O_{13}$-Zn_2SiO_4 composites were prepared by solid state synthesis, tape casting, screen printing, isostatic lamination and co-firing. The composites are promising candidates for LTCC substrates of microwave and terahertz circuits due to their low sintering temperature, low and temperature stable dielectric permittivity, low loss tangent and enhanced thermal conductivity.

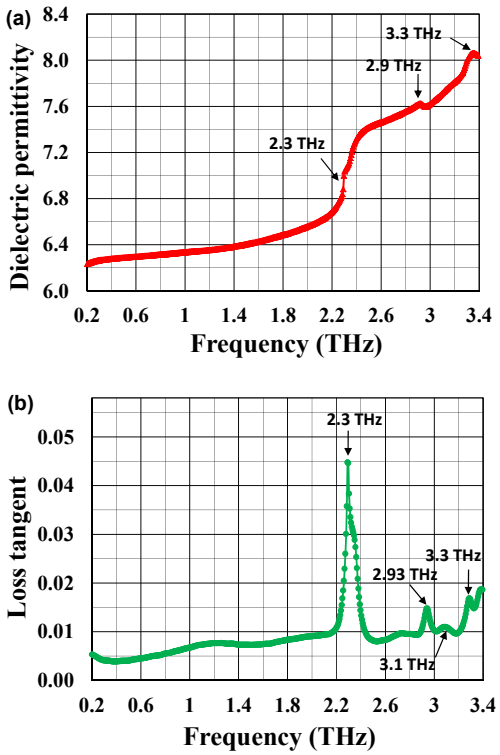

Fig. 4. Dielectric permittivity (a) and loss tangent (b) versus frequency for $Zn_4B_6O_{13}$-Zn_2SiO_4 ceramics.

Acknowledgements

The work was financed by National Science Centre, Poland, grant number 2019/35/B/ST5/02674.

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Implementation Tool Qualification Methodology for ASIC Design

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Summary: Implementation tool qualification is one of the important aspects of ASIC design execution. Often, it is done through tool flow downloading from the vendor and performs basic death on arrival check. Such deployment raises the doubt of possible unquantifiable risk escapes. Hence, for multinational design house, more than death on arrival flow qualification is performed, instead of relying on the reference methodology flow from EDA vendor. This paper will focus on the proposed stability check for tool qualification. Hopefully, the result from the proposed tool stability check will provide additional insight and benefit to the design community.

Keywords: EDA tool, Qualification, Stability check.

1. Introduction

In ASIC development, EDA tool is used to ease the designers to accomplish the development goal. As electronic components now account for 40 % of the cost of car, ISO 26262 is used as standard for automotive functional safety standard. Within ISO 26262, it highlights the need to increase confidence of use for all tools in SOC development cycle as shown in Fig. 1.

iso 26262-8 Tables 4 and 5		TCL1	TCL2				TCL3			
Methods	ISO 26262-8 Reference		ASIL				ASIL			
			A	B	C	D	A	B	C	D
1a Increased confidence for use	11.4.7	Needs no qualification methods	++	++	++	+	++	++	+	+
1b Evaluation of the tool development process	11.4.8		++	++	++	+	++	++	+	+
1c Validation of the software tool	11l4.9		+	+	+	++	+	+	+=	++
1d Development in accordance with a safety standard	*		+	+	+	++	+	+	+=	++

++ Indicates that the method is highly recommended for the identified ASIL
+ Indicates that the method is recommended for the identified ASIL

NOTE: * No safety standard is fully applicable to the development of software tools.
Instead, a relevant subset of requirements of the safety standard can be selected.
Example: Development of the software tool in accordance with ISO 26262, IEC 61508 or RTCA DO-178

Fig. 1. ISO 26262 EDA Tools Requirement [9].

For the current research of EDA tool, it is summarized as in Table 1 below.

Table 1. EDA Tool Research Topic [1-16].

EDA Developments	Years
Machine learning feature	2021,2018,2017
Tool flow validation methodology	2021
New tool initiative	2021,2020
EDA tool safety standard	2021,2017,2015
Bug , validation, qualification	2021,2011,2009,2002,2000

To understand the quality of the EDA tool release, users may refer to the release notes to understand the type of bugs fixes. However, the bugs fixed in the EDA tool release only imply two aspects:

- Speed of the vendor's bug fixes;
- History of the bugs exist in older version.

The rate of bugs fix is never a quality assurance indicator for the current tool release. Users can only hope that EDA vendor has done sufficient qualification prior release to customers. For the rate of tool bug fixes by year and release cadence, it is shown in Fig. 2. Typically, the current year release will inherit most of the bug from the previous release version. Higher bug fixes on a particular tool version, may be an indicator of the user adoption, on a particular tool version as well.

For ISO 26262 related issues, it is currently adopted by the EDA vendors, as part of the release. The status is still no known issue but does not imply zero risk. Users are encouraged to regularly check online. The ISO 26262 release of snippet from EDA is shown in Fig. 3.

For most design houses where focus is on speed of development with limited resources, they may opt to reference methodology download from EDA tool vendor as well as flow recommendation from foundry for particular node. For the type of checks in implementation tool qualification, it typically covers the following scenarios:

- Death on arrival check;
- Limited basic quality check.

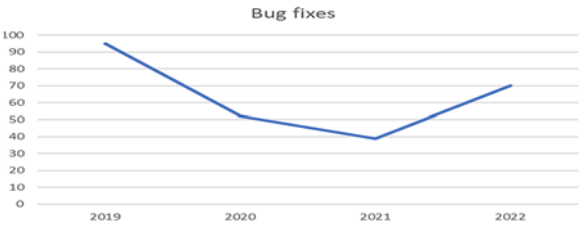

Fig. 2. Tool Bug Fixes Rate by Release Year, per Release Cadence [16].

Fig. 3. ISO 26262 Release by EDA Vendor [16].

This paper focus on internal qualification on the EDA tool prior to production deployment, as well as the additional proposed stability methodology in the tool qualification. For stability methodology by the EDA vendor, also known as repeatability or noise quality, where it focuses on repeatability of the result with design input collateral remains unchanged. The EDA vendor noise regression [14] focus on the following effects:

- Random initial ordering;
- Random seeds;
- Random naming.

The proposed stability check covers the existing gap with design input collateral adjustment less than 1 %, to capture the swing in quality of result.

2. Existing Qualification

The common method of EDA tool deployment is referring to the foundry reference flow for particular technology as well as tool certification from foundry. Example of the reference flow is shown in Fig. 4.

User just need to download the reference script from the EDA tool vendor, then configured the required variables, before kicks off the project deployment. Example of flow deployment is shown in Fig. 5 below.

For most designers, in-house tool deployment qualification only focuses on the signoff tool related. For example, in timing sign-off, correlation is done against the spice simulation for 1000 critical paths as well as timing quality validation against older tool version release, for any outliers' review. Similarly, for physical verification sign-off, it will validate of the physical design rule check (DRC) against existing tape out DRC report. The typical EDA qualification method can be summarized as in Fig. 6 and Fig. 7.

From Fig. 6 and Fig. 7, existing check deploys in the field, mainly focus on the outlier review with the existing tape out tool version as golden, as well as accuracy check with golden sign-off tool such as Hspice and Field solver for RC parasitic extraction.

For this paper, we will share the additional stability check for implementation tools deployment, to fill in the gap in implementation tool qualification.

3. Implementation Tool Qualification

For implementation tool qualification, it covers the following pillars in sequence:

- Function check;
- Integration death on arrival check;
- Basic quality matrix check;
- Tool stability quality.

The implementation tool qualification pillar is illustrated in Fig. 8. For functional check and integration check, it focuses on the implementation features for project deployment and overall script integration as one reference flow for deployment. It is similar to reference methodology (RM) flow trial run before project deployment. Hence, functional check and integration check are considered as basic flow deployment and will not be discussed further.

For basic quality matrix check, the standardized reference designs are used to evaluate the flow from performance, power, area (PPA) and turnaround time (TAT). For timing quality check, it involved worst negative slack (WNS), worst hold slack (WHS), total negative slack (TNS), total hold slack (THS), timing design rule check (DRC) and crosstalk noise. To

enable the basic quality matrix check, a good base reference is required. Classical method for establishing base reference run is the multiple frequency regression. The optimal frequency can be derived by plotting the target frequency against frequency achieved or target frequency against total negative slack. The spread of frequency sweep is typically 50 MHz or 100 MHz apart, so that the peak achieved frequency or spike of total negative slack can be clearly visible from the graph plotting. The base frequency also can be scaled from older technology design to estimate the possible base frequency. To automate these manual processes, Fmax turner was developed and deployed, as illustrated in Fig. 9 [2].

Fig. 4. TSMC Reference Flow for Cadence Tool [18].

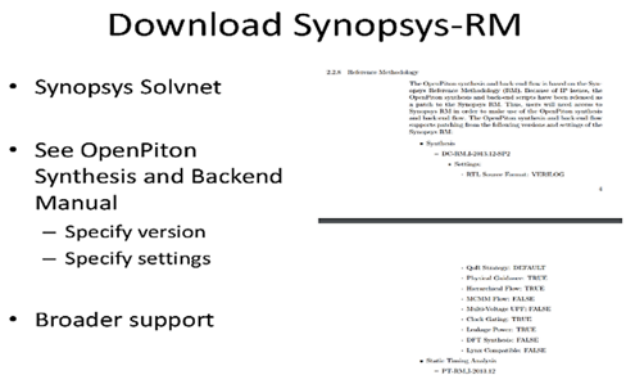

Fig. 5. Field RM Flow Deployment Example [19].

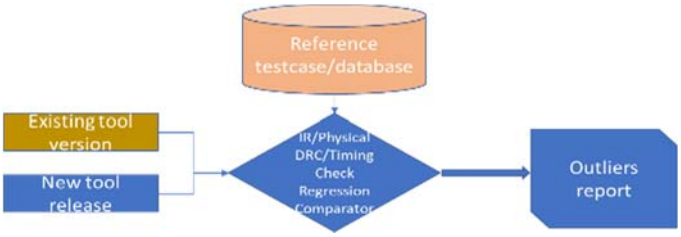

Fig. 6. Signoff Tool Qualification in Outlier Review.

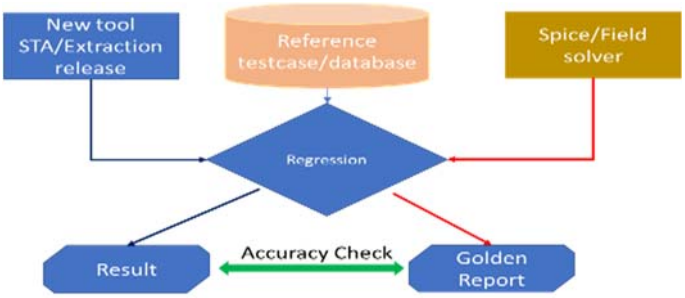

Fig. 7. Signoff Tool Qualification in Accuracy Check.

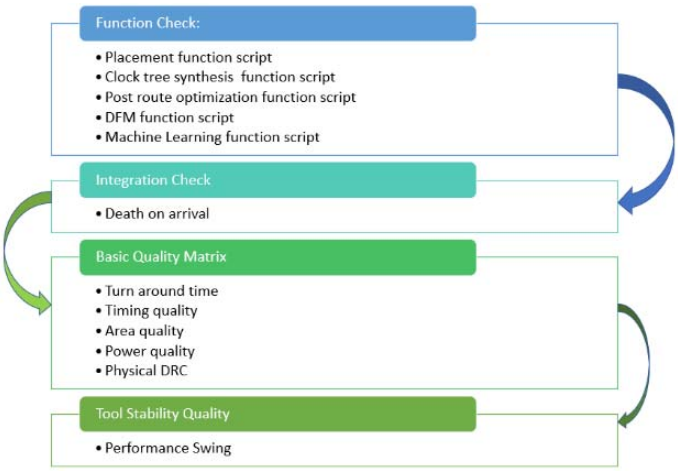

Fig. 8. Implementation Tool Qualification Pillars.

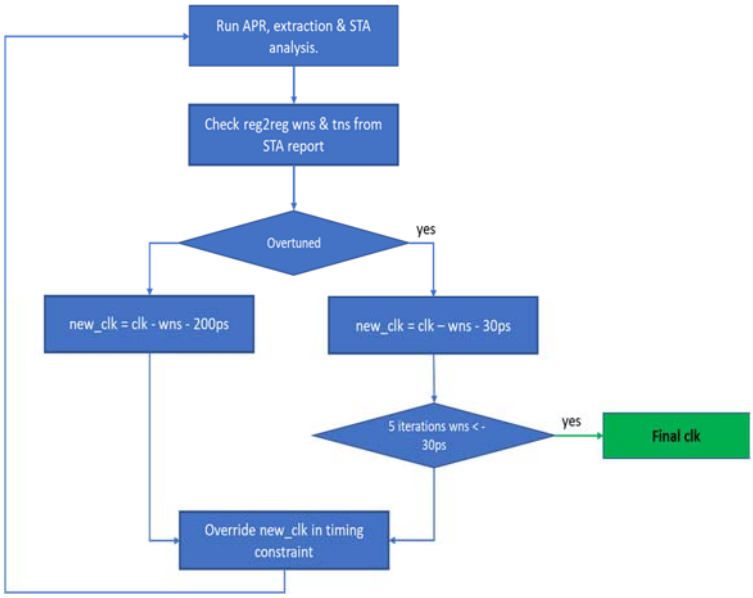

Fig. 9. Fmax Turner [2].

The technology comparison from Fmax turner will not be discussed further in this paper. The basic quality check result will be shared instead.

To enable tool stability quality check, the methodology is shown in Fig. 10. To enable stability quality check, 1 ps frequency adjustment counter is implemented, to adjust the period for the regression. The maximum cumulative adjustment is below 1 % of the max frequency. The results from the stability regression will be used for quality swing analysis. The test-case candidates for the basic quality matrix and the tool stability check, are beyond the discussion of this paper.

The different between the basic quality check against the tool stability check, is the tool stability check is validated based on the same tool version, across technology with 1 ps frequency adjuster. For the basic quality check, the tool version can be different across technology, different tool version for flow release milestone and different tool version for the same technology but different release milestone. The goal for basic quality matrix check is to validate any outliers against known good base (KGB) runs. Hence, the basic quality matrix allows different tool version comparison, different tool flow methodology comparison as well as cross technology benchmark. The tool stability check validates the tool sensitivity on particular technology as well as across technology, based on the same design.

4. Results

4.1. Basic Quality Check

The same sample of the basic quality check snapshot is shown in Fig. 11 and Fig. 12. Fig. 11 shows the quality of result (QoR) based on signoff regression.

From Fig. 12, the turnaround time (TAT) quality check is separated from the rest of basic quality check, as turnaround time (TAT) also affected by the machine workload. There is work in progress for machine workload balancing mechanism, which is beyond the scope of this paper. For confidential reason, all critical parameters such as technology node, process, voltage, temperature and actual performance target will not be revealed in this discussion.

The overview of death on arrival (DOA) and quality of result (QoR) for various design and tool flow release indicators is shown in Fig. 13.

4.2. EDA Tool Stability Quality

For stability check, the regression is done on the same design, across technology. For this evaluation, pure standard cell only design is used. For the performance noise quality, it is illustrated in Fig. 14.

From Fig. 14, for most of the performance target, the swing is around 2 %, except for one performance target, the swing is around 4 %. Further root causing is required, to eliminate the possibility of collateral quality issue.

For the power noise quality plot, it is illustrated in Fig. 15.

For power noise quality, total power is used as total power is dominated by dynamic power. From Fig. 15, it is concluded that the power noise quality swing around 2 % to 5 % range, for less than 1 % noise injection. Though the power swing percentage is larger than performance swing, further evaluation to be done with power recovery feature through signoff tool.

5. Summary

Inhouse tool qualification methodology will increase the confident of the implementation tool deployment instead of relying on the signoff tool as last gating check. It will reduce the risk of product launching delay due to tool-flow-methodology (TFM) quality. From the implementation tool stability qualification, we observe the followings:

- The performance noise of the tested tool version is stable and consistent for most of the technology node;
- The total power noise swing of the EDA tool is 2X of the performance noise swing.

Implementation tool stability qualification flow increase the confident of flow release to project deployment. Hopefully, the sharing will benefit the flow developer.

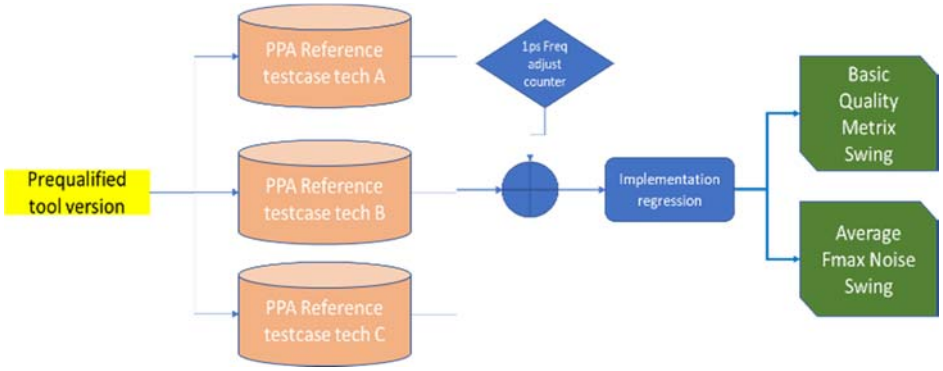

Fig. 10. Tool Stability Check Methodology.

				BlockName	dhm	
Flow	Stage	Metric	Target	Base	Comp-0	Delta-0
FEV_APR	fev_syn2apr	non_equivalent	∓ 10%	0.0	0.0	0%
FEV_APR	disk_usage	overall	∓ 10%	1.309096	1.312196	0.2%
SGDFT_NETLIST_DRC	disk_usage	overall	∓ 10%	0.428536	0.732896	71.0%
SAGE_ATPG	disk_usage	overall	∓ 10%	0.481812	0.483084	0.3%
VCLP_APR	disk_usage	overall	∓ 10%	0.609212	0.609564	0.1%
EXTRACTION	star_pv	errors_starrc	∓ 10%	0.0	0.0	0%
EXTRACTION	star_pv	open_nets	∓ 2%	0.0	0.0	0%
EXTRACTION	star_pv	open_nets_in_spef	∓ 10%	0.0	0.0	0%
EXTRACTION	star_pv	percentage_good_nets	∓ 10%	100.0	99.9531	-0.0%
EXTRACTION	star_pv	shorted_nets	∓ 2%	0.0	7.0	700.0%
EXTRACTION	disk_usage	overall	∓ 10%	0.494364	0.495108	0.2%
NOISE	disk_usage	overall	∓ 10%	3.175484	2.97474	-6.3%
POWER	test1	dynamicpoweruw	∓ 10%	4184.78076824	4141.71359362	-1.0%
POWER	test1	leakage_poweruw	∓ 10%	314.1657	313.7258	-0.1%
POWER	test1	pvscenario	∓ 10%	func.nominal.TM_100.tttt	func.nominal.TM_100.tttt	0%
POWER	test2	pvscenario	∓ 10%	func.highvcc.TT_100.tttt	func.highvcc.TT_100.tttt	0%
POWER	test3	pvscenario	∓ 10%	func.highvcc.TM_100.tttt	func.highvcc.TM_100.tttt	0%
POWER	test4	pvscenario	∓ 10%	func.nominal.TT_100.tttt	func.nominal.TT_100.tttt	0%
POWER	disk_usage	overall	∓ 10%	5.01274	4.723236	-5.8%
LV_CALIBRE	denall	total_errors	∓ 10%	11.0	11.0	0%
LV_CALIBRE	drc	total_errors	∓ 10%	5.0	37.0	640.0%
LV_CALIBRE	disk_usage	overall	∓ 10%	1.069016	1.076668	0.7%
LV_ICV	badpolydummyid	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	check_oas	total_errors	∓ 10%	1203.0	0.0	-100.0%
LV_ICV	check_sp	total_errors	∓ 10%	1194.0	1210.0	1.3%
LV_ICV	con2cell	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	denall	total_errors	∓ 10%	11.0	15.0	36.4%
LV_ICV	drc_IL	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	drc_IPall	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	drc_TUC	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	drcd	total_errors	∓ 10%	2.0	2.0	0%
LV_ICV	dregclmp	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	gnacpin	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	hgate	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	hier_denall_block	total_errors	∓ 10%	9.0	9.0	0%
LV_ICV	libintegrity	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	single_bump	total_errors	∓ 10%	0.0	0.0	0%
LV_ICV	trclvs	total_errors	∓ 10%	0.0	0.0	0%
CALIBER	caliber_func_nominal_TT_100_tttt	must_viols	∓ 10%	1023.0	1058.0	2.4%
CALIBER	disk_usage	overall	∓ 10%	1.947972	1.835536	-5.8%
STA_PT	func_highvcc_TM_100_tttt__min	int__lt_n50	∓ 10%	42.0	0.0	-100.0%
STA_PT	func_highvcc_TM_100_tttt__min	int__n50_n30	∓ 10%	72.0	4.0	-94.5%
STA_PT	func_highvcc_TM_100_tttt__min	tns	∓ 10%	-17024.449999999993	-5826.889999999996	-65.8%
STA_PT	func_highvcc_TM_100_tttt__min	wns	∓ 10%	-336.07	-198.23	-41.0%
STA_PT	func_highvcc_TM_100_tttt__min	tns_c2c	∓ 10%	0.0	0.0	0%
STA_PT	func_highvcc_TM_100_tttt__min	wns_c2c	∓ 10%	0.0	0.0	0%
STA_PT	func_highvcc_TM_100_tttt__min	tns_int	∓ 10%	-7218.069999999993	-1163.6299999999976	-83.9%
STA_PT	func_highvcc_TM_100_tttt__min	wns_int	∓ 10%	-114.3	-42.73	-62.6%
STA_PT	func_highvcc_TT_100_tttt__max	int__lt_n50	∓ 10%	0.0	0.0	0%
STA_PT	func_highvcc_TT_100_tttt__max	int__n50_n20	∓ 10%	0.0	0.0	0%
STA_PT	func_highvcc_TT_100_tttt__max	tns	∓ 10%	-337366.9200000002	-190663.26000000004	-43.5%
STA_PT	func_highvcc_TT_100_tttt__max	wns	∓ 10%	-470.0	-342.66	-27.1%
STA_PT	func_highvcc_TT_100_tttt__max	tns_c2c	∓ 10%	0.0	0.0	0%
STA_PT	func_highvcc_TT_100_tttt__max	wns_c2c	∓ 10%	0.0	0.0	0%
STA_PT	func_highvcc_TT_100_tttt__max	tns_int	∓ 10%	0.0	0.0	0%
STA_PT	func_highvcc_TT_100_tttt__max	wns_int	∓ 10%	0.0	0.0	0%
STA_PT	func_nominal_TM_100_tttt__min	int__lt_n50	∓ 10%	22.0	0.0	-100.0%
STA_PT	func_nominal_TM_100_tttt__min	int__n50_n30	∓ 10%	65.0	0.0	-100.0%
STA_PT	func_nominal_TM_100_tttt__min	tns	∓ 10%	-7160.699999999999	-20978.21000000001	193.0%
STA_PT	func_nominal_TM_100_tttt__min	wns	∓ 10%	-180.31	-151.55	-16.0%
STA_PT	func_nominal_TM_100_tttt__min	tns_c2c	∓ 10%	0.0	0.0	0%
STA_PT	func_nominal_TM_100_tttt__min	wns_c2c	∓ 10%	0.0	0.0	0%
STA_PT	func_nominal_TM_100_tttt__min	tns_int	∓ 10%	-5091.36	-1.2	-100.0%
STA_PT	func_nominal_TM_100_tttt__min	wns_int	∓ 10%	-180.31	-1.2	-99.3%
STA_PT	func_nominal_TT_100_tttt__max	int__lt_n50	∓ 10%	0.0	0.0	0%
STA_PT	func_nominal_TT_100_tttt__max	int__n50_n20	∓ 10%	0.0	0.0	0%
STA_PT	func_nominal_TT_100_tttt__max	tns	∓ 10%	-333526.2399999997	-163706.00000000003	-50.9%
STA_PT	func_nominal_TT_100_tttt__max	wns	∓ 10%	-626.74	-502.44	-20.9%
STA_PT	func_nominal_TT_100_tttt__max	tns_c2c	∓ 10%	0.0	0.0	0%
STA_PT	func_nominal_TT_100_tttt__max	wns_c2c	∓ 10%	0.0	0.0	0%
STA_PT	func_nominal_TT_100_tttt__max	tns_int	∓ 10%	-568.9899999999999	-82.0	-85.6%
STA_PT	func_nominal_TT_100_tttt__max	wns_int	∓ 10%	-91.96	-9.51	-89.6%
STA_PT	disk_usage	overall	∓ 10%	1.845584	1.797588	-2.6%
PT_ECO	disk_usage	overall	∓ 10%	2.424356	2.321332	-4.2%
FILL_DP_FC	disk_usage	overall	∓ 10%	1.25268	1.252988	0.0%
APR_ECO	disk_usage	overall	∓ 10%	1.396752	1.38864	-0.6%

Fig. 11. Basic Quality Check Snapshot.

Results ...

Show violations only

				BlockName	parmcschbsddr	
Flow	Stage	Metric	Target	Base	Comp-0	Delta-0
PREPARE_INDICATOR	clock_route_opt	elapsed_time	∓ 10%	11.67 hours	9.24 hours	-20.8%
PREPARE_INDICATOR	compile_final_opto	elapsed_time	∓ 10%	2.91 hours	2.43 hours	-16.5%
PREPARE_INDICATOR	compile_initial_opto	elapsed_time	∓ 10%	3.92 hours	3.22 hours	-17.9%
PREPARE_INDICATOR	cts	elapsed_time	∓ 10%	0.92 hours	0.76 hours	-17.4%
PREPARE_INDICATOR	fill	elapsed_time	∓ 10%	1.67 hours	1.50 hours	-10.2%
PREPARE_INDICATOR	finish	elapsed_time	∓ 10%	0.49 hours	0.43 hours	-12.2%
PREPARE_INDICATOR	floorplan	elapsed_time	∓ 10%	0.51 hours	0.40 hours	-21.6%
PREPARE_INDICATOR	import_design	elapsed_time	∓ 10%	0.33 hours	0.27 hours	-18.2%
PREPARE_INDICATOR	init_floorplan	elapsed_time	∓ 10%	0.08 hours	0.08 hours	0%
PREPARE_INDICATOR	initial_map	elapsed_time	∓ 10%	0.82 hours	0.70 hours	-14.6%
PREPARE_INDICATOR	insert_dft	elapsed_time	∓ 10%	0.30 hours	0.28 hours	-6.7%
PREPARE_INDICATOR	logic_opto	elapsed_time	∓ 10%	1.11 hours	0.92 hours	-17.1%
PREPARE_INDICATOR	quick_route	elapsed_time	∓ 10%	4.74 hours	10.30 hours	117.3%
PREPARE_INDICATOR	read_upf	elapsed_time	∓ 10%	0.09 hours	0.11 hours	22.2%
PREPARE_INDICATOR	redefine	elapsed_time	∓ 10%	0.10 hours	0.08 hours	-20.0%
PREPARE_INDICATOR	route_auto	elapsed_time	∓ 10%	5.18 hours	11.02 hours	112.7%
PREPARE_INDICATOR	route_opt	elapsed_time	∓ 10%	31.16 hours	26.99 hours	-13.4%
PREPARE_INDICATOR	setup_timing	elapsed_time	∓ 10%	0.16 hours	0.14 hours	-12.5%

Fig. 12. Runtime Basic Quality Check Snapshot.

Fig. 13. Release Metric Indicator.

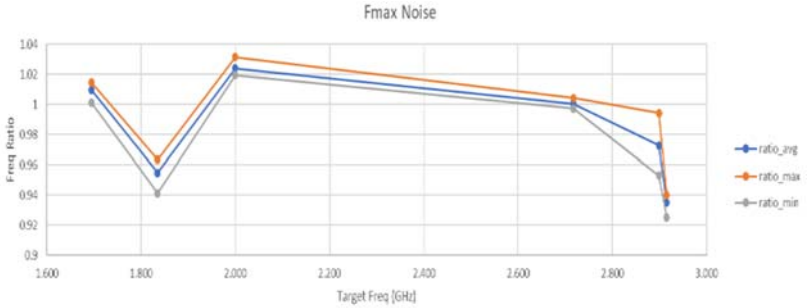

Fig. 14. Fmax Noise Quality.

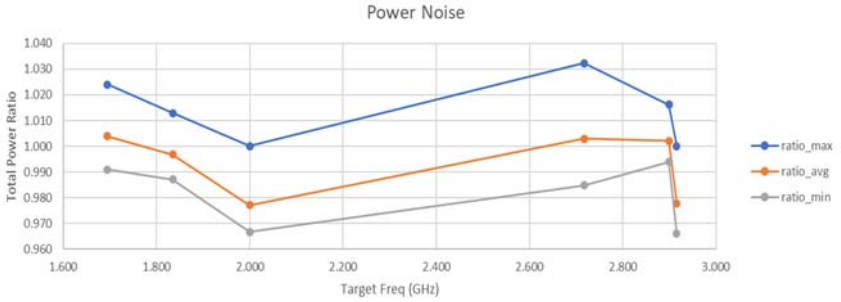

Fig. 15. Power Noise Quality.

Acknowledgements

Thanks to management for the support given.

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(041)

Impact of Mask Tapering on SF_6/O_2 Plasma Etching

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Summary: We implement a physical SF_6/O_2 plasma etching model which is based on Langmuir equations. The simulation is performed using Monte Carlo ray tracing to calculate the surface rates and coverages in order to ultimately obtain the final surface velocities. The model was implemented using the in-house Level Set-based process simulator ViennaPS and it was validated by matching the simulated profiles to published experimental studies. The variables which were used for the best fits matched well with those published in the literature. The model is then used to study the impact of mask tapering on the feature profile in a cylindrical trench. We found that increasing the positive tapering results in a higher etch rate at the bottom of the trench, ultimately resulting in a deeper vertical trench for tapered masks. Increasing the mask tapering also results in more bowing along the cylindrical walls. This is a consequence of particles reflecting off of the mask layer and striking the sidewalls at high angles.

Keywords: Plasma Etching, High aspect ratio, 3D integration, SF_6/O_2, Mask tapering.

1. Introduction

As packaging becomes the bottleneck towards achieving more-than-Moore integration and high density in functionality and increased performance, the heterogeneous integration of die with different functionalities grows in importance. The layers of the required three-dimensional (3D) structure are electrically connected using vias - vertical interconnects - through e.g. silicon, in the case of through-silicon vias (TSVs). This leads to an increased demand for high aspect ratio (HAR) structures. Plasma etching is one of the most frequently used fabrication steps to generate such structures; however, the process is complex and providing a physical model which includes all relevant physics is a challenging task. Accurate physical models are essential since the only alternative is repeated experiments which involve many trial-and-error procedures, due to the sheer complexity of plasma etching [4].

A commonly used technology to generate HAR TSVs is the Bosch process, otherwise known as Deep Reactive Ion Etching (DRIE). DRIE is a cyclical process which includes cycles of SF_6/O_2 plasma etching and conformal layer deposition. For some geometries SF_6/O_2 plasma etching can be used independently to etch tapered via profiles [3], albeit with several limitations when compared to DRIE.

We implemented the SF_6/O_2 plasma etching model in the in-house developed Level Set-based process simulator ViennaPS. The model was validated by matching the simulation profiles to experimentally obtained cylindrical holes and comparing the obtained process variables to the reported variables from Belen et al. [1]. Subsequently, we used the model to take a qualitative look at the influence of silicon oxide mask tapering on the etched hole profile.

2. TCAD Workflow

We implemented the plasma etching model in the in-house simulator ViennaPS (PS for process simulator) by following the workflow suggested in [4] using the Level Set library ViennaLS and the top-down ray tracer ViennaRay. ViennaLS uses the Level Set method to simulate the surface, while the ray tracer computes particle rates at the surface. The particle rates are then used in the surface chemistry model to obtain the surface advection velocities.

2.1. The Level-Set Method

The Level-set method is a form of implicit surface representation, where the surface is described by a signed distance function (SDF) $\phi(\vec{x})$. The function is defined on a Cartesian grid with a value defined at each point in space. The surface is then located by points where the function equals a specific scalar value, typically zero. In this case, the surface is located at the zero level set. $\phi(\vec{x})$ is constructed based on the signed distance d of a domain point $\vec{x}$ from the surface S bounding the volume M:

$$\phi(\vec{x}) = \begin{cases} -d, & \vec{x} \in M \\ 0, & \vec{x} \in S \\ d, & \vec{x} \notin M \end{cases} \quad (1)$$

The sign of $\phi(\vec{x})$ indicates whether the point is inside or outside of the volume. The time evolution of the surface is described by the surface normal velocity $v(\vec{x})$. For a typical geometry with non constant SDF gradient, the gradient is used to normalize $v(\vec{x})$ which leads to the level set equation:

$$\frac{\partial\phi(\vec{x},t)}{\partial t} + v(\vec{x})|\nabla\phi(\vec{x},t)| = 0 \quad (2)$$

The resulting velocity is subsequently used to update the SDF $\phi(\vec{x})$. The SDF values are typically stored at the points defined on a regular grid and, as the surface evolves, the points remain at the same position while their SDF value changes [6]. This is why this method of storing the surface is referred to as "implicit", since the exact location of the surface in space is not explicitly known.

2.2. Surface Model Description

To describe the temporal simulation of feature scale SF_6/O_2 plasma etching, we consider the rates of ions and neutral particles - oxygen and fluorine - along with their surface coverages at each time step. The ray tracer is employed to compute particle impingement rates which are, in turn, used to compute coverages and ultimately the surface velocity. The coverages θ are calculated based on a Langmuir–Hinshelwood-type surface site balance equation [2], shown in equations (3) and (4). Oxygen and fluorine rates are dependent on the surface coverage at the impact point. Particle rates are used to compute their fluxes on the surface, denoted by Γ. Equation (5) shows how the surface velocity is calculated. The first term represents chemical etching, followed by physical sputtering, and finally the ion-enhanced etching. Both sputtering and ion-enhanced etching depend on the ion incidence angle accounted for by the yield terms Y_p and Y_{Si}, respectively [2]:

$$\sigma_{Si}\frac{d\theta_F}{dt} = \gamma_F\Gamma_F(1-\theta_F-\theta_O) - k\sigma_{Si}\theta_F - 2Y_{Si}\Gamma_i\theta \quad (3)$$

$$\sigma_{Si}\frac{d\theta_O}{dt} = \gamma_O\Gamma_O(1-\theta_F-\theta_O) - \beta\sigma_{Si}\theta_O - Y_O\Gamma_i\theta_(\quad (4)$$

$$R_{etch} = \frac{1}{\rho_{Si}}\left(\frac{k\sigma_{Si}\theta_F}{4} + Y_p\Gamma_i + Y_{Si}\Gamma_i\theta_F\right) \quad (5)$$

In the above equations, Γ_F and Γ_O are the fluorine and oxygen fluxes, respectively, θ_F and θ_O are their respective surface coverages γ_F and γ_O are sticking coefficients on a clean surface, $k\sigma_{Si}$ is the chemical etch reaction rate constant, $\beta\sigma_{Si}$ is the oxygen recombination rate and ρ_{Si} is the Si density. Assuming pseudo-steady-state conditions, the equations (1) and (2) simplify to:

$$\theta_F = \left(1 + \left(\frac{k\sigma_{Si} + 2Y_{Si}\Gamma_i}{\gamma_F\Gamma_F}\right)\left(1 + \frac{\gamma_O\Gamma_O}{\beta\sigma_{Si} + Y_O\Gamma_i}\right)\right)^{-1} \quad (6)$$

$$\theta_O = \left(1 + \left(\frac{\beta\sigma_{Si} + Y_{SiO_2}\Gamma_i}{\gamma_O\Gamma_O}\right)\left(1 + \frac{\gamma_F\Gamma_F}{k\sigma_{Si} + 2Y_{Si}\Gamma_i}\right)\right)^{-1} \quad (7)$$

3. Results and Discussion

The etch rate and feature profile shape depend on the composition of the chamber gas, the RF bias, the pressure, and the feature size. The fluorine flux Γ_F, and oxygen flux Γ_O are varied to model the composition of the chamber gas, the ion energy encapsulates the effect of RF bias, and the pressure is not modeled directly, but is rather included in the model by matching the simulations to experimentally-obtained profiles. To calibrate and validate our model, we used experimental data from [1]. 3D simulations of SF_6/O_2 plasma etching through 0.35 µm diameter holes using a 1.2 µm thick oxide mask are performed and the relevant process parameters are calibrated to match the experimental SEM profiles, obtained by varying the chamber gas composition and by varying the pressure [1]. The reactor setup from the experiment is provided in Table 1. The variables which were shown to provide the best fit are shown in Table 2 and Table 3.

Table 1. Reactor setup for experimentally obtained profiles from [1] used for validation. The RF-bias which was applied while varying pressure was -20 V.

Process Parameter	Value
Pressure	10 - 45 mTorr
Total gas flow rate	80 sccm
Inductive coil power	800 W
RF-bias voltage	-20 V, -120 V
Wafer temperature	5 °C
O_2 fraction in feed, y_{O_2}	0.44 - 0.62

Table 2. Variable sets for simulating the best matches to experimentally-obtained profiles in variable chamber gas compositions.

Param.	y_{O_2} = 0.44	y_{O_2} = 0.5	y_{O_2} = 0.56	y_{O_2} = 0.62
F flux, $cm^{-2}\ s^{-1}$	4.8×10^{18}	4.5×10^{18}	4×10^{18}	3.5×10^{18}
O flux, $cm^{-2}\ s^{-1}$	3×10^{17}	8×10^{17}	2×10^{18}	2.5×10^{18}
Ion flux,$cm^{-2}\ s^{-1}$	1×10^{16}	1×10^{16}	1×10^{16}	1×10^{16}
F sticking, γ_F	0.7	0.7	0.7	0.7
O sticking, γ_F	1	1	1	1
A_O	4	3	2	1
A_{Si}	5	5	5	5
$\beta\sigma_{Si}$, $cm^{-2}\ s^{-1}$	8×10^{13}	8×10^{13}	8×10^{13}	8×10^{13}

Table 3. Variable sets for simulating the best matches to experimentally-obtained profiles under variable chamber pressures.

Param.	P = 10 mTorr	P = 25 mTorr	P = 40 mTorr
F flux, cm^{-2} s^{-1}	2×10^{18}	7×10^{18}	1×10^{19}
O flux, cm^{-2} s^{-1}	1×10^{17}	3×10^{17}	8×10^{17}
Ion flux,cm^{-2} s^{-1}	1×10^{16}	7×10^{15}	4.5×10^{15}

3.1. Impact of Varying Gas Composition

In this section, we examine the impact of varying the difference in concentration between the SF_6 and O_2 gases. The simulation with the lowest oxygen content resulted in the highest lateral etch rate, shown in Fig. 1a. With an increase in oxygen flux, the sidewall passivation becomes more pronounced and lateral etching is decreased, while higher oxygen coverage directs more fluorine flux towards the bottom of the hole, resulting in a higher vertical etch yield Fig. 1b.

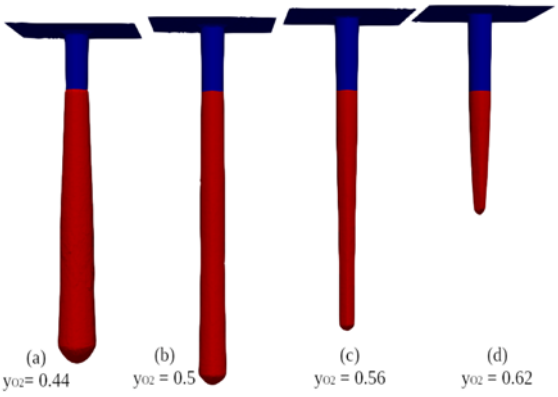

Fig. 1. Simulated 3D profiles using the parameters from Table 2. An increase in oxygen content hinders lateral etching and initially enhances vertical etching (a) and (b). Further increasing the O_2 flux leads to negative tapering and reduced vertical etching (c) and (d).

As the oxygen flux is further increased and the fluorine flux is decreased, the sidewall tapering changes from positive to negative (cf. Fig. 1c) and inhibits vertical etching (cf. Fig. 1d). We additionally overlaid the cross-sections of the simulation results with experimentally observed ones from [1] in Fig. 2, where the described trends are clearly visible. The absolute values of the fluxes and other model parameters which were determined by fitting the profiles are reasonably close to the ones reported in [1], with the only significant difference being the oxygen recombination rate, which is doubled in our results. Additionally, the F-to-O flux ratios differ in absolute terms - our simulations produced the best fit with differences between the F and O fluxes. However, the trend of change is consistent with the increase in O fraction and similar to the one in the reference simulation.

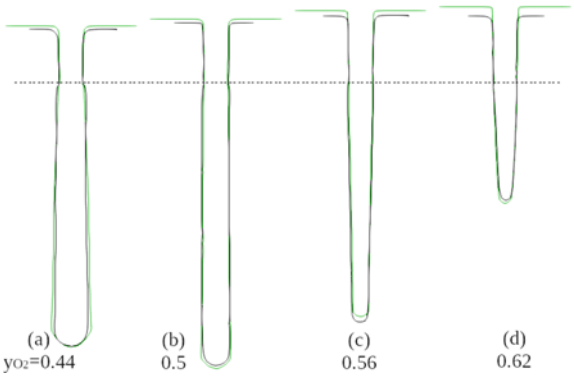

Fig. 2. Cross sections of the simulated etched holes from Fig. 1 in green laid over the experimental results from [1] shown in black. The profiles are an excellent match up to the oxide mask etching. The dashed line shows the location of the mask-Si interface.

3.2. Impact of Varying Chamber Pressure

We repeated the process from the previous section in order to study the effects of induced pressure variations. Changes in feature profiles were closely captured by varying neutral and ion fluxes, shown in Table 3. Increasing the pressure leads to higher F and O fluxes and a lower ion flux at the surface. At the low pressure, the inhibiting effect of oxygen coverage is less significant and we observe positive sidewall tapering (cf. Fig. 4a). As the pressure increases, despite a decreased ion flux, vertical etching slightly increases due to the same effect of more fluorine reflecting towards the bottom (cf. Fig. 4b). Further increasing the pressure inhibits both vertical and lateral etching and changes the sidewall tapering from positive to negative (cf. Fig. 4c).

The model parameters which are shown to produce the best fit to experimental data are provided in Table 3. These values agree well with those reported in [1]. The largest difference is in the ion flux, which is about one half the value in the case when the lowest pressure is applied. F and O fluxes are very close to the ones reported in literature [1]. It is reasonable to expect that the ratio is constant as the gas composition is kept constant, but the simulation parameters do not reflect this. This discrepancy is consistent with the results presented in [1] and is due to the fact that the applied pressure impacts the flows of the fluorine and oxygen molecules differently.

A good fit to the experimental data is achieved using physically reasonable values, which brings

confidence that the model can be used to describe a wider variety of plasma etching settings. However, the model fails to describe the impact of the increase in oxygen flux on the mask etching with full accuracy (cf. Fig. 3d) and a further study is necessary.

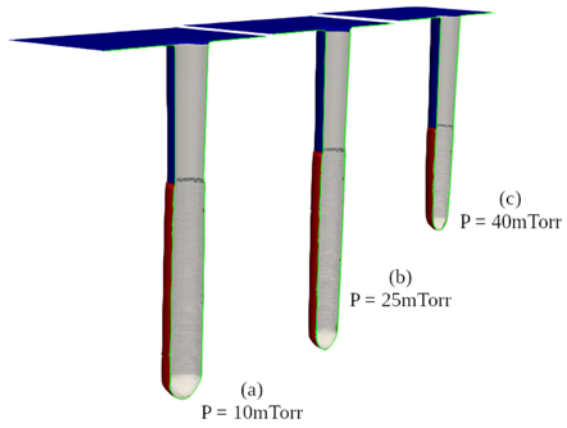

Fig. 3. Simulated 3D profiles using the parameters from Table 3. The profiles are clipped at the middle where the cross sections shown in Fig. 3 are taken.

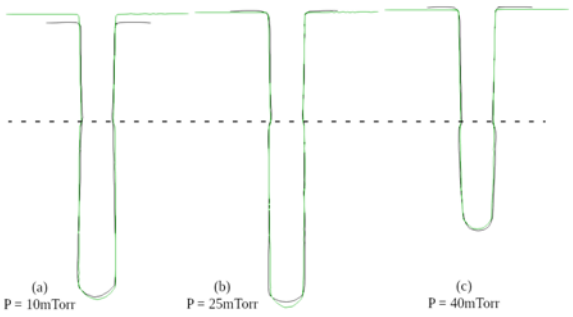

Fig. 4. Cross sections of the simulated etched holes from Fig. 3 in green laid over the experimental results of pressure variation from [1] shown in black. The dashed line shows the mask-Si interface.

3.3. Impact of Varying Mask Tapering

We finally use our model for a qualitative insight into the impact of mask tapering on the etched feature profile. We applied the parameter set describing y_{O2} = 0.56 from Table 2 as it results in a desirable positive tapering for the via, while the mask etching inaccuracy is not as significant. The mask tapering is varied from 0° to 4°, with selected profiles showing the trends depicted in Fig. 5 and the plot of depth and width-at-half-depth (width) vs. the tapering angle in Fig. 6.

The initial increase in the mask taper angle (from 0° to 0.5°) enhances the vertical etching since more ions get directly reflected towards the bottom. As the vertical etching approaches its peak, the increase in the angle means more ions start getting reflected directly towards the sidewalls, which leads to a rapid increase of the width-at-half-depth, around the angle of 0.5°, and a minimal increase in the vertical etching. This minimal increase happens as the ions can still reflect to the bottom, albeit with a lower energy. Further increasing the angle serves to only redirect more ions towards the sidewall and less towards the bottom. The ions get reflected higher up the sidewall, closer to the mask, as the angle is increased. This forms the frequently-observed bowing in such holes or trench geometries. Since oxygen coverage is the highest at these positions, the lateral etching still gets reduced. For angles greater than 2°, both vertical and lateral etching is reduced as less ions are reflected downwards through the narrow mask bottom.

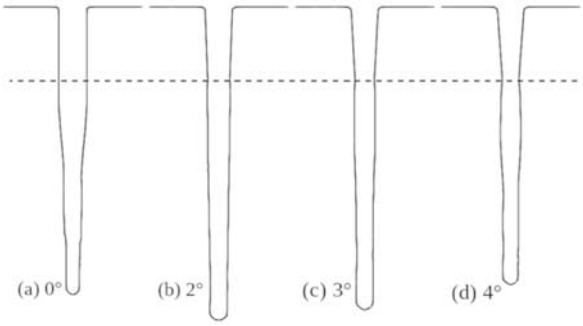

Fig. 5. Cross sections of the etched holes obtained by varying the mask tapering. 1° tapering is omitted as it shows the same profile as the 2°-tapered profile.

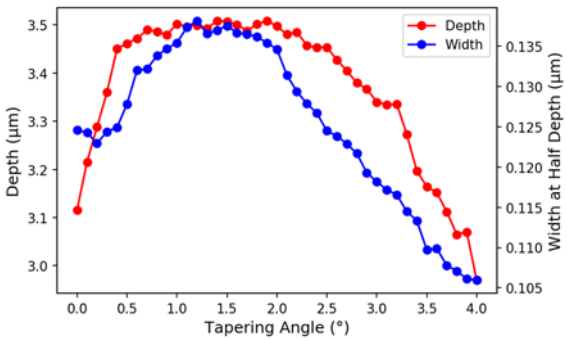

Fig. 6. Depth and width-at-half-depth vs. mask tapering angle. Both parameters peak after an initial angle increase and decrease significantly as the angle increases further and makes the mask bottom narrower.

4. Conclusion

We implemented a 3D feature-scale model for SF_6/O_2 plasma etching, validated it by fitting the profiles to experimental data, and compared the parameters to those provided in literature. The model was further applied to study the impact of the mask tapering on the feature profile.

With our model, we were able to link equipment settings, such as applied pressure and gas composition to relevant model parameters. The results show good agreement with experiments and previously published values.

We also note that mask tapering, which is often unavoidable in lithography processing, has a significant effect on the feature profile. Both the hole

depth and width-at-half-depth reach a maximum at a tapering angle between 1° and 1.5°. Therefore, perfectly vertical mask sidewalls will not produce the highest hole etch rates. With this approach, we also show that we are able to reproduce observed bowing effects in these three-dimensional geometries.

Acknowledgements

This work was supported in part by the Austrian Research Promotion Agency FFG (Bridge Young Scientists) under Project 878662 ”Process-Aware Structure Emulation for Device-Technology Co-Optimization”.

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ISBN 978-84-09-43856-3