

Microelectronic Devices and Technologies

Proceedings of the 8th International Conference
on Microelectronic Devices and Technologies
(MicDAT '2026)



30 September - 2 October 2026
Granada, Spain



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Edited by Sergey Y. Yurish



Sergey Y. Yurish, *Editor*
Microelectronic Devices and Technologies
MicDAT '2026 Conference Proceedings

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ISBN: 978-84-09-90032-9

BN-20260923-XX

BIC: TJFD

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Foreword

The continuing development of microelectronics remains one of the fundamental driving forces behind technological progress. At the same time, emerging applications in artificial intelligence, communications, autonomous systems, sensing, industrial automation, and energy technologies are placing new and increasingly demanding requirements on microelectronic devices and their design.

An important feature of contemporary microelectronics is the growing convergence of traditionally separate technology domains. Progress can no longer be achieved solely through transistor scaling. Increasing attention is being given to system-level optimization, heterogeneous integration, three-dimensional integration, System-on-Chip and System-in-Package solutions, advanced packaging, novel materials, and new computing architectures. These approaches offer opportunities to improve performance, functionality, energy efficiency, and reliability while addressing the physical and economic limitations of conventional scaling.

The contributions presented within the framework of MicDAT' 2026 reflect this continuing transformation. They encompass analog, digital, mixed-signal and RF circuits; semiconductor devices and processing technologies; VLSI systems; microprocessors and embedded systems; low-power electronics; electronic materials; nanoelectronics and spintronics; flexible and stretchable electronics; MEMS, MOEMS and NEMS technologies; optoelectronics; computer-aided design; modeling, simulation and verification; reliability and qualification; thermal management; and assembly and packaging. Each paper has undergone careful peer review to ensure scientific quality and relevance.

Particular attention is also being directed toward the rapidly expanding interaction between microelectronics and artificial intelligence. Modern AI applications require increasingly specialized and energy-efficient hardware, while embedded intelligence is moving progressively closer to sensors, actuators, and physical processes. Edge AI, TinyML, non-von Neumann architectures, neuromorphic approaches, and hardware accelerators are creating new requirements for device technologies, circuit architectures, memory systems, data converters, and system integration. This interaction between advanced hardware and intelligent algorithms is likely to remain one of the major technological drivers of the coming years.

MicDAT' 2026 is intended not only to present scientific results but also to encourage the exchange of knowledge between academia and industry. Such interaction is particularly important in microelectronics, where progress depends on close cooperation between fundamental research, design methodologies, fabrication technologies, equipment development, and practical application requirements. By providing a common forum for these communities, the conference contributes to identifying emerging challenges, exchanging technological experience, and developing new opportunities for international collaboration.

The conference is organized under the umbrella of the International Frequency Sensor Association (IFSA) and is co-located with the XII International Conference on Sensors and Electronic Instrumentation Advances (SEIA' 2026). This combination creates additional opportunities for interaction between specialists in microelectronics, sensors, instrumentation, embedded systems, and intelligent technologies, reflecting the increasingly interdisciplinary nature of modern electronic engineering.

I would like to express my sincere gratitude to all authors for contributing their research to MicDAT' 2026. My special thanks go to the members of the International Program Committee and the reviewers for their valuable expertise and careful evaluation of the submitted papers.

I hope that these Proceedings will provide a valuable reference for researchers, engineers, and practitioners and will stimulate further scientific exchange, technological development, and international cooperation in the rapidly evolving field of microelectronic devices and technologies.

Prof., Dr. Sergey Y. Yurish
MicDAT' 2026 Chairman

Active-Only Current-Controlled Memcapacitor Emulator Circuit

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Summary: This study presents a compact circuit topology for emulating a current-controlled memcapacitor. The proposed structure uses only active elements, including current-controlled current conveyors (CCCI), an operational transconductance amplifier (OTA), bipolar junction transistors (BJTs), and an analog multiplier to obtain nonlinear response and pinched hysteresis characteristics. An internal capacitor ensures dynamic operation without requiring external passive resistors. With low component count and simple structure, the circuit provides a practical alternative to earlier designs. Theoretical analysis and Cadence simulations confirm feasibility, reliability, and agreement with predicted circuit behaviour.

Keywords: Current-controlled memcapacitor, Active-element emulator, Nonlinear hysteresis, Analog circuit design.

1. Introduction

The memristor is regarded as the fourth fundamental passive circuit element alongside the resistor, capacitor, and inductor [1]. It establishes the missing relation between charge and magnetic flux and exhibits a nonlinear I–V characteristic with a pinched hysteresis loop. First introduced theoretically by Chua in 1971 [1] and generalized by Chua and Kang in 1976 [2, 3], the memristor gained significant attention after its physical realization using TiO₂ by HP Labs in 2008 [4].

Memristive devices can retain their resistance state without power, enabling non-volatile memory applications. Owing to their nonlinear and memory-dependent behaviour, they are widely studied for neuromorphic systems, adaptive circuits, oscillators, and memory technologies [5]. However, due to limited practical implementations, most research relies on SPICE models and emulator circuits [6]. Since memristors do not intrinsically store energy, memcapacitor and meminductor concepts were introduced as memory-based energy storage elements [7]. Various memcapacitor emulator circuits have been reported using different active building blocks and circuit configurations. Earlier designs typically use multiple active devices together with passive components, which increases circuit complexity and reduces integration suitability. Many reported implementations employ combinations of OTAs, CCIs, VDTAs, multipliers, and passive elements, leading to relatively complex structures [8-10]. In contrast, the proposed memcapacitor emulator (MEC) uses a compact fully active architecture consisting of 2 CCCIs, 2 voltage buffers, 2 BJTs, 1 OTA and 1 analog multiplier without passive capacitors.

Unlike the authors' previous active-only memcapacitor emulator based on current-conveyor integrator stages and intrinsic buffer capacitances [11], the present work introduces a current-controlled

charge-dependent memcapacitor realization employing a BJT-based sinh nonlinear block together with an OTA/multiplier stage to realize the desired memcapacitance characteristic. Therefore, the main contribution of this work is not the active-only implementation concept itself, but the proposed current-controlled nonlinear architecture, its analytical charge-domain memcapacitance formulation, and its validation through XFAB 0.18 μm CMOS simulations. Moreover, the proposed circuit offers electronic tunability via bias currents, resulting in a simpler and more compact implementation. The remainder of this paper is organized as follows: Section 2 describes the proposed MEC architecture and its operating principle, while Section 3 presents the simulation results. Section 4 provides a performance comparison between the proposed MEC and previously reported memcapacitor emulator circuits. Section 5 analyzes the proposed MEC by considering non-ideal effects, Section 6 demonstrates an application of the proposed MEC, and finally, Section 7 concludes the paper.

2. Basic Design Concepts for Proposed MEC

The proposed circuit is developed based on an active-only design strategy, guided by the following design considerations:

- i) In this work, an active-only design approach is adopted by utilizing the intrinsic MOSFET gate capacitance (C_{gs}) instead of external passive capacitors. Since C_{gs} remains nearly constant over a wide range of V_{GS} , it can be regarded as a linear capacitor [12].
- ii) Incorporating this intrinsic capacitance into the circuit synthesis enables high-frequency operation while reducing chip area due to the high capacitance density of MOS transistors. This design philosophy differs from conventional approaches that treat transistors as

ideal active elements. The proposed emulator consists of two CCCII-based integrator stages, each followed by a buffer unit. In both integrators, the intrinsic gate-to-source capacitance (C_{gs}) of the buffer input is intentionally utilized as the integration capacitor, eliminating the need for external passive capacitors. The nonlinear “sinh” function is realized using a matched bipolar transistor pair, while an OTA and an analog multiplier complete the emulator architecture shown in Fig. 1. The resulting nonlinear state-dependent memcapacitance gives rise to the characteristic pinched hysteresis behavior.

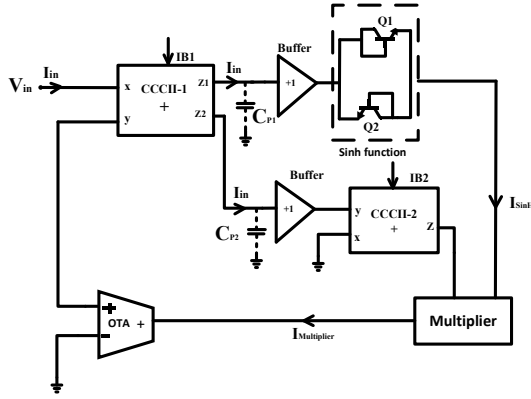


Fig. 1. Circuit diagram of the proposed MEC circuit.

Based on the constitutive equation of the CCCII in [13], the fundamental relationships required for deriving the memcapacitance are formulated as follows:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & r_x & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix}, \quad (1)$$

$$I_{CP1} = I_{in} = C_{P1} \frac{dV_{CP1}}{dt} \quad V_{CP1} = \frac{q_{in}}{C_{P1}}, \quad (2)$$

$$I_{Q1} + I_{Q2} = I_S (e^{\frac{V_{C1}}{V_T}} + e^{-\frac{V_{C2}}{V_T}} - 2) \quad V_{C1} = -V_{C2}, \quad (3)$$

where V_T and I_S represent the thermal voltage and saturation current, respectively.

$$I_{sinh} = 2I_S [\sinh(\frac{q_{in}}{C_{P1}V_T}) - 1] \quad (4)$$

Based on the above analysis, the output of the analog multiplier can be formulated as:

$$I_{multiplier} = I_{sinh} \cdot I_{Z2} \quad (5)$$

The voltage across the C_{P2} capacitor is readily obtained from the circuit equations. This voltage is

then converted into a current by the CCCII-(2), which serves as a voltage-to-current conversion stage. The resulting current is subsequently multiplied by the I_{sinh} current using an analog multiplier, yielding the desired output signal.

$$I_{CP2} = I_{in} = C_{P2} \frac{dV_{Y2}}{dt}, \quad (6)$$

$$V_{Y2} = \frac{q_{in}}{C_{P2}} I_{Z2} = \frac{V_{Y2}}{r_{x2}} = \frac{q_{in}}{r_{x2}C_{P2}} \quad (7)$$

If the relationship between the applied input voltage and input current is formulated, it can be written as follows:

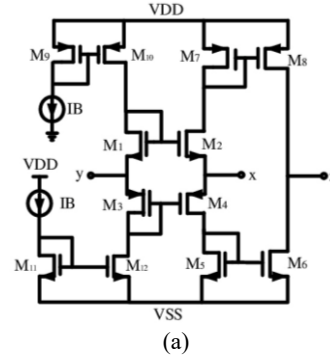
$$V_{in} = i_{in}r_x + V_{Y1}, \quad (8)$$

$$I_{multiplier} = G_m V_{Y1} = G_m (V_{in} - i_{in}r_x) \quad (9)$$

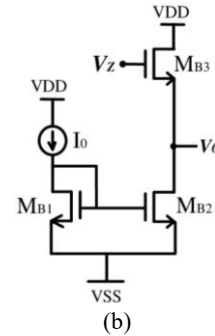
By rearranging the equation and utilizing the capacitor constitutive relation, $q(t) = Cv(t)$, the expression for the memcapacitance is obtained as follows:

$$C_M^{-1} = \frac{V_{in}(t)}{q_{in}} = \frac{2I_S}{G_m r_{x2} C_{P2}} [\sinh(\frac{q_{in}}{C_{P1}V_T}) - 1] + r_x \frac{i_{in}}{q_{in}}, \quad (10)$$

where G_m denotes the transconductance of the OTA, while C_{P1} and C_{P2} represent the equivalent capacitances observed at the inputs of the two voltage buffers. The implementation of the CCCII active element based on a standard trans-linear configuration is depicted in Fig. 2(a), whereas the voltage buffer circuit is presented in Fig. 2(b).



(a)



(b)

Fig. 2. (a) Transistor-level CMOS implementation of the CCCII [14]; (b) CMOS voltage buffer circuit.

The design of the proposed circuits is based on two primary considerations. First, the voltage buffer is configured to provide a sufficiently high intrinsic input capacitance; consequently, relatively large MOS transistors are employed in its input stage. Second, the CCCII is designed to support high-frequency operation by minimizing the dimensions of its constituent MOS transistors. Based on these design requirements, the transistor aspect ratios adopted for the proposed circuits are listed in Table 1.

Table 1. Aspect ratios of transistors.

NMOS	$W(\mu\text{m})/L(\mu\text{m})$
$M_{B1}\text{-}M_{B2}/M_{B3}$	2/0.8, 12/3
$M_1\text{-}M_2, /M_5\text{-}M_6, M_{11}\text{-}M_{12}$	2/0.8, 5/0.8
PMOS	$W(\mu\text{m})/L(\mu\text{m})$
$M_3\text{-}M_4 / M_7\text{-}M_8, /M_9, M_{10}$	10/0.8, 1.5/0.8, 4/0.8

2.1. Multiplier Circuit Implementation

The operating principle of the multiplier sub-block is based on the well-known algebraic identity reported in [15], which is expressed as:

$$(X + Y)^2 - (X - Y)^2 = 4XY \quad (11)$$

To implement this operation, the proposed multiplier employs two translinear loops that perform current-mode squaring functions [15].

As shown in Fig. 3, the first translinear loop, composed of transistors $M_1\text{-}M_4$, generates a current proportional to the $(X+Y)^2$ term, while the second loop, consisting of transistors $M_5\text{-}M_8$, produces the $(X-Y)^2$ component. Based on the trans-linear principle, the output current of the multiplier is expressed as:

$$I_{out} = \frac{I_X I_Y}{I_B} \quad (12)$$

The aspect ratios of the transistors used in the multiplier stage are summarized in Table 2.

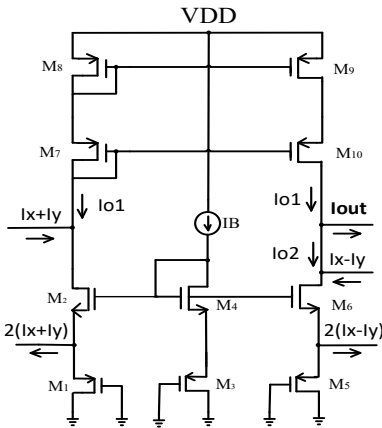


Fig. 3. Transistor-level implementation of the analog multiplier circuit.

Table 2. MOSFET aspect ratios of the analog multiplier.

PMOS	$W(\mu\text{m})/L(\mu\text{m})$
M7-M10	10/0.8
M1-M3 and M5	8/0.8
NMOS	$W(\mu\text{m})/L(\mu\text{m})$
M2-M4 and M6	2.5/0.8

3. Simulation-Based Performance of the Proposed MEC

The functionality of the proposed emulator circuits was confirmed through transistor-level simulations performed in the Cadence environment. All test results were obtained with constant supply voltages of $V_{DD} = 1.25$ V and $V_{SS} = -1.25$ V. The bias currents of CCCII-1 and CCCII-2 were set to $I_{B1} = 100$ μA and $I_{B2} = 100$ μA , respectively. The simulations utilized the 0.18- μm XFAB CMOS process parameters for device modeling. Suitable transistor sizing was selected to assess the complete circuit performance. Fig. 4 shows the charge-voltage pinched hysteresis loops obtained from the proposed MEC at different operating frequencies from 30 MHz to 80 MHz.

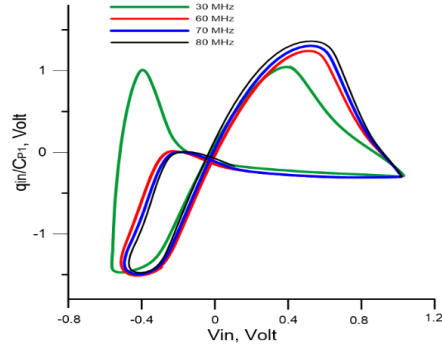


Fig. 4. Charge-voltage hysteresis loops of the proposed MEC at different operating frequencies.

Fig. 5 presents the performance of the proposed design under three different temperature conditions. The results confirm that the circuit preserves its functionality and accuracy even in the presence of considerable thermal variations. The electronic tuning capability of the proposed circuit was investigated by varying the bias current to 60 μA , 80 μA , and 100 μA . The resulting hysteresis characteristics are shown in Fig. 6. Since the memcapacitance of the proposed MEC is influenced by the intrinsic capacitance, its hysteresis behavior was evaluated under different process corners, including TM, WO, WP, WS, and WZ.

As shown in Fig. 7, only slight variations are observed among the process conditions, while the emulator continues to exhibit stable and reliable operation. Furthermore, these variations can be effectively compensated by tuning the electronically adjustable transconductance parameter, G_m .

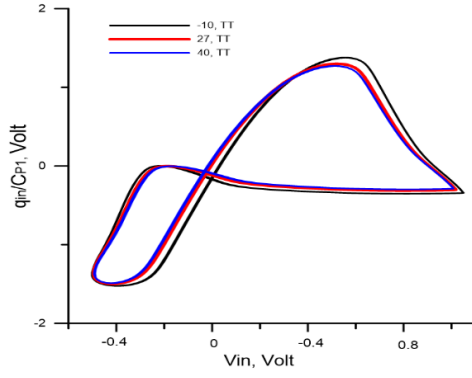


Fig. 5. Memcapacitor behavior under three distinct temperature conditions.

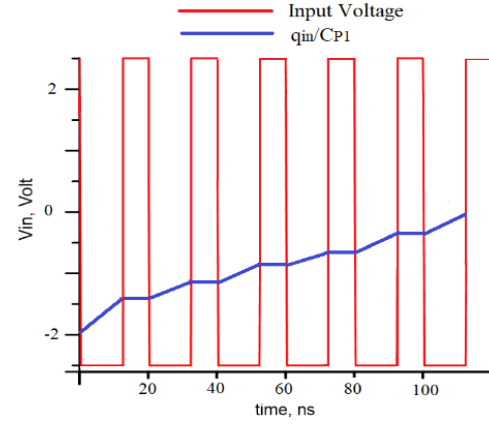


Fig. 8. Non-volatile response of the proposed MEC during incremental operation.

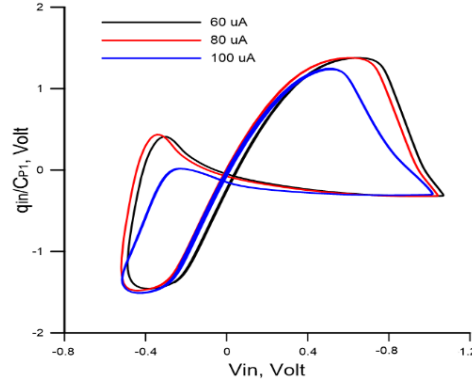


Fig. 6. Pinched hysteresis loops obtained for bias currents of 60 μ A, 80 μ A, and 100 μ A.

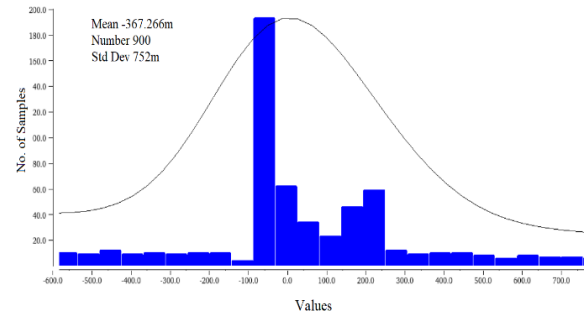


Fig. 9. Monte Carlo analysis of the proposed MEC.

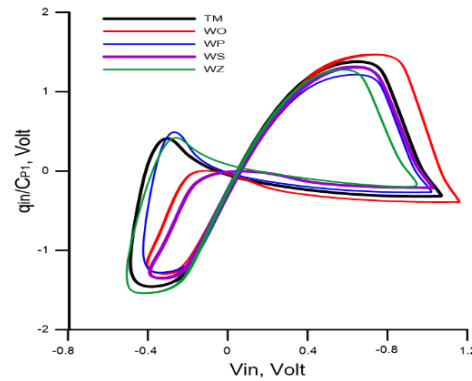


Fig. 7. Pinched hysteresis responses for various process corners.

To verify the non-volatile memory characteristic of the proposed MEC, a voltage pulse train ranging from -2 V to $+2$ V with a 20 ns period was applied, and the response is shown in Fig. 8. In addition, a Monte Carlo analysis was performed to evaluate the robustness of the proposed emulator against process-induced capacitance variations. As illustrated in Fig. 9, the pinched hysteresis characteristics are maintained with only minor deviations, demonstrating that the intrinsic capacitances can be reliably utilized without degrading the memcapacitive behavior.

4. Performance Comparison Between the Proposed MEC and Literature Circuits

Table 3 compares the proposed memcapacitor emulator with previously reported designs. Unlike most earlier implementations, which require one or more passive components such as resistors and capacitors [16-19], the proposed circuit is realized without any passive elements, making it more suitable for monolithic CMOS integration by reducing chip area and eliminating external passive components. Only the recent studies in [8] and [20] also achieve passive-element-free implementations. Compared with [8], the proposed design offers a significantly lower power consumption while maintaining a high operating frequency of 80 MHz. Although the operating frequency is slightly lower than that of [20] (90 MHz), the proposed circuit still operates in the tens-of-megahertz range with a low power consumption of only 0.75 mW. Furthermore, unlike most previous studies, which operate below 1 MHz [16, 17, 19] except for [8, 18], and [20], the proposed emulator achieves high-speed operation while preserving a fully integrated passive-less architecture. These features demonstrate that the proposed design provides an attractive trade-off between integration capability, operating frequency, and power consumption, making it a promising candidate for compact integrated memcapacitive applications.

$$C_M^{-1} = \frac{V_{in}(t)}{q_{in}} = \underbrace{\frac{2\alpha_1(s)\alpha_2(s)}{G_m(s)r_{x2}C_{p2}} I_S \left[\text{Sinh}\left(\frac{q_{in}}{C_{p1}V_T} - 1\right) \right] + \frac{r_{x1}}{q_{in}} I_{in}}_{\text{Ideal Meminductance value}} + \underbrace{\frac{sC_0}{q_{in}G_m(s)} V_{ota} - 2\alpha_1(s) I_S \left[\text{Sinh}\left(\frac{q_{in}}{C_{p1}V_T} - 1\right) \right] - \frac{sC_{z2}}{q_{in}G_m(s)} V_{z2}}_{\text{Non-ideal term}} \quad (20)$$

6. Application of MEC

A memristive logic gate operates based on the voltage division principle, where the applied voltage is distributed according to the states of series-connected memristors. By switching between low (ON) and high (OFF) resistance states, memristors enable binary logic operation. Since memcapacitive devices also exhibit state-dependent capacitance, the same concept can be applied to memcapacitive logic gates. To validate the proposed MEC, a 2-input logic gate was implemented and verified through Cadence simulations.

The truth table of the proposed OR gate is constructed from the possible input combinations of a and b and the corresponding output values of y , as shown in Fig. 11 and described in [22].

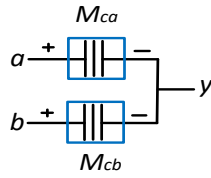


Fig. 11. Memcapacitor-based two-input OR gate.

$$Q_{Mca} = Q_{Mcb}, \quad (21)$$

$$(V_a - V_y) * M_{Ca} = (V_y - V_b) * M_{Cb}, \quad (22)$$

$$V_y = \frac{V_a * M_{Ca} + V_b * M_{Cb}}{M_{Ca} + M_{Cb}}, \quad (23)$$

$$V_a = 0V, V_b = 0V: V_y = 0V, \quad (24)$$

$$V_a = 0V, V_b = 1V: V_y \approx \text{logic } 1, \quad (25)$$

$$V_a = 1V, V_b = 0V: V_y \approx \text{logic } 1, \quad (26)$$

$$V_a = 1V, V_b = 1V: V_y = 1V \quad (27)$$

The simulation results for the proposed OR gate are presented in Fig. 12. These results confirm that the designed circuit operates correctly and produces the expected output.

7. Conclusions

This work presents a novel active-only MEC implemented exclusively with active building blocks, including CCCIs, CCIs, OTAs, voltage buffers, and analog multipliers, without requiring any passive components. The proposed architecture offers a

compact and straightforward design while enabling efficient operation in the high-frequency region. To validate the performance of the proposed emulator, extensive simulation studies are carried out and discussed in Section 3. The obtained results confirm reliable high-frequency operation, which is achieved by exploiting only the intrinsic gate capacitances as the energy-storage elements. Moreover, the equivalent memcapacitance can be adjusted electronically by varying the bias current, providing enhanced tunability for different application requirements. The practicality and versatility of the proposed emulator are further demonstrated through simulation-based implementation of digital logic function, where OR gate operation is successfully verified.

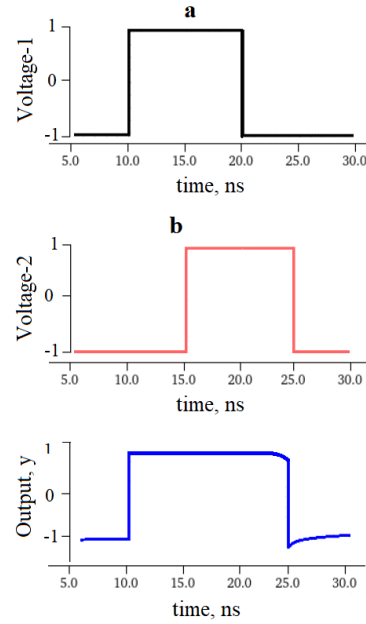


Fig. 12. Simulation results of the proposed OR gate.

Acknowledgements

This work was supported by the ITU BAP within the scope of research project number 46878. We would like to thank project researcher Melike Girgin for her contributions.

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Analysis and Pre-Silicon Verification of an FDC-Based CT Detector IC with Integrated Photodiode

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Summary: High-resolution Computed Tomography (CT) medical imaging demands compact, low-noise readout front-ends capable of managing wide signal dynamic ranges. This work presents a synchronous charge-balancing Frequency-to-Digital Converter (FDC) architecture operating at 100 MHz over an input range of 0–175 nA, implemented at schematic/transistor level in a 0.35 μm CMOS process for pre-silicon simulation. The architecture features an adaptive resolution profile that shows a minimum of 11.96 effective bits under zero-input dark conditions, matching medical contrast requirements while maintaining an ultra-low input-referred charge noise simulated at 0.163 fCrms via Spectre. To enable exhaustive architectural optimization without the prohibitive computational overhead of brute-force Spectre simulations, an efficient top-down verification flow is implemented using a discrete-time, clock-cycle-accurate Python behavioral engine. Co-verified against transistor-level Spectre results at targeted control points, the Python framework estimates main parameters such as resolution, noise and linearity. This numerical prediction serves as an ideal baseline before accounting for transistor-level non-idealities. The methodology demonstrates a 4736-fold computational acceleration per simulation run compared to transistor-level baseline transients, compressing characterization cycles from days to seconds.

Keywords: Frequency-to-digital converter, Charge-balancing loop, CT readout front-end, Adaptive resolution, Behavioral-to-transistor co-validation.

1. Introduction

Next-generation Computed Tomography (CT) demands readout integrated circuits (ICs) combining wide dynamic range and high spatial resolution [1]. Under extreme near-dark conditions (high X-ray attenuation and/or low dose), front-end electronics must exhibit ultra-low noise to preserve clinical contrast [2]. Charge-balancing Frequency-to-Digital Converters (FDCs) offer native adaptive resolution and superior area efficiency, achieving optimal performance in their synchronous loops demands thorough and wide-range characterization. This paper presents a pre-silicon analysis and verification methodology utilizing a discrete-time Python behavioral engine co-verified against transistor-level Spectre results. The proposed flow establishes a significant simulation acceleration to allow for quick early-stage architectural exploration cycles prior to extensive transistor-level simulations.

2. Charge-balancing FDC Architecture and Adaptive Resolution

The continuous-time current digitizer relies on a charge-balancing Frequency-to-Digital Converter (FDC) loop, which provides a strong performance baseline [3] for wide-dynamic-range interfaces without area penalty. As shown in Fig. 1, the operational sequence is governed by the continuous integration of the total input current (I_{in}) onto an

integrating node, where I_{in} is the sum of the generated photodiode current (I_{pd}) and the offset current (I_{offset}), needed to get a minimum frequency above $1/T_{int}$:

$$I_{in} = I_{pd} + I_{offset} \quad (1)$$

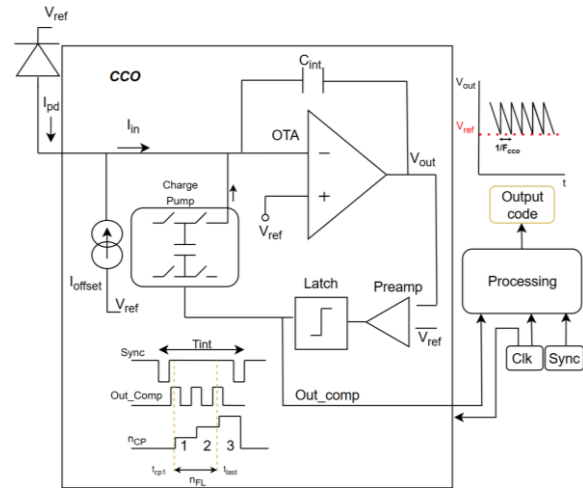


Fig. 1. Architecture of CT detector.

Once the integrator voltage (V_{out}) crosses a predefined threshold, a dynamic comparator triggers a charge pump to inject a reference charge packet (Q_{ref}) that actively discharges the integration capacitor. This self-oscillating process enforces strict charge balance

over an integer number of oscillation periods. The final output code is digitally evaluated in the time domain by tracking the charge pump event count (n_{CP}) and a high-frequency clock counter (n_{FL}):

$$D_{out} = \frac{1}{F'_{cco}} = \frac{n_{FL}}{n_{CP}-1} \quad (2)$$

The denominator uses $n_{CP} - 1$ because it corresponds to the number of sawtooth cycles between first and last charge-pump pulses inside the integration window.

This architectural arrangement features a native adaptive resolution profile that aligns well with CT contrast requirements:

- **High-Signal Regime:** At elevated photodiode currents, rapid loop dynamics maximize clock counter accumulation ($n_{FL} \approx n_{FL,max}$), yielding a peak resolution of 13.25 bits;
- **Near-Dark Regime:** When I_{pd} approaches 0 nA, the loop slows down, reducing the elapsed time captured between feedback pulses, lowering the bit depth.

To analytically formalize this adaptive behavior, the minimum current resolution step (ΔI_{in}) can be derived from the fundamental charge-balancing equations. The average oscillator frequency (F_{cco}) relates to the input current through the charge packet delivered by the charge pump ($Q_{ref} = C_{cp} \cdot V_{ref}$). By tracking two adjacent quantization states, the current resolution step is defined as:

$$\begin{aligned} \Delta I_{in} &= I_{in} - I_{in+1}, \\ \Delta I_{in} &= (C_{cp} \cdot V_{ref} \cdot F'_{cco}) - \\ &\quad - (C_{cp} \cdot V_{ref} \cdot F'_{cco+1}) \end{aligned} \quad (3)$$

Expressing the oscillator periods in terms of the high-frequency reference clock (F_{clk}) and utilizing the baseline loop relationship where $I_{in} = C_{cp} \cdot V_{ref} \cdot F_{clk} \cdot (n'_{CP}/n_{FL})$, equation (3) directly normalizes to the final closed-form expression for the converter's step:

$$\frac{\Delta I_{in}}{I_{in}} = \frac{1}{n_{FL}+1} \quad (4)$$

This formal relationship confirms the physical nature of the adaptive profile. At elevated input currents, the rapid loop dynamics maximize the probability that the initial charge-pump event occurs immediately after the synchronization window opens, while the final event is pushed toward the very edge of the integration window (T_{int}). This phenomenon expands the active time-domain counting window, maximizing n_{FL} and minimizing ΔI_{in} , which compresses the quantization step and elevates the effective resolution to its peak value. Conversely, under near-dark conditions, the reduced event frequency shrinks the effective n_{FL} time window, bounding the resolution to its lower limit. This adaptative resolution is illustrated in Fig. 2 [4].

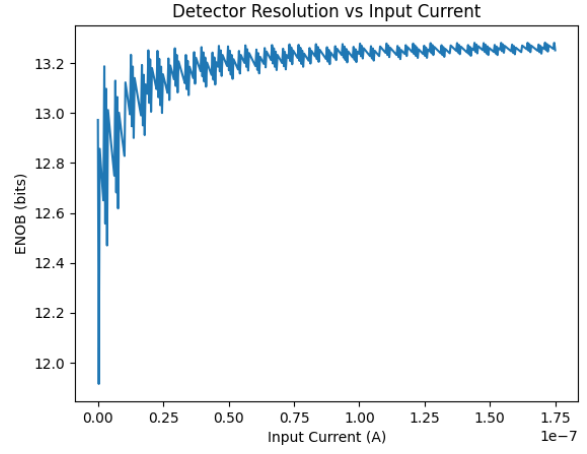


Fig. 2. ENOB vs input Current.

The baseline offset current (I_{offset}) is analytically determined to guarantee system operability under dark conditions ($I_{in} = 0$). In this synchronous charge-balancing loop, a minimum of two feedback events ($n_{CP} = 2$) is strictly required within the integration window (T_{int}) to define a valid time-domain interval (ΔT_{int}), yielding an effective pulse count of $n_{CP} - 1 = 1$. Behavioral Python simulations under zero-input conditions evaluate the clock cycle count separating these initial events at approximately ≈ 4000 clock cycles. Utilizing the baseline FDC current equation:

$$I_{offset} \geq C_{cp} \cdot V_{ref} \cdot F_{clk} \cdot \frac{n'_{CP,min}}{n_{FL}}, \quad (5)$$

with $C_{cp} = 270$ fF, $V_{ref} = 1.25$ V, and $F_{clk} = 100$ MHz, the minimum operating current yields exactly 8.43 nA. Selecting this specific I_{offset} value involves a strict trade-off: conversion failure under dark conditions ($n_{CP} < 2$). Conversely, a higher current unnecessarily shortens the minimum n_{FL} window, which degrades the worst-case resolution below the required 11.96 bits.

To assess the impact of manufacturing tolerances, PVT and Monte Carlo variations are evaluated through (5). The primary variations stem from both the charge-pump capacitance (C) and the current source (I_{offset}), where a typical 10 % process tolerance independently shifts each parameter up to its respective maximum deviation ($I_{offset} = 10.2$ nA would be implemented).

3. Circuit Analysis with Python Model

A custom discrete-time, clock-cycle-accurate Python framework was developed to perform the top-down pre-silicon analysis of the FDC system. To avoid computationally intensive differential equations, the behavioral engine abstracts the continuous-time physical system into a modular, object-oriented model synchronized with the reference clock period ($T_{clk} = 10$ ns).

The simulation execution operates sequentially at each clock edge through the following algorithmic steps:

- **Input Parameter Generation:** The total input current (I_{in}) is defined. Note that the hardware offset (I_{offset}) is generated externally to the core oscillator model, allowing the injection of its specific input-referred current noise profiles before entering the block;
- **Encapsulated CCO Integration:** These combined currents are passed to a dedicated current-controlled oscillator (CCO) behavioral class. Internally, this class updates the integration state variable (V_{out}) and manages the threshold-detection logic within a single time step;
- **Voltage-Domain Noise Injection:** Physical noise contributions from the internal analog blocks (such as the integrator, preamplifier, comparator and charge pump) are directly modeled as voltage-domain variations and injected into the internal state variables during the per-cycle evaluation;
- **Compensation and Raw Event Output:** If an internal threshold crossing is detected, the class internally triggers the charge pump compensation mechanism (Q_{ref}) and outputs a raw comparator event pulse to an external tracking counter;
- **External Post-Processing Windowing:** Outside the CCO block, a global testbench engine generates a synchronization signal (SYNC) that dictates the fixed integration windows (T_{int}). By counting the discrete T_{clk} simulation steps elapsed between the first and the last charge pump event within the active window, the framework externally evaluates the final n_{CP} and n_{FL} counters required for digital code generation.

This efficient algorithmic approach encapsulates the CCO dynamics enables exhaustive dynamic-range characterization and parameter sweeps following the flow shown in Fig. 3. To ensure reproducibility, the parameterized Python behavioral model and complete verification benchmarks are available at https://github.com/Angel-El/FDC_MicDAT2026.

4. Transistor-level CMOS Design and Co-Verification

The core analog blocks – including the current source, continuous-time integrator, preamplifier, dynamic comparator, and charge pump – were implemented at the transistor level using a 0.35 μm CMOS process node (Fig. 4). To validate silicon-accurate performance under device-level noise and non-idealities without the prohibitive computational overhead of full transistor-level simulations, a dedicated noise co-verification flow was established between Spectre and Python [5, 6].

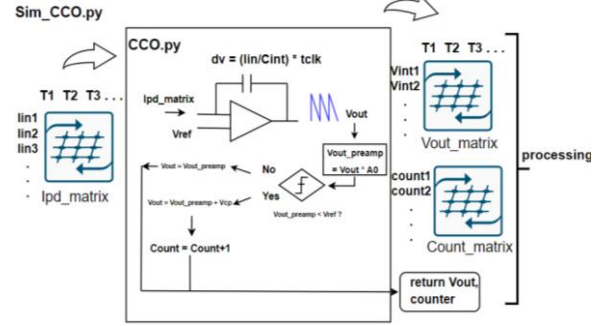


Fig. 3. Block Diagram of CCO Class Operation.

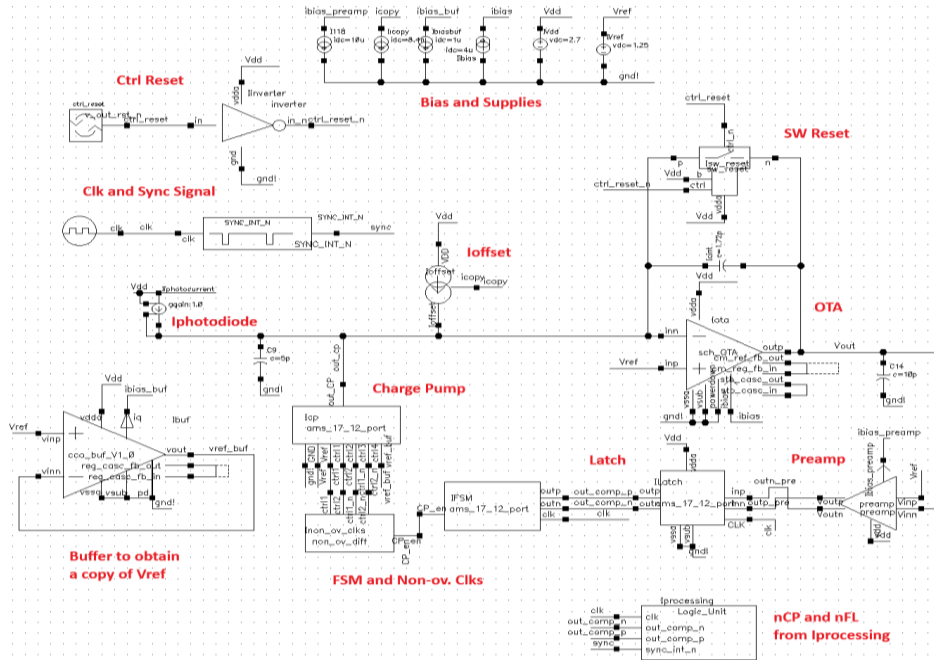


Fig. 4. CT Detector built in Cadence.

The primary technical contribution of this methodology lies in establishing a systematic co-verification framework that bridges both simulation environments, structuring the design phases to maximize simulation throughput. To illustrate this interaction, the complete co-verification workflow is mapped out in the flowchart of Fig. 5. While the initial modeling and co-verification setup requires an upfront development effort, this represents a one-time investment. For medical imaging applications, these behavioral models are highly reusable. In subsequent design iterations, customizing or scaling the framework to new detector specifications requires minimal effort, enabling rapid architectural exploration with a drastically reduced time-to-market.

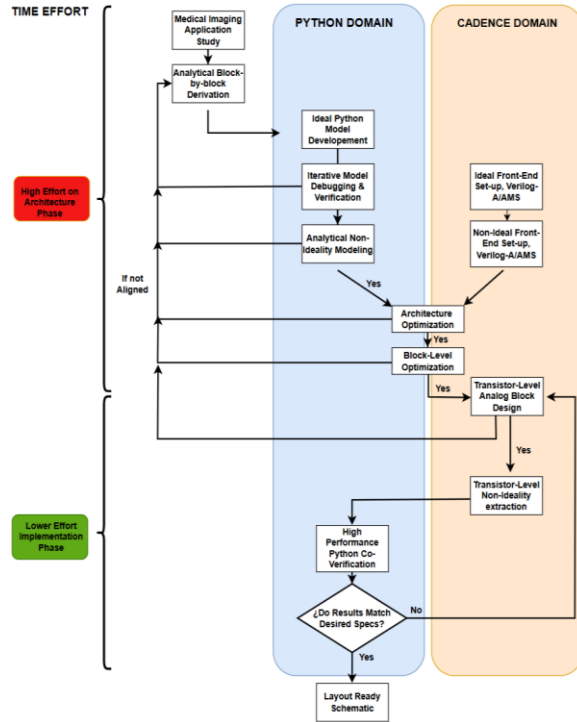


Fig. 5. Used Top-Down Methodology Flowchart.

The abstraction bridge operates as follows:

1. The device-level thermal and flicker ($1/f$) noise contributions of the critical analog blocks are extracted at block level via noise simulations in Spectre;
2. These physical noise profiles are parameterized and mapped into the discrete-time Python engine as stochastic voltage-domain models [7].

To validate the methodology, full-system transient noise simulations were executed in Spectre with device noise enabled. The tight agreement between the extracted transistor-level data and the behavioral Python execution proves the effectiveness of the methodology, confirming that it accurately captures complex multi-block noise interactions while drastically reducing verification time [8].

5. Simulation Results and Framework Co-Verification

To validate the top-down methodology, nominal performance metrics under dark conditions ($I_{pd} = 0$ nA) were compared across the ideal theory, the Python, behavioral framework, and Cadence Spectre simulations. To extract the transistor-level metrics without prohibitive computational overhead, a dedicated Verilog-AMS block within the schematic logs the dynamic comparator's raw digital outputs during the Spectre transient run; these events are subsequently parsed and post-processed via Python to compute the simulated linearity and charge resolution (Q_{res}). As summarized in Table 1, both simulation environments show excellent agreement, yielding an identical minimum charge resolution of ≈ 0.084 fC and closely matching the low intrinsic linearity (49 ppm in Python vs. 82 ppm in Spectre) along with a total dark-current input noise of 0.163 fC_{rms} (Spectre). To further characterize the noise behavior across the full dynamic range, the input-referred charge noise (Q_{in}) was swept using the Python framework, as illustrated in Fig. 6. The resulting distribution shows that with higher input current the effective LSB grows, so noise per LSB – and thus input-referred charge noise – decreases, with the worst case at lowest current.

Table 1. Simulation and Performance Benchmark Comparison.

Metric	Theory	Python	Spectre
Qres (fC/LSB)	0.084	0.089	0.086
INL (ppm FSR)	-	49	82
Total Input Noise (fC _{rms})	0.184	0.181	0.163

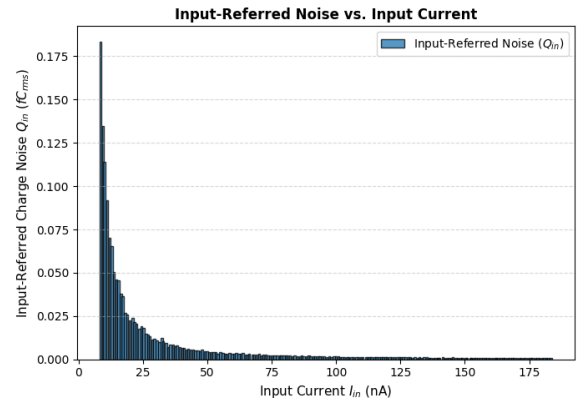


Fig. 6. Noise vs Input Current.

The effectiveness and architectural accuracy of this co-verification framework is demonstrated by these silicon-matching results, capturing complex non-linear quantization beating patterns with an absolute resolution step deviation of less than 4 %. Crucially, while simulating a single current point for a 6 ms integration window requires 1.75 days in Spectre, the

clock-cycle-accurate Python engine completes the execution in just 32 seconds. By delivering a 4736-fold simulation acceleration factor, the proposed methodology successfully compresses multi-point swept verification times from months to minutes, proving to be a highly efficient and robust framework for pre-silicon IC optimization under tight dynamic constraints.

6. Conclusions

A highly efficient top-down verification methodology for CT readouts has been successfully demonstrated, validating the framework proposed in this work. By pairing the custom clock-cycle-accurate Python behavioral engine with transistor-level Spectre simulations, the methodology achieves a massive computational acceleration that compresses early optimization simulation cycles from days to seconds.

This co-verification strategy links high-level loop modeling with device-level noise effects under dark conditions, enabling architectural validation prior to the more expensive Spectre simulations needed for full circuit verification. Decoupling early-stage parameter optimization from technology primitives drastically reduces engineering time to achieve the best architecture within the specifications.

To evaluate the architectural impact of the proposed framework, a direct comparison with the baseline commercial architecture (ams OSRAM AS5952 [9]) is compiled in Table 2. Both designs operate under a fixed integration window and target medical CT imaging using the same 0.35 μm CMOS process node. However, the proposed architecture eliminates the traditional embedded ADC, relying instead on an event-frequency-driven increasing resolution profile. This architectural simplification inherently reduces the silicon area per channel by eliminating a dedicated ADC. Although this approach results in a lower resolution compared to the commercial device, the simulated noise-area trade-off proves highly promising and perfectly sufficient for the target X-ray scanner detector applications. Future work will focus on migrating the proposed architecture to a scaled-down fabrication process node, which is expected to drastically minimize both logic area and power consumption through technology scaling.

Acknowledgements

This work was supported by the UPV–VaSiC Chair (CHIP Chairs Program) and PERTE CHIP PRTR (TSI-0691000-2023-0009), funded by the Spanish Ministry for Digital Transformation and European Union NextGenerationEU. We also thank ams OSRAM/infineon for their technical support.

Table 2. State of the art comparison table.

Parameter	This Work	AS5952 ([9])
Process Node	0.35 μm CMOS	0.35 μm CMOS
Architecture	FDC-Based	ADC-Based
Input Noise	0.163 fC	0.36 fC
Power Consumption/Channel	0.843 mW	1.23 mW

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Optimizing Electrical Conductivity in Amorphous GeSn Thin Films via Thermally Activated Sn Diffusion

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Summary: Amorphous GeSn has emerged as a promising semiconductor material for device-oriented thin-film applications due to its compatibility with low-temperature processing and silicon-based technologies. In this work, amorphous GeSn thin films were synthesized through thermally activated Sn diffusion into PECVD-grown a-Ge:H layers. The electrical conductivity of the resulting films was evaluated as a function of annealing temperature (150–250 °C) and diffusion time (10–30 min). Compared with the as-deposited a-Ge:H films, the annealed samples exhibited conductivities up to three orders of magnitude higher and a clear dependence on the annealing conditions, with the highest values obtained at intermediate temperatures. These results demonstrate an effective low-temperature route for improving the electrical performance of amorphous Ge-based films while maintaining compatibility with temperature-sensitive substrates and large-area fabrication schemes.

Keywords: Amorphous GeSn, Electrical conductivity, Low-temperature processing, Solid-state diffusion, Amorphous semiconductors.

1. Introduction

GeSn has attracted increasing attention as a versatile semiconductor system due to its tunable electronic properties and compatibility with silicon-based technologies [1]. While crystalline GeSn has been widely developed for infrared photonics and Si-based optoelectronic devices, its amorphous counterpart has gained significant interest for applications in thin-film transistors [2]. In this context, amorphous GeSn offers an attractive route for low-temperature processing compatible with silicon-based technology platforms and thermally constrained device fabrication [3]. In a previous work [9], we have discussed the low-temperature formation of GeSn from a-Ge:H and the low-temperature solid-state diffusion of Sn reaching up to 12 % of Sn in the alloy at the temperature range of 150 to 250 °C.

In this contribution, we focus on the resulting enhancement of electrical conductivity upon Sn incorporation into PECVD a-Ge:H, evaluating its dependence over a broad, low-temperature processing window. Window, which is defined by annealing temperature and diffusion time, while enabling fabrication routes compatible with the Si technology and flexible electronics.

2. Methodology

Hydrogenated amorphous germanium (a-Ge:H) thin films were deposited onto SiO₂/Si substrates using a plasma enhanced chemical vapor deposition (PECVD) technique to obtain uniform amorphous layers. Subsequently, a Sn layer was deposited on top

of the a-Ge:H films by e-beam evaporation at room temperature, forming a bilayer structure designed to promote solid-state diffusion.

Thermal diffusion of Sn into the a-Ge:H layer was performed by annealing the samples at temperatures of 150, 175, 200, 225, and 250 °C for 10, 20, and 30 minutes under a N₂ atmosphere to limit oxidation. This process enables the formation of amorphous GeSn alloys through the gradual incorporation of Sn into the Ge matrix, driven by both Sn interdiffusion and the structural relaxation of the initial a-Ge:H network associated with hydrogen redistribution and partial effusion during annealing [4]. Finally, an HCl-based wet etching process was used to selectively remove unreacted surface Sn while preserving the underlying GeSn layer.

The thickness of the prepared samples was determined using profilometry, while the electrical conductivity was measured at room temperature using a four-point probe configuration in order to minimize contact resistance and accurately evaluate the transport properties of the films.

3. Results and Discussion

The evolution of film thickness as a function of annealing temperature and diffusion time is shown in Fig. 1a. All annealed samples exhibit thicknesses in the range of approximately 250–300 nm, with no clear monotonic dependence on temperature. Compared with the initial a-Ge:H layer (~190 nm prior to Sn deposition onto it), the processed films consistently present larger thickness values, because the Sn incorporation during thermal treatment. The absence

of a systematic temperature dependence suggests that multiple competing processes, including structural relaxation of the amorphous network and compositional modifications associated with Sn

diffusion, may contribute to the final film thickness [5]. The corresponding standard deviation values (Fig. 1c) remain relatively low across all processing conditions, suggesting good thickness uniformity.

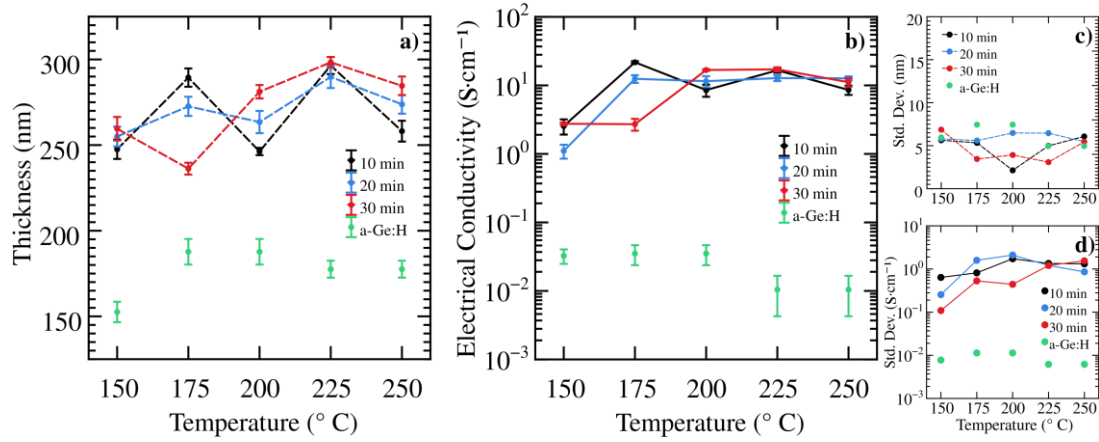


Fig. 1. Physical properties as a function of annealing temperature for 10, 20, and 30 min processing times: a) film thickness, b) room-temperature electrical conductivity on a logarithmic scale, and c, d) their corresponding standard deviation values. Green markers denote independent, unannealed amorphous hydrogenated germanium (a-Ge:H) control films synthesized alongside each experimental batch to account for baseline sample-to-sample variability. Error bars represent the spatial variation across the film surface.

In contrast, the electrical conductivity (Fig. 1b) exhibits a strong dependence on annealing temperature. The as-deposited a-Ge:H films show conductivity values on the order of 10^{-3} – 10^{-2} ($\Omega^{-1}\cdot\text{cm}^{-1}$), whereas all annealed samples display increases of several orders of magnitude, reaching values close to 10^0 – 10^1 ($\Omega^{-1}\cdot\text{cm}^{-1}$). As the annealing temperature increases from 150 °C to approximately 200–225 °C, conductivity rises markedly, suggesting that thermally activated processes associated with Sn diffusion and structural rearrangement enhance electronic transport [5, 6]. This coincides with the tendency reported in [7], where the effect of growth temperature on the formation of $\text{Ge}_{1-x}\text{Sn}_x$ alloy the author reported that with the increase of temperature, Sn atoms occupied the position of Ge atoms forming $\text{Ge}_{1-x}\text{Sn}_x$ alloy, and with the increase of temperature to 240 °C, the Sn doping peak was reached. When the temperature continued to rise, segregation occurred. When the temperature rose to 260 °C, segregation intensified, Sn atoms migrated to the surface of the sample, and the Sn content of $\text{Ge}_{1-x}\text{Sn}_x$ alloy decreased.

At 250 °C, conductivity tends to saturate or slightly decrease regardless of annealing time, revealing the existence of an optimal processing window near 200–225 °C. The conductivity standard deviation values shown in Fig. 1d remain small compared with

the overall conductivity increase, demonstrating good reproducibility across different measurement regions. Overall, the weak dependence on annealing time compared with the pronounced temperature effect indicates that temperature is the primary parameter

governing the electrical evolution of the amorphous GeSn films under the conditions investigated.

4. Conclusions

Amorphous GeSn thin films were successfully synthesized through solid-state diffusion of Sn into a-Ge:H. While the film thickness remains relatively constant across the explored conditions, the electrical conductivity increases by several orders of magnitude with temperature compared to the as-deposited material. An optimal window around 200–225 °C yields the highest conductivity, attributed to enhanced Sn incorporation within the amorphous Ge matrix, whereas higher temperatures lead to a slight saturation or degradation, likely due to Sn segregation and cluster formation.

The weak dependence on diffusion time indicates that Sn redistribution occurs rapidly under the studied conditions as depicted in [8], with temperature acting as the dominant parameter. Overall, these results underline the importance of controlling annealing temperature to optimize electrical performance in amorphous GeSn thin films, highlighting their potential for low-temperature electronic and silicon-compatible device applications.

Acknowledgements

Jael Marisol Carmona-Sánchez gratefully acknowledges the financial support provided by the Secretaría de Ciencia, Humanidades, Tecnología e

Innovación (SECIHTI) and by the German Academic Exchange Service (DAAD, Grant No. 91900144).

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A Low-Voltage Low-Power Oscillator-Based Rectifier for Biomedical Implantable Devices in 0.18 μm Technology

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Summary: Biomedical implantable devices have grown significantly in the last few decades. In these types of systems, it is necessary to receive power from the outside of the body. Inductive powering provides continuous wireless communication between the implant and the external device and also reduces the risk of skin infection and battery leakage compared to wired connections. Rectifiers are commonly used in electrical energy conversion chains to transform the harvested AC power to DC. In this paper, a novel design of a low-voltage low-power Oscillator-Based Rectifier is presented for 0.18 μm CMOS technology. The proposed circuit is able to work as a half- or full-wave rectifier while the LC tank circuit boosts the output DC level. Simulation results show that the proposed rectifier circuit can achieve 89 % Power Conversion Efficiency (PCE) for an AC source of 40.68 MHz with a signal amplitude of 1.8 V (peak). The circuit consumes only 115 μW of DC power and delivers a boosted output voltage of 5.6 V across a 6 k Ω load.

Keywords: Biomedical implantable devices, Inductive powering, Oscillator-based rectifier.

1. Introduction

Biomedical implantable devices have been available for more than sixty years. The first transistorized biomedical implantable device was designed and developed by Earl Bakken in 1957 for the cardiac pacemaker [1]. Since then, providing a robust and continuous power supply has remained a challenge in bioimplantable devices. In many applications, the implant communicates with an external base station via a wireless link. The implant typically sends data to the base station through an inductive-power-link system [2].

The inductive-power-link is composed of two loosely coupled coils. The external coil is usually energized by an oscillator generating a sinusoidal wave [3]. The internal part captures the power through the magnetic field at resonance frequency and converts the AC signal into a constant DC voltage to power up the internal micro-device. However, the power loss of the rectifier circuit on the internal side is one of the major sources that lowers the total efficiency.

Initially, rectifiers were implemented using diode bridges, but since the diode voltage drop is high, they consume significant power and are not suitable for low-voltage circuits [4]. To overcome this problem, several circuit-level rectifiers have been proposed in recent years to increase the efficiency of power supply [5].

In [6], a rectifier bridge was implemented by diode-connected NPN transistors; however, the presence of resistors in these transistors increases substrate leakage currents and reduces the power efficiency. Due to the lower on-resistance (R_{on}) of CMOS transistors compared to bipolar devices, a higher output power can be achieved. But because of

the high turn-off time of input transistors, reverse leakage current causes a decrease in output power [7].

A solution to lower the leakage currents of diode-connected CMOS transistors is using low-threshold-voltage transistors. However, since these types of transistors are fabricated in advanced CMOS processes, they require additional masks and more fabrication steps, resulting in high manufacturing cost [8]. Another method is the use of threshold voltage cancellation techniques. However, in this method, due to the large size of the transistors, the substrate leakage current increases, which in turn reduces power output [8].

Use of comparator-based rectifiers is another approach to suppress the leakage mechanisms. Although comparator-based rectifiers can achieve efficiencies of over 80 %, the design of the comparators plays an important role in their power efficiency, which is not easy to design at high frequencies [8]. As a result, they typically operate at very low frequencies, and to achieve high power efficiency, they require a large input signal or, in some cases, calibration [9].

Bulk-Driven Winner-Take-All (BD-WTA) is an implementation of rectifiers which uses the bulk terminal of the input transistors. The advantages and disadvantages of this method are, respectively, low-voltage and low-power operation, higher input noise compared to gate-driven mode, and reduction of unity-gain frequency due to larger input parasitic capacitance [9].

Recent works have also explored active rectifiers at 40.68 MHz for biomedical WPT [10-12], primarily employing delay-compensated comparators or synchronous control techniques. However, these approaches often require complex control logic or

off-chip components, whereas our oscillator-based topology offers intrinsic voltage boosting and zero voltage drop with minimal circuitry.

While prior comparator-based active rectifiers [10-12] achieve high efficiency, they require precise delay-compensation logic and often operate with input voltages >2 V. Bulk-driven techniques [9] reduce voltage headroom but suffer from lower unity-gain frequency and higher noise. In contrast, the oscillator-based topology inherently provides voltage boosting and zero voltage drop without requiring comparators or complex control. However, previous implementations [2] were limited to lower frequencies and larger technology nodes.

Unlike [13, 14], the proposed circuit incorporates a gating mechanism that decouples the output frequency from the input frequency. This decoupling ensures that the rectifier's performance remains stable against input frequency variations. Additionally, the differential oscillator architecture inherently generates half-wave rectified signals that are combined to produce a full-wave-like DC output. The integrated MOS-resistor averaging network further stabilizes the output voltage across a wide range of load conditions. These architectural innovations collectively provide superior efficiency, voltage boosting, and operational robustness compared to conventional rectifier designs.

This paper is organized as follows. In Section 2, the proposed oscillator-based rectifier is presented. In the proposed circuit, a boosted rectified voltage is provided to the regulator block. Simulation results are shown in Section 3. Finally, conclusions are drawn in Section 4.

2. Proposed Oscillator-Based Rectifier

Fig. 1 shows the proposed rectifier structure. The design of the new rectifier is inspired by the MOS cross-coupled LC oscillators.

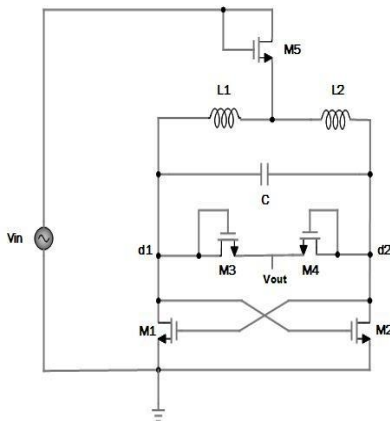


Fig. 1. Proposed rectifier structure.

The induced voltage on the internal part of the inductive-power-link is used as the power supply of the circuit. Depending on the induced input voltage, the

oscillator will switch on and off. Transistors M_1 and M_2 , capacitor C , and inductors L_1 and L_2 constitute a cross-coupled VCO. Inductors (L_1 , L_2) and capacitor (C) determine the output rectified signal frequency, which could be the same as or different from the induced input voltage. The larger the size of the inductors, the greater the current in the circuit, and therefore the DC level of output voltage increases; but since the application of the circuit in implantable devices inside the body is required, the size of the implanted part should be reduced as much as possible. As a result, we need to find a compromise between the size of the inductors and the output voltage level.

The M_5 transistor is a diode-connected NMOS transistor. By applying the input signal to this transistor, the circuit is turned on only during the positive half-cycle of the input signal; during the negative half-cycle, the circuit is turned off. By adding this transistor to the oscillator circuit, the circuit operates as a half-wave rectifier and a half-wave rectified signal is obtained as the output. In addition to rectifying the input signal, due to the presence of an LC tank, voltage amplification also occurs, and the DC voltage level increases. This results in reducing the need for a large AC signal at the input, and the design of the transmitter circuit becomes simpler in the wireless power transmission system. On the other hand, because the circuit is only turned on during the positive half-cycle, power consumption is significantly reduced.

A key operational principle of the proposed rectifier in comparison to structures of [13, 14], is the intentional relationship between the input frequency and the LC tank's resonant frequency. The diode-connected NMOS transistor M_5 is designed to work as a switch which only conduct during the positive half-cycles of the input AC signal. This mechanism ensures that the output frequency is entirely independent of the input frequency, providing exceptional stability of the rectified output against input frequency variations. Moreover, the differential outputs at nodes d_1 and d_2 each produce half-wave rectified signals due to the alternating conduction of M_1 and M_2 . However, because the LC oscillator operates in differential mode, the load effectively sees a full-wave-rectified output. The MOS-resistor averaging network (M_3 and M_4) further smooths the differential half-wave signals, producing a non-regulated DC output that remains relatively constant across a wide load range (4 k Ω to 9 k Ω). This load-independent behavior is a direct consequence of the oscillator's ability to maintain stable oscillation amplitude regardless of output loading, as long as the load remains within the designed range.

3. Simulation Results

The proposed rectifier circuit is simulated in the 0.18 μm CMOS process. The amplitude of the input sinusoidal voltage is 1.8 V and its frequency is 40.68 MHz. Fig. 2 shows the output waveforms of the circuit.

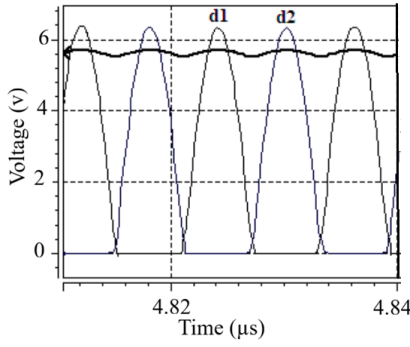


Fig. 2. The output waveforms of Oscillator-Based rectifier.

As shown in Fig. 2, the differential voltages of nodes d_1 and d_2 are half-wave rectified. V_{out} is the non-regulated DC output signal after adding transistors M_3 and M_4 , which each operate as a resistor. Due to the voltage amplification operation in the new rectifier, by applying an input signal with a voltage level of 1.8 V, the voltage level of the output non-regulated DC is about 5.6 V. The output voltage ripple could be suppressed by using a voltage regulator.

The power conversion efficiency (PCE) is defined as:

$$\eta_{RECT} = \frac{P_{DC}}{P_{AC}} \times 100 \% = \frac{V_{out} \times I_{out}}{V_{in,rms} \times I_{in,rms}} \times 100 \%, \quad (1)$$

where P_{DC} is the output DC power delivered to the resistive load R_L , and P_{AC} is the input AC power from the source. All simulations use an ideal sinusoidal voltage source with 50 Ω output impedance to model the inductive coil output. The output load is $R_L = 6 \text{ k}\Omega$ unless otherwise stated. The circuit power consumption of 115 μW refers to the total DC power dissipated by the rectifier core (excluding the load), calculated as $P_{diss} = P_{in} - P_{out}$.

Circuit power consumption is 115 μW and power conversion efficiency is 89 %.

The power conversion efficiency in proportion to the resistive output load change at the 40.68 MHz frequency is shown in Fig. 3. Due to the fact that the circuit is only turned on during the positive half-cycle, it can significantly reduce power consumption and increase output power. As shown in Fig. 3, the output power from a load of 4 $\text{k}\Omega$ to a load of 9 $\text{k}\Omega$ is approximately constant and is more than 85 %, which shows the circuit stability relative to variations in the output load. According to the obtained results, the maximum efficiency is related to the load of 6 $\text{k}\Omega$ and is equal to 89 %.

Fig. 4 shows the rate of efficiency compared to input frequency variations with a resistance of 6 $\text{k}\Omega$.

In Fig. 4, as the frequency increases, the efficiency decreases due to increased power consumption. The highest efficiency at 13 MHz is 94 %.

Given that the target output frequency of the rectified circuit is determined by the LC tank, the circuit output frequency is constant and the input frequency variations do not affect it. Fig. 5 shows the

frequency variation of the circuit output in half-wave relative to the input frequency variation. The output frequency is constant at 100 MHz.

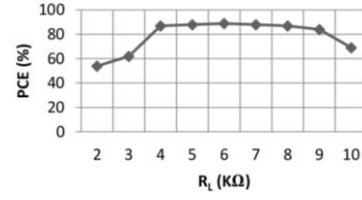


Fig. 3. The efficiency in proportion to the output load.

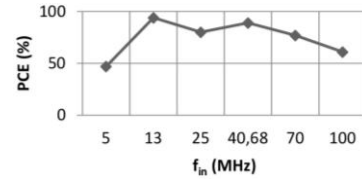


Fig. 4. The efficiency in proportion to input frequency variations.

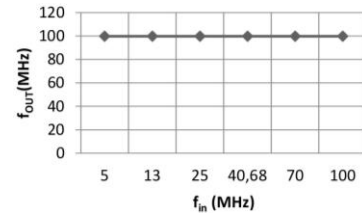


Fig. 5. The frequency variation of the circuit output in half-wave in proportion to input frequency variations.

Table 1 gives a brief comparison of the target rectifier with other structures. According to Table 1, the main drawback of [6] is the high voltage drop. In the new proposed rectifier, in addition to zero voltage drop, the voltage is amplified simultaneously. In [4], to overcome the high voltage drop of the diodes, MOS transistors with low threshold voltage were used, which caused higher substrate leakage current and consequently more power consumption. In the design of the new rectifier, we do not face such challenges.

4. Conclusions

This paper presents a low-voltage low-power oscillator-based rectifier in 0.18 μm CMOS technology for biomedical implantable devices. The proposed circuit operates as a half- or full-wave rectifier while boosting the output DC level using an LC tank. Simulation results achieve 89 % power conversion efficiency at 40.68 MHz with 1.8 V input, delivering 5.6 V output and consuming only 115 μW . Compared to prior works, the design offers zero voltage drop, voltage amplification, and stable

efficiency across load variations, making it suitable for inductive powering in implantable applications.

Table 1. A brief comparison of the target rectifier with other structures.

Ref	Freq	PCE (%)	V _{drop} (V)	R _L (kΩ)	Process
[2]	(4-13.5) MHz	77.78	~ 0.7	-	0.5 μm CMOS
[4]	40.68 MHz	85.8	0.36	8	0.18 μm CMOS
[6]	(1-10) MHz	n/a	2.62	1	BiCMOS
[7]	13.56 MHz	81.9	0.17	1	0.18 μm CMOS
[9]	(1-200) kHz	n/a	0	n/a	0.18 μm CMOS
This work	40.68 MHz	89 %	0	6	0.18 μm CMOS

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A VLC-Based Microelectronic Framework for MARL-Coordinated Multi-Intersection Traffic Control

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Summary: This work introduces a photonics-enabled intelligent traffic management framework that integrates Visible Light Communication (VLC) with Multi-Agent Reinforcement Learning for real-time optimization of urban signal control. LED-based luminaires and traffic signals operate as geo-referenced optical transceivers, creating a distributed VLC layer that supports V2I, I2V, and P2I communication with high spatial resolution and low latency. Vehicles and pedestrians transmit position, velocity, queue states, and crossing requests through optical uplinks, enabling continuous situational awareness across interconnected intersections. On top of this photonic infrastructure, decentralized agents adapt signal phases without predefined cycles, using a queue–request–response mechanism to coordinate structurally critical nodes. The deterministic nature of the optical channel enhances synchronization, allowing cooperative policies that reduce queue lengths, vehicle delays, and pedestrian waiting times. Simulation results show improved throughput and resilience under asymmetric peak-hour flows, demonstrating the potential of photonics-driven sensing and control for next-generation intelligent transportation systems.

Keywords: Visible light communication, Optical wireless communication, Photonic sensing, LED-based communication, Intelligent transportation systems, Multi-agent reinforcement learning, Adaptive traffic signal control, V2X optical communication, Smart cities, Edge computing.

1. Introduction

The convergence of photonics, solid-state lighting devices, and machine learning is enabling new architectures for intelligent sensing and control in Smart Cities. Modern traffic networks require low-latency, high-resolution data acquisition, yet conventional signal control strategies remain limited by reactive operation and coarse sensing modalities. Recent advances in Multi-Agent Reinforcement Learning (MARL) have improved adaptive control, but most implementations assume idealized communication layers and overlook the physical constraints of real infrastructures [1, 2].

Visible Light Communication (VLC), built upon LED-based microelectronic devices, offers a compelling photonic platform by combining illumination, sensing, and optical wireless communication in a single solid-state element. Embedding VLC capabilities into street luminaires and traffic signals transforms urban lighting into a distributed photonic sensing and communication network, enabling deterministic, high-density state propagation [3-5].

This work addresses the gap between photonic device capabilities and learning-based control, proposing a VLC-enhanced MARL framework that couples optical channel characteristics with decentralized decision-making for scalable, next-generation traffic management.

2. Communication and Sensing Model

The proposed framework integrates a VLC-based photonic layer to enable low-latency communication and high-resolution sensing using LED microelectronic devices and PIN-photodiode receivers. Street luminaires operate as geo-referenced optical transmitters, broadcasting synchronization beacons and local traffic-state data, while intersections act as edge-computing nodes processing VLC streams in real time. The system adopts a hybrid Light-to-Vehicle (L2V) and V2I/P2I topology, supporting uplink transmission of position, velocity, queue state, and crossing requests. Downlink I2V/I2P signals close the control loop (see Fig. 1).

The optical physical layer adopted in this work, tetra-chromatic white LED transmitters using OOK modulation and dual PIN photodiodes for wavelength discrimination, follows the hardware architecture and baseline communication protocol previously established in [4] and [5]. Those prior publications defines the emitter–receiver configuration, optical channel model, and frame structure used here as the underlying VLC link. The contributions of this work are distinct, namely: the queue–request–response phase-selection mechanism for decentralized coordination; the integration of SAPA for adaptive priority assignment; in nine intersections and the multimodal MARL-based control evaluation across adjacent intersections. Thus, [4] provides only the

physical-layer foundation, while the control logic, coordination strategy, and performance analysis introduced here are original. Regularly spaced luminaires (20 m) provide deterministic optical coverage, supporting localization, density estimation, and bidirectional interaction. Although VLC is sensitive to weather and illumination, advances in filtering and photodetector sensitivity improve resilience, making VLC a complementary photonic channel to RF systems in intelligent transportation networks.

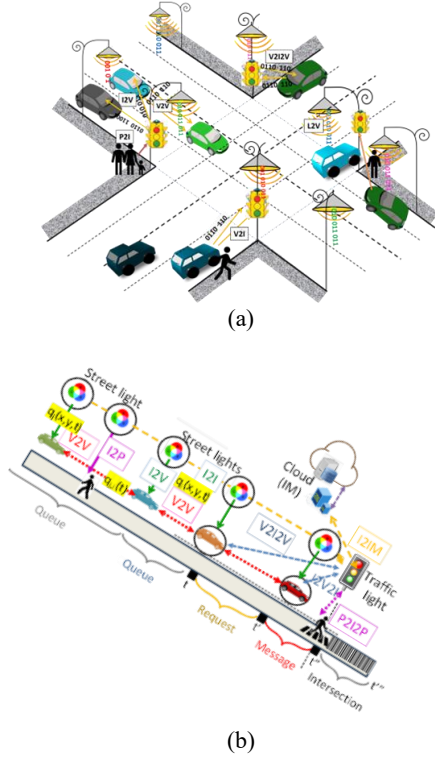


Fig. 1. (a) Overview of visible light communication channels within the intersection area, (b) Draft of the V-VLC architecture.

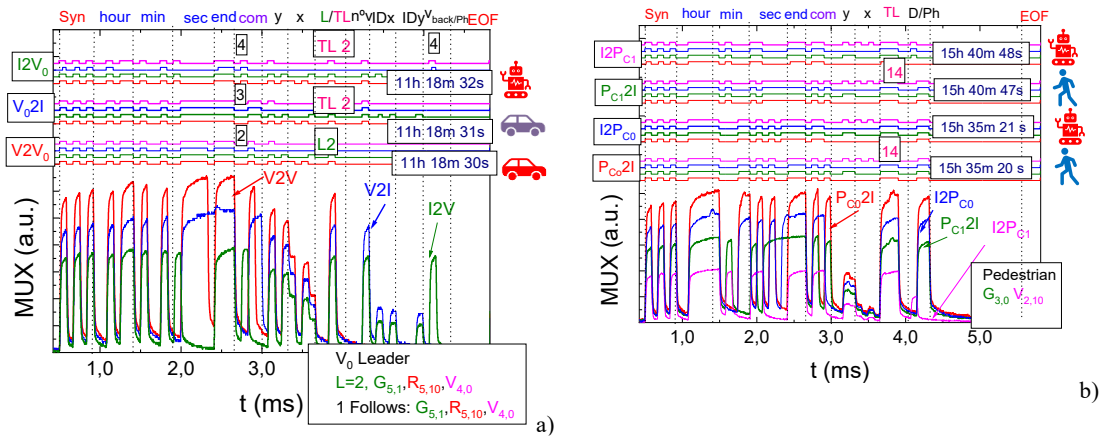


Fig. 2. MUX signal exchange visualization and decoded message flow between: a) Vehicles ↔ Traffic Lights (V2I, I2V) and b) Pedestrians ↔ Traffic Lights (P2I, I2P).

3. Photonic-Enhanced Adaptivity

The proposed VLC-based V2X framework enables optical communication between vehicles, infrastructure, and pedestrians using LED headlights and traffic luminaires as photonic transmitters. Vehicles exchange structured state data through V2V/V2I optical uplinks, while intersections respond via I2V downlinks, completing deterministic multi-hop cycles within 1.2–2.0 s. Individual VLC links exhibit end-to-end latencies in the 3–8 ms range under LOS conditions, supporting the low-latency claim (see Fig. 2).

The optical layer supports real-time V2I, V2V, P2I and I2P exchanges, enabling queue aggregation, phase-aware coordination, and continuous bidirectional data flow. Embedded into luminaires and vehicle lighting, VLC operates as a dual-function platform for illumination and high-resolution sensing.

Integrated with MARL, VLC provides high-frequency state updates that allow agents to optimize signal phases, synchronize adjacent intersections, and incorporate pedestrian requests. Intersections' state propagation prevents spillback by disseminating upstream congestion indicators and downstream availability, enabling coordinated adjustments that preserve flow continuity. The synergy between photonic communication and decentralized learning yields a scalable, congestion-aware, and resilient architecture for next-generation intelligent transportation systems.

4. MARL-Based Traffic Control under Directional Strategies

The traffic network comprises nine four-arm intersections, including two radial corridors and a circular arterial, with C1 and C5 acting as topologically critical nodes (see Fig. 3).

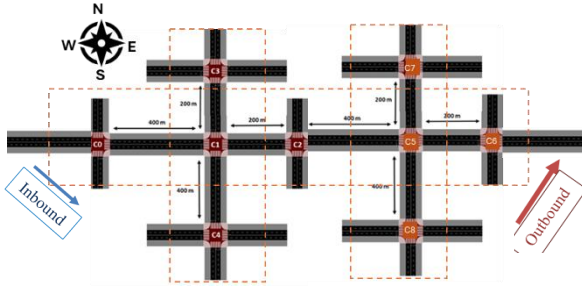


Fig. 3. Traffic scenario including two radial arteries (C3–C4 and C7–C8) and one main circular artery (C0–C6).

A key contribution is the integration of Visible Light Communication (VLC) as a low-latency photonic layer enabling inter-agent coordination and infrastructure-to-user interaction. LED streetlights operate as geo-referenced transmitters, while intersections function as edge-computing nodes processing real-time V2I/P2I optical uplinks carrying position, speed, lane occupancy, and crossing requests. Wavelength-selective filtering and photodiode-based reception ensure robust operation under urban illumination.

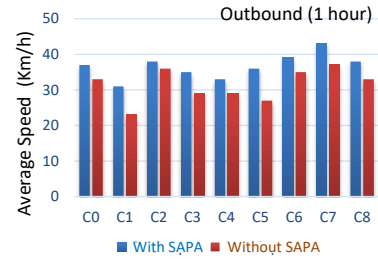
Two directional traffic strategies emulate peak-hour asymmetries – outbound and inbound dominant flows – each trained with DQL and MAPPO controllers (see Fig. 3). VLC-enabled state propagation allows MARL agents to synchronize phase transitions, reducing queues and delays at critical intersections. The photonic layer supports real-time coordination across thousands of vehicles and pedestrians, demonstrating the scalability and effectiveness of VLC-assisted MARL for adaptive urban traffic control.

5. Strategic Anti-Blocking Phase Adjustment

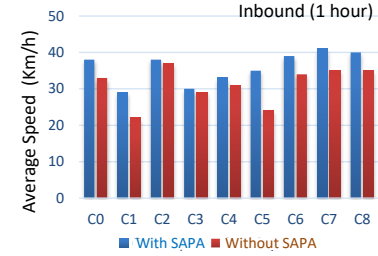
The Strategic Anti-Blocking Phase Adjustment (SAPA) mechanism complements MARL-based control by adapting green durations using VLC-derived queue and occupancy data. Instead of fixed cycles, SAPA adjusts timing according to upstream congestion, downstream lane availability, and the active directional strategy. Green phases are extended when capacity exists and shortened under saturation to prevent spillback, while secondary movements retain fairness weighting.

By integrating real-time VLC sensing with adaptive timing, SAPA improves throughput, mitigates gridlock, and preserves pedestrian safety – particularly at radial–circular junctions. Under both outbound and inbound peak-hour scenarios, SAPA yields higher average speeds and fewer stop-and-go events, as shown in Fig. 4.

The synergy between VLC-enabled state acquisition and MARL-driven decision-making provides decentralized, congestion-aware, and scalable signal control suitable for Smart City deployment.



(a)



(b)

Fig. 4. Evolution of the average vehicle speeds under MAPPO with and without SAPA: (a) Outbound strategy, (b) Inbound strategy,

SAPA consistently yields higher mean speeds, reflecting smoother traffic, reduced stop-and-go events, and better mobility.

Fig. 5 shows that SAPA modifies green-time allocation for Phases 1, 5 and 9. Under outbound demand, SAPA reduces Phase 1 by 4 % at C3 and 17 % at C7, while Phase 5 increases by 11 % at C2. Pedestrian Phase 9 decreases by 7 % at C1, 2 % at C5 and 10 % at C8, reflecting localized, demand-driven adjustments [4]. These targeted reallocations – derived from VLC-based sensing – improve discharge efficiency without compromising multimodal fairness. The results confirm the effectiveness of combining photonic V2X communication with coordinated MAPPO control, demonstrating that VLC-enabled state propagation and cooperative MARL yield adaptive, scalable, and congestion-resilient urban traffic management.

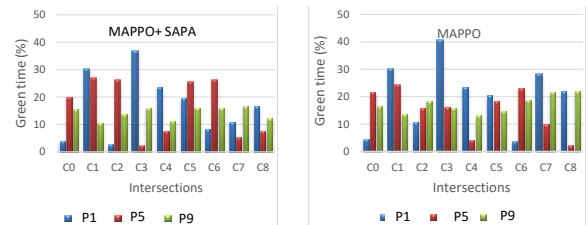


Fig. 5. Percentage of green time allocated to the main signal phases (P1, P5, and P9) with and without the SAPA module.

6. Conclusion and Future Work

This work demonstrates that integrating VLC-based photonic sensing, MARL coordination,

and SAPA adaptive timing provides a scalable and congestion-resilient solution for urban traffic control. VLC enables low-latency, high-resolution detection of vehicles and pedestrians, while MARL supports cooperative decision-making across intersections. SAPA refines phase timing using real-time queue and capacity data, reducing spillback and improving multimodal service.

Simulated results confirm demand-driven optimization: green times are selectively increased or reduced across intersections, queues shorten, stop-and-go events decrease, and average speeds rise.

Overall, the synergy between photonic communication and decentralized learning enhances throughput, fairness, and robustness under asymmetric peak-hour conditions. Future work will extend the framework to network-wide multi-cell coordination, leveraging VLC-enabled state propagation for real-time global optimization.

Acknowledgements

This research received support from FCT – Fundação para a Ciência e a Tecnologia, through the Research Unit CTS – Center of Technology and Systems, with references UID/00066/2025 and by the Fundação Santander Portugal and Instituto Superior de

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Photonics-Enabled Multimodal Traffic Control Using VLC and Multi-Agent Reinforcement Learning (MARL)

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Summary: This work presents a multimodal adaptive urban traffic control framework that integrates artificial intelligence with Visible Light Communication (VLC), leveraging public LED lighting as a high-reliability optical channel for simultaneous illumination and data transmission. By exploiting the deterministic, interference-free nature of VLC, the system delivers real-time signal and road-condition information to vehicles, buses, cyclists, and pedestrians without burdening congested radio-frequency networks. Agents are trained using MAPPO, while DQN is included only as a conceptual baseline for single-agent reinforcement learning, optimizing signal policies based on queue lengths, modal priorities, and cumulative delays. The architecture incorporates dynamic bus-lane allocation, enabling real-time reconfiguration that enhances public transport flow while preserving overall network performance. Pedestrian-aware perception mechanisms further reinforce safety and equitable decision-making. By combining MARL with an optical communication layer, the proposed system advances toward a more efficient, sustainable, and resilient paradigm for next-generation multimodal traffic management.

Keywords: Multimodal urban traffic control, Visible light communication, Photonic traffic control, Multi-agent reinforcement learning, Public transport prioritization.

1. Introduction

Urban mobility in large cities increasingly depends on traffic systems capable of handling multimodal flows involving private vehicles, buses, cyclists, and vulnerable road users. In Lisbon, rising mobility demand intensifies congestion and reduces transport reliability, exposing the limitations of traditional signal control. This context reinforces the need for coordinated, adaptive strategies that support long-term efficiency and safety.

Advances in Artificial Intelligence enable new traffic-management paradigms that optimize intersections in real time while integrating modal priorities [1]. The objective of this research is to enhance multimodal circulation by improving signal performance, reducing delays, and ensuring safer conditions for pedestrians and cyclists. The framework also incorporates dedicated priority mechanisms for public transport, promoting faster and more reliable bus operations across the network. Overall, the work contributes to a more coordinated, adaptive, and sustainable multimodal traffic system for the city of Lisbon. The integration of an optical communication layer distinguishes this approach from traditional RF-based ITS solutions.

2. Intelligent Transport Systems

Intelligent Transport Systems increasingly rely on Connected and Autonomous Vehicles (CAVs) supported by V2X communication to enhance

situational awareness and cooperative driving. Although RF technologies such as DSRC and C-V2X remain widely used, they face congestion and reliability limitations in dense urban environments. Visible Light Communication (VLC) emerges as a complementary optical channel with high bandwidth, security, and suitability for short-range interactions at intersections, benefiting multimodal scenarios involving cars, buses, cyclists, shared mobility, and vulnerable road users [2-4]. Urban mobility also evolves through Multimodal Transit Hubs and predictive models such as MC-GRU, which integrate spatial-temporal traffic patterns to anticipate congestion [5].

VLC-enabled ITS applications – ranging from collision avoidance to cooperative planning – leverage LED infrastructure and photodiode or image-sensor receivers to support precise, low-latency communication. Beyond the foundational aspects of VLC, the research [6] highlights its critical role in enhancing ITS, specifically through a centralized collision avoidance scheme designed for multi-lane roundabouts. Unlike traditional RF communications, which may face signal interference and long transmission delays, VLC offers a reliable alternative with lower complexity and cost-effectiveness for vehicle-to-infrastructure (V2I) coordination. Fig. 1 illustrates the VLC-based urban communication model. As detailed in [7], VLC-enabled traffic control can support coordinated vehicle and pedestrian management through optical V2X links. This prior work provides the underlying communication model adopted here, while the present study extends

it to multimodal scenarios and MARL-based optimization [9].

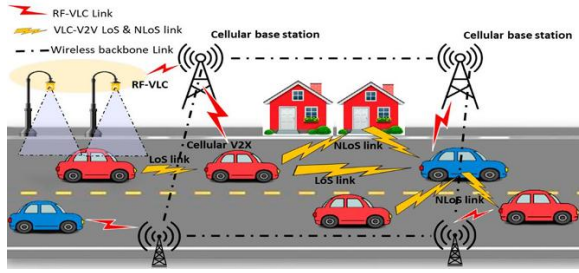


Fig. 1. Urban Traffic using VLC Based Communication. LOS/NLOS VLC propagation paths.

Traditional fixed-time traffic control remains limited, whereas dynamic timing strategies improve throughput, reduce delays, and enhance safety across multimodal networks.

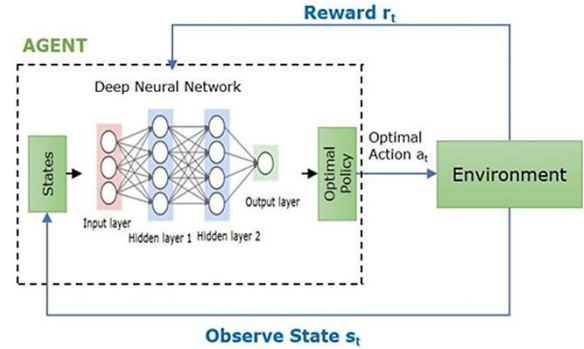
3. Reinforcement Learning

Reinforcement Learning (RL) has become a key approach for adaptive traffic signal control, enabling agents to learn optimal actions through continuous interaction with the environment. In this context, Deep Q-Learning (Fig. 2a) uses neural networks to approximate action-value functions and adjust signal phases based on real-time states such as queues, delays, speeds, and pedestrian presence. Experience replay stabilizes learning by decorrelating sequential traffic data, allowing agents to reduce congestion and improve throughput compared to fixed-time controllers.

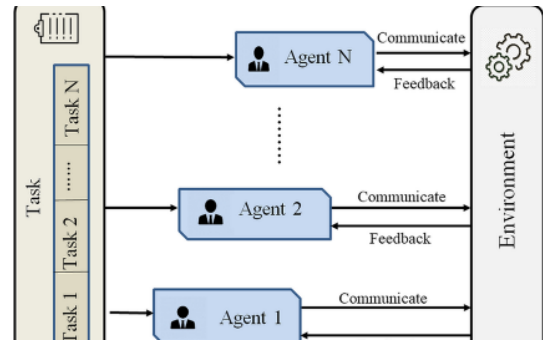
For large networks, Multi-Agent Reinforcement Learning models each intersection as an autonomous agent operating within a shared environment. Algorithms such as MAPPO (Fig. 2b) leverage centralized training with decentralized execution to mitigate non-stationarity and coordinate multiple intersections efficiently. Bounded reward structures and global critics support stable policy updates, enabling scalable, cooperative traffic optimization across multimodal urban networks [7, 8].

Prior work on VLC-enabled traffic control and decentralized multi-agent reinforcement learning, including the studies in [7, 8], those papers, established the foundations for optical communication and MARL-based signal optimization. This work builds upon prior developments in VLC-enabled traffic control, including the arterial-level framework presented in [9], which introduced the foundations of optical V2X coordination. The present paper introduces new contributions: full multimodal integration (cars, buses, cyclists, pedestrians), dynamic bus-lane allocation, pedestrian-aware perception, and a MAPPO-based coordination strategy evaluated on a nine-intersection Lisbon corridor. The results

presented here extend previous work with a comprehensive multimodal analysis and new performance findings.



(a)



(b)

Fig. 2. Draft of (a) Deep Q-learning algorithm, (b) MARL architecture.

Deep Q-Learning is included in this work as a conceptual baseline illustrating single-agent reinforcement learning principles. It is not used in the multimodal experiments. All experimental results reported in this paper were obtained using MAPPO under a centralized-training/decentralized-execution paradigm, which enables stable learning across multiple intersections and supports multimodal coordination.

4. Multimodal-Focused Results

The evaluation demonstrates how multimodal dynamics – buses and regular vehicles sharing the same arterial corridor – shape network performance under MAPPO-based adaptive control. The right-side radial (Fig. 3) acts as the primary multimodal entry route, where buses operate at lower speeds and require larger headways, creating structural constraints that influence agent decisions.

Heatmaps in Fig. 4 show that synchronized inflow of both modes produces a pronounced bottleneck at C1, while downstream intersections maintain fluidity, indicating that agents learn to preserve corridor continuity for public transport.

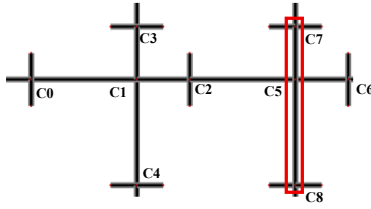


Fig. 3. Traffic Network (9 intersections).

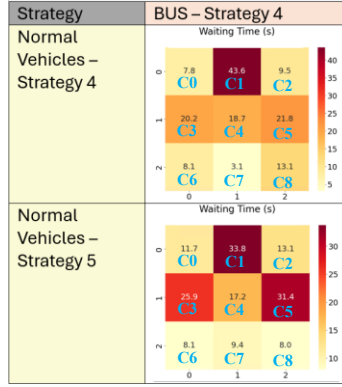


Fig. 4. Waiting Time through intersections.

When inflow and outflow compete, the system prioritizes bus movement, redistributing delays to lateral intersections and revealing a clear multimodal trade-off between bus priority and car throughput. Reward patterns confirm that intersections with heavy bus presence exhibit higher learning difficulty due to conflicting modal objectives.

Fig. 5 shows that increasing car volumes sharply reduce bus median speed until stabilizing near 13 km/h, reinforcing the operational need for dedicated multimodal priority to maintain reliable public transport performance. This behavior may induce the need and a possible advantage for a dedicated BUS priority lane.

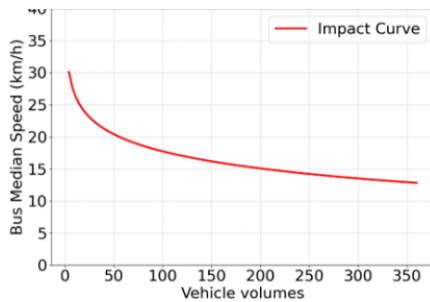


Fig. 5. Normal Vehicles impact on bus speed.

5. Conclusions

This work shows that integrating Visible Light Communication (VLC) with Multi-Agent Reinforcement Learning provides a photonics-driven

foundation for next-generation multimodal traffic control. By exploiting the city's LED lighting grid as an optical communication layer, the system enables deterministic, interference-free data exchange that complements congested RF channels and supports real-time coordination among heterogeneous road users.

The MAPPO-based controller effectively manages multimodal interactions, learning signal policies that preserve public-transport efficiency while balancing private-vehicle flows. Prioritizing the right radial corridor demonstrates the operational value of optical communication, achieving waiting times as low as 3.1 s at critical nodes.

Reward and speed analyses confirm that even under increased photonic-channel load – driven by bus presence and multimodal variability – the agents converge toward stable, efficient policies. Overall, the results validate the role of VLC-enabled, AI-driven traffic systems as a viable path toward safer, more efficient, and sustainable urban mobility grounded in photonic communication. These results highlight the potential of photonics-enabled ITS as a foundational technology for future smart-city infrastructures.

Acknowledgements

This research received support from FCT – Fundação para a Ciência e a Tecnologia, through the Research Unit CTS – Center of Technology and Systems, with references UID/0066/2025 and by the Fundação Santander Portugal and Instituto Superior de Engenharia de Lisboa (ISEL) through the IPEX2025/INUV-LIGHT_ISEL project and 2025.01957.BD grant.

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Investigation of Harmonic Distortion in High Speed SiGe HBT Power Cells at Cryogenic Temperatures

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Summary: The current-voltage characteristics (I-V), small signal S-parameters and harmonic distortion (HD) of high-speed SiGe HBT power cells were experimentally investigated over a temperature (T) range from room down to 4.5 K and for various RF input power (P_{IN}) levels. An industry-standard compact model (CM) was employed to support the analysis and simulation of the measured characteristics at 300 K and partially, at cryogenic temperatures. The cryogenic RF power performance of the SiGe HBTs was analyzed in terms of dynamic terminal currents, diffusion junction capacitances and time-domain voltage and current waveforms. Attention was devoted to carrier-tunneling-related current components and their impact on harmonic distortion and power linearity at cryogenic temperatures. Furthermore, different vector network analyzer probe-tip calibration approaches suitable for cryogenic measurements were evaluated. The experimental and simulation results indicate that the output-power (P_{OUT}) linearity of high-speed SiGe HBT power cells at cryogenic temperatures is strongly influenced by the dynamic current components associated with the base-emitter junction and the substrate. These findings provide further insight into the nonlinear behavior and power performance of SiGe HBTs under cryogenic operating conditions.

Keywords: SiGe HBTs, S-parameters, Harmonic distortion, Power linearity, Transit frequency, Cryogenic temperatures.

1. Introduction

SiGe heterojunction bipolar transistor (HBT) technology is a promising platform for high-speed and high-frequency electronic circuits operating at cryogenic temperatures. SiGe HBT operation has been demonstrated at temperatures down to approximately 70 mK [1-4], while exceptional high-frequency performance has been reported at higher cryogenic temperatures. In particular, the current-gain cut-off frequencies (f_T) exceeding 600 GHz at 45 K [1] and reaching 710 GHz at 4 K [5] have been demonstrated.

The design of the circuits operating at cryogenic temperatures requires accurate compact transistor models, capable of reproducing both the linear and nonlinear behavior of the devices. Conventional compact models, including VBIC and MEXTRAM, describe cryogenic device behavior only to a limited extent [6, 7]. Cryogenic device operation may introduce additional physical effects, including tunneling currents, which have recently been incorporated into a cryogenic implementation of the HICUM compact model [7]. However, this model is not publicly available, limiting its application for independent circuit design and verification. Consequently, the available compact-model descriptions and experimental investigations of SiGe HBT nonlinear behavior remain limited, particularly at deep cryogenic temperatures. Existing model parameter extraction has mainly relied on selected DC and RF characteristics, whereas the mechanisms governing large-signal and harmonic behavior under cryogenic conditions are still insufficiently understood.

Recently, high-frequency stacked SiGe HBT power cells (PwC) with optimized interconnections between individual HBT devices have been proposed for power-amplifier (PA) applications. At room temperature, these power cells have demonstrated promising high-frequency performance, low noise, and good power linearity [8, 9]. For yielding the highest output powers in PA design, it is essential PAs, however, it is essential to understand the generation of nonlinear and harmonic distortion within the power cell and its dependence on bias conditions, input power, frequency, and ambient temperature. Although nonlinear distortion mechanisms and harmonic characteristics of SiGe HBTs have been investigated at room temperature, their behavior at cryogenic temperatures has received little attention. The power characteristics of SiGe HBTs at cryogenic temperatures was investigated in [10]. It was found that power gain increases but output power, power added efficiency and linearity degrade.

This topic is relevant not only from the perspective of fundamental device physics but also for the development of practical cryogenic electronic systems. SiGe HBT technology has been investigated for a variety of cryogenic applications, including low-noise amplifiers for satellite electronics [11], amplifiers for cooled analog-to-digital converters [12], operational amplifiers operating at 4 K [13], transceivers in the 448–491 GHz frequency range [14], and cryogenic readout electronics [15]. As cryogenic electronic systems increasingly incorporate high-frequency and high-power signal-processing functions, understanding and controlling nonlinear distortion become important for achieving the required system-level performance.

The objective of this work is to address the limited understanding of the nonlinear behavior of high speed SiGe HBT power cells under cryogenic operating conditions. We present experimental measurements and analysis of the DC, RF, and large-signal power characteristics of high-frequency SiGe HBT power cells over a cryogenic temperature range, with particular emphasis on harmonic distortion at high frequency. Measurements are complemented by compact-modeling investigations to evaluate the extent to which the observed linear and nonlinear characteristics can be reproduced using available models. The results provide experimental insight into the temperature dependence of harmonic distortion and nonlinear behavior in SiGe HBT power cells and contribute to the development of linear high-frequency power amplifiers for cryogenic applications.

2. DUT and Measurement setup

Investigated devices were SiGe power cells, employing a $2 \times \text{CBE}^2\text{EBC}$ contact configuration. Each device had a drawn emitter area of $A_{E0} = 0.13 \mu\text{m} \times 10.16 \mu\text{m} \times 2$. Further details of the device structure and design are provided in [8, 9]. The measurements were conducted at TU Dresden within the DOT5 research project and, partially, at the ATV Systems LabOne. The devices were fabricated using the IHP SG13G2 BiCMOS technology, which provides seven metal layers for device routing and interconnection [16]. Each SiGe PwC consists of two HBTs connected in parallel and separated by a shallow trench isolation, thereby forming a composite power cell. Following electromagnetic (EM) simulation and optimization, the base and collector terminals of the individual transistors were interconnected and terminated using the second top metal layer of the technology.

On-wafer DC, small-signal RF (0.1–67 GHz), and nonlinear power measurements were performed using a Keysight PNA-X N5247A nonlinear vector network analyzer (NVNA), N6705C source/measure unit (SMU), c. f. Fig. 1. Further details of the measurement setup are provided in [8]. The NVNA calibration, including the phase-reference module, was performed according to the procedure described in the Keysight application note 5989-8575, *Nonlinear Vector Network Analyzer*. Probe-tip calibration was performed and monitored using QAlibria advanced RF calibration software from MPI Corporation. Several calibration approaches, including model-based Short-Open-Load-Thru (SOLT), Thru-Match-Reflection-Reflection (TMRR), and multiline-Thru-Reflection-Line (mTRL), were applied and cross-verified. The stability was verified on a “thru” structure with a “Repeatability” measurement built-in QAlibria software, c. f. Fig. 2.

In addition, the influence of potential probe-tip calibration errors was investigated by emulating calibration uncertainties and evaluating their impact on the measured RF and nonlinear power characteristics. Since the Probe/Substrate model is derived at room

temperature, at low temperatures it loses accuracy and we had to use less model dependent TMRR and self-extracting mTRL VNA calibration methods. Cryogenic measurements were carried out using a Lake Shore TTPX cryogenic probe station, equipped with temperature controller and liquid-helium Dewar, enabling precise control of the Device Under Test (DUT) temperature c. f. Fig. 3.

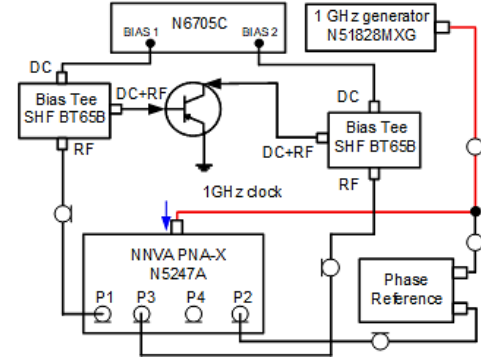


Fig. 1. HD measurement NVNA setup.

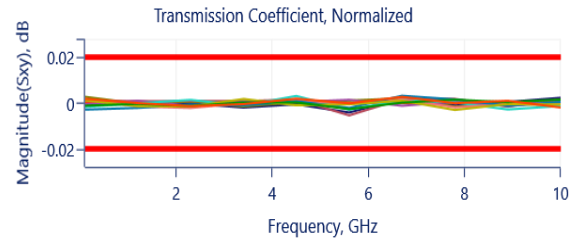


Fig. 2. The mag S.21 repeatability plot of the calibrated VNA and probes on the “thru” calibration standard. (10 frequency points and 6 sweeps, all at 4.5 K).

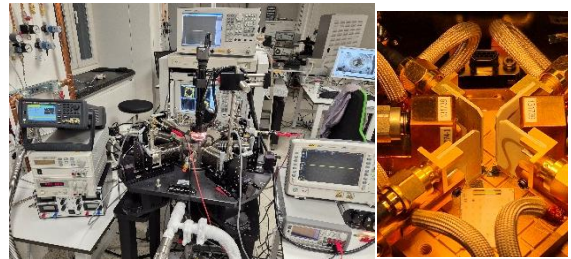


Fig. 3. The photo of TTPX and chuck with the 6 probes (2×RF GSG probes and 4 needle probes for DC bias).

As is seen from the TTPX schematic Fig. 4, even for the cooled down chuck to 4.3 K the probe body in the vacuumed separation is still 30 K. This means that the probe temperature is not well defined and model-based calibration methods like SOLT (derived at room temperature) are not accurate enough for cryogenic temperatures, especially for the high frequency (h. f.) measurements. Therefore, we have selected less model dependent calibration method TMRR and self-extracting mTRL method.

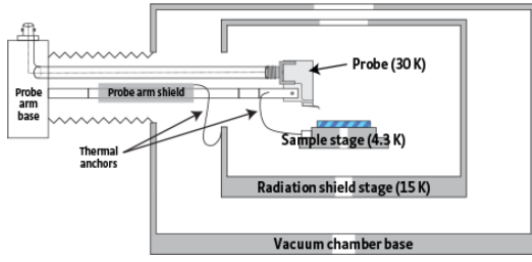


Fig. 4. Schematic of TTPX chamber (www.lakeshore.com). The measured die is located direct on the chuck platen (blue).

3. Results, Analysis and Discussion.

Measured Gummel IV characteristics at different temperatures are given in Fig. 5 base current density $J_B(V_{BE})$ and Fig. 6 collector current density $J_C(V_{BE})$ versus different T . At temperatures from 250 K down to 4.8 K J_B bumps at lower V_{BE} are observed (c. f. Fig. 5), which are related to the contribution of the base recombination current [17, 18] and Early effect related base width modulation [19]. The J_B non-homogeneously increases with V_{BE} [7]. With the T decrease, V_{BE} threshold voltage increases due to band gap temperature dependence [17].

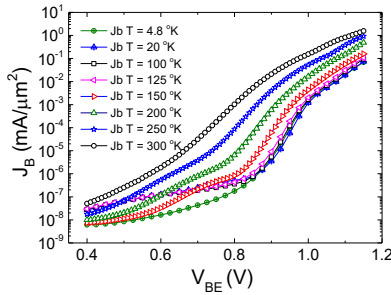


Fig. 5. Measured base current density (J_B) versus V_{BE} of SiGe HBT power cell at different temperatures.

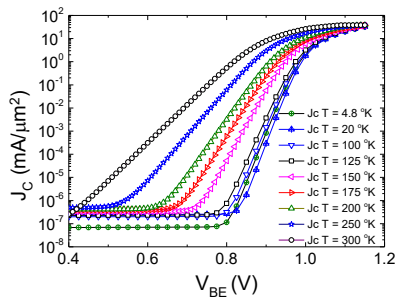


Fig. 6. Measured collector current density (J_C) versus V_{BE} of SiGe HBT power cell at different temperatures.

The dependence on temperature of drift diffusion-controlled collector current and backward emission base current is explained in [7]. The Standard Compact model (for the details see [8]), realized in a

Verilog-A code, was used for simulation with Keysight Advanced Design System simulator. In this work simulations were done at room temperature due to available model limitations to account cryogenic effects like tunneling currents (trap assistant tunneling or direct tunneling from emitter to collector) arising at deep cryogenic temperatures and other effects. In this work the J_B exhibits an additional current component, related to recombination in the base, already below $J_B = 10^{-6}$ mA/μm². As is seen in Fig. 6, the impact on J_C of this additional base current is not visible (J_C homogeneously increases to saturation). Direct and trap assistant tunneling (TAT) currents usually appears in J_C at lower V_{BE} and for the 3rd SiGe generation HBTs are in the range of 10^{-10} A/μm² [18]. In our case the lower current limit was set by the bias-tee down to $J_C = 10^{-7}$ mA/μm². Consequently, it is expected that power linearity of SiGe HBT PwC is not affected by the tunneling currents at $C_{Tyo}T$. The output characteristic of the SiGe HBT PwC at two T shows an increase of J_C at 4.5 K, c. f. Fig. 7 shows very good agreement at 300 K $J_C(V_{CE})$ for both V_{BE} and I_B driven cases [19]. The J_C increase is due to impact ionization and thermal heating, which are also present at $C_{Tyo}T$.

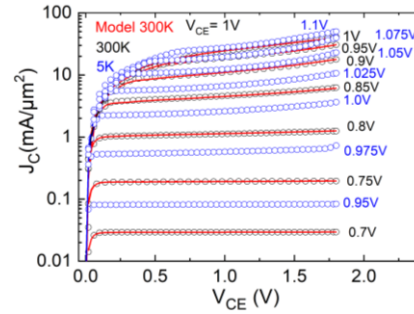


Fig. 7. Collector current density (J_C) over V_{CE} of SiGe HBT power cell with V_{BE} drive at $T = 4.5$ K ($V_{BE} = 0.95$ to 1.1 V, 25 mV step) and 300 K ($V_{BE} = 0.7$ to 1.0 V, 50 mV step). Red lines are CM simulation results.

Measured S-parameters over bias enabled an extraction of the maximum oscillation and current gain cut-off frequency $f_{max}(J_C)$, $f_T(J_C)$ dependences, c. f. Fig. 8, 9. A significant f_T increase at cryogenic temperature is related to reduced carrier scattering and as a result to mobility increase and is less related to diffusion capacitance variation, c. f. Fig. 10. The threshold shift of $C_{BE}(V_{BE})$ towards higher V_{BE} is related to the J_C and J_B threshold shift, c. f. Fig. 5, Fig. 6. An increase of $C_{BE}(V_{BE})$ at 20 K is not visible. The dynamic bias and quiescent $V_{BE} + V_{BED}$ waves are superimposed on $C_{BE}(V_{BE})$ for the harmonic distortion explanation. Incident RF source power is set to 0 dBm at 2 and 10 GHz. Quiescent V_{BE} was swept from 0.6 to 1.1 V. The dynamic waves V_{BED} are onset on $V_{BE} = 1.05$ V bias at 20 K, c. f. Fig. 7. Power wave swings hit an area of diffusion charges, c. f. Fig. 10, so contributing to P_{out} non-linearity. Base/collector junction depletion and diffusion charges as well as

collector/substrate capacitances at different temperatures show the bias dependency beyond $V_{BC} > 0.5$ V, c. f. Fig. 11.

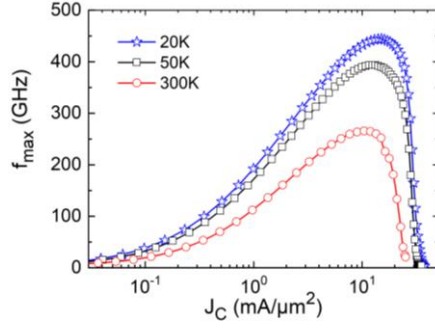


Fig. 8. Maximum oscillation frequency f_{max} of the SiGe HBT PwC over J_C at 300, 100, 50 and 20 K.

Superimposed wave swings of dynamic V_{BC} hit nonlinear C_{BC} and C_{SC} regions, especially at lower frequency. This significantly impacts P_{out} , seen at fundamental frequency and harmonics.

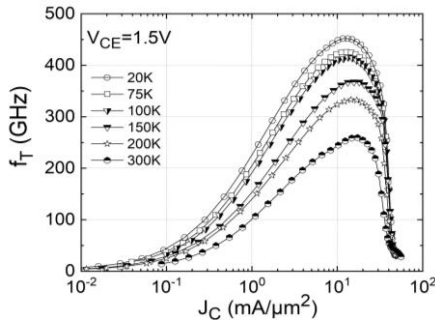


Fig. 9. Measured current gain cut-off frequency f_T of SiGe HBT PwC over J_C at 300, 200, 150, 100, 75 and 20 K.

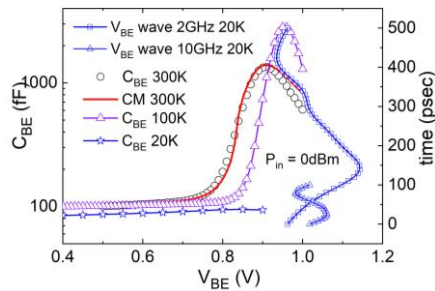


Fig. 10. Base-emitter depletion and diffusion capacitances C_{BE} at different T over V_{BE} . On right axis are dynamic V_{BE} swings in time domain.

Note, that C_{SC} turns to negative values so seen by the system as inductance. Such negative capacitance was already observed and explained in PN diodes [19] and reported for the SiGe HBT PwC [20]. Recently it was shown that the third order intermodulation

distortion IM3 in $A_{III}B_V$ HBT deteriorates with the C_{BC} nonlinearity. Therefore, C_{BC} for linear operation must have possibly low voltage dependence.

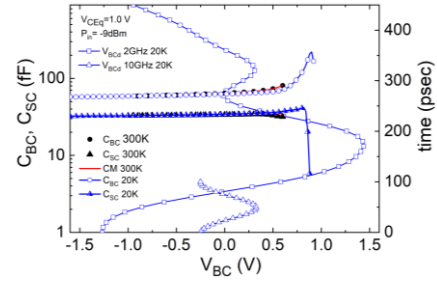


Fig. 11. Base-collector junction depletion and diffusion capacitance C_{BC} and collector substrate C_{SC} capacitance versus V_{BC} at 20 K and 300 K. Red lines (behind the symbols) is CM simulation).

The diffusion capacitance dominates the C_{BE} and shapes the transit frequency f_T . Nevertheless, it was shown that the transit time change from 1.5 psec to 6 psec did not affect IM3 [22]. A negative capacitance effect in semiconductor diodes was explained by relaxation material theory [19], which can also be applied for investigated SiGe HBTs. P_{out} and Transducer Power Gain (G_T) versus P_{IN} at 2 GHz source shows very good agreement with the CM at 300 K, c. f. Fig. 12. Deep analysis of harmonic distortion peculiarities (the drop-out of the 3rd harmonic at fundamental source frequency of 10 GHz (c. f. Fig. 13, Fig. 14) was explained by the base and collector and **substrate dynamic current** dependence on incident power and frequency in [21]. As is seen from Fig. 14, the behavior of the 3rd harmonic remains for all investigated temperatures. At cryogenic temperatures the third harmonic power is reduced at the cost of slightly lower G_T , c. f. Fig. 13 (blue curves compared to red ones) and Fig. 14.

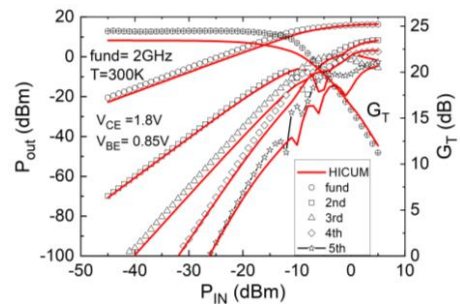


Fig. 12. P_{out} versus input power (P_{IN}) and G_T for SiGe HBT PwC at 300 K with 2 GHz source. Lines: CM [21].

The dynamic V_{CEd} and V_{BED} voltage swings in time domain for different incident source powers at 10 GHz frequency exhibit good agreement with the model even at very high input power +5 dBm, where the wave

distortion is significant, c. f. Fig. 15. Dynamic base and collector bias and current analysis in time domain, c. f. Fig. 15-17 enable deeper insight into the harmonic distortion and device linearity and are used for HD analysis at C_{Tyo} . Compact model simulation enables decomposition and impact of different physical effects in terms of thermal heating, avalanche multiplication, diffusion capacitances, and substrate currents on HD.

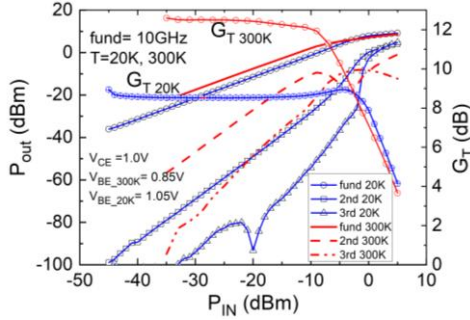


Fig. 13. P_{out} and G_T versus P_{IN} for SiGe HBT PwC at 20 K and 300 K with 10 GHz source. $V_{CE} = 1$ V. Lines: CM.

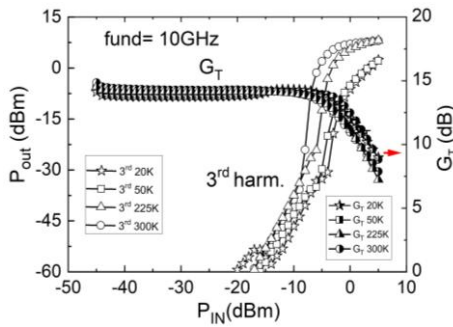


Fig. 14. P_{out} 3rd harmonic and G_T versus P_{IN} of SiGe HBT PwC at 20, 50, 225 and 300 K.

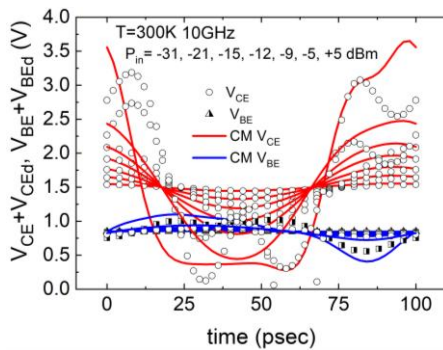


Fig. 15. Dynamic V_{BED} and quiescent base V_{BED} and collector bias V_{CED} waves with different source powers at 10 GHz in time domain at $T = 300$ K. Lines are CM simulation.

The comparison of P_{out} (P_{IN}) of SiGe HBT PwC at different lattice temperatures shows that SiGe HBT PwC at 20 K still exhibits G_T of 9 dB at 10 GHz, an

improved P_{OUT} linearity and lower power of undesired 3rd order harmonic.

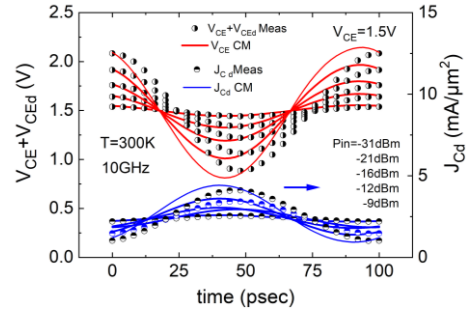


Fig. 16. Dynamic V_{CED} and quiescent V_{CE} collector bias and current density waves with different source powers at 10 GHz in time domain at $T = 300$ K. Lines are CM simulation.

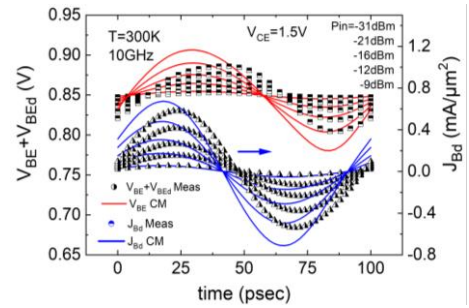


Fig. 17. Dynamic V_{BED} and quiescent V_{BE} base bias and J_{Bd} current density waves with different source powers at 10 GHz time domain at $T = 300$ K. Lines are CM simulation.

4. Conclusions

SiGe HBT Power Cells were investigated in terms of I/V, RF and Power linearity, Harmonic distortion at different cryogenic temperatures. Harmonic distortion and Power linearity analysis was enabled with CM approach and investigation of dynamic base and collector currents as well as diffusion capacitance of emitter/base and base/collector junctions. VNA probe tip calibration and error term correction methods were investigated at different cryogenic temperatures. Harmonic distortion was investigated in terms of the dynamic currents and biases in time domain. The impact of erroneous calibration on RF and Power characteristics was emulated and evaluated. It was found that at low cryogenic temperatures the high speed SiGe HBT power cell can operate with an improved linearity. The observed peculiarity (the 3rd order harmonic drop-out at fundamental frequency of 10 GHz) does not depend on the lattice temperatures at observed temperature range. High frequency SiGe HBT power cells can be used for the power amplifier operating at cryo-temperatures design.

Acknowledgement

ATV Systems and CEDIC TU Dresden are acknowledged for experimental support. BPTI is acknowledged for financial support.

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Visible Light Communication for Intelligent Traffic Control in a V2X Environment

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Summary: This paper proposes an adaptive urban traffic control framework combining Multi-Agent Reinforcement Learning (MARL) with Visible Light Communication (VLC), exploiting public LED infrastructure as a simultaneous illumination and high-reliability data transmission medium. Each signalised intersection operates as an autonomous agent trained via Double Deep Q-Learning (DDQN) and with a Multi-Agent Proximal Policy Optimization (MAPPO), optimising signal timing based on queue lengths and accumulated delays. By coupling cooperative multi-agent learning with an optical communication layer, the proposed system contributes toward a more efficient, sustainable, and resilient paradigm for next-generation urban traffic management.

Keywords: Visible light communication, Photonic traffic control, Multi-agent reinforcement learning, Public transport prioritization.

1. Introduction

Urban mobility is increasingly constrained by persistent traffic congestion, driven by rapid population growth and the continuous rise in vehicle numbers across metropolitan areas, resulting in longer travel times, higher fuel consumption, increased emissions, and reduced overall productivity.

Despite the scale of these challenges, traffic management infrastructure has not evolved at a commensurate pace. Many cities, including Lisbon, continue to rely on rigid, pre-timed signal plans that lack the capacity to respond to real-time traffic conditions or unforeseen disruptions such as demand peaks and incidents. Furthermore, conventional monitoring systems based on fixed sensors suffer from limited spatial coverage, constraining the availability of timely and granular traffic data.

Consequently, traffic control remains largely reactive rather than proactive. Given that urban intersections constitute the primary loci of congestion formation and propagation, there is a compelling need for intelligent, data-driven systems capable of dynamically adapting signal control strategies in response to prevailing real-time conditions.

2. Advances and Challenges in Vehicular Visible Light Communication

For ITS to be effective, large-scale deployment of intelligent vehicles and infrastructure is required to support comprehensive data acquisition and dissemination. Although RF communication has

traditionally underpinned these systems, the rapid growth of mobile data traffic has exposed its spectral limitations [1]. VLC, enabled by advances in LED technology, exploits the vast unlicensed bandwidth of the visible light spectrum and has demonstrated significant potential for vehicular communication within V2V and V2I/I2V frameworks, particularly in dense traffic environments. However, VLC remains susceptible to atmospheric interference, positioning it as a complementary rather than substitutive technology to RF. Recent studies have examined its physical-layer performance under varying environmental and geometric conditions [2], yielding promising yet scenario-dependent results. Despite this progress, the integration of VLC with data-driven control strategies remains largely unexplored. This work addresses that gap by combining VLC-based traffic sensing with reinforcement learning for intelligent and adaptive signal control.

3. Intelligent Urban Traffic Management through Deep Reinforcement Learning

Deep Reinforcement Learning has emerged as a prominent paradigm for adaptive traffic signal control, with research spanning from single-intersection agents to large-scale multi-agent systems. Value-based approaches, particularly Deep Q-Learning, have demonstrated strong performance in this domain. Notable contributions include a DQN-based controller for partially observable intersections with connected vehicles, and a multi-step DQN model that leverages both local and adjacent intersection data to reduce

simulating peak-hour conditions: the morning scenario emphasises inbound flows (C3/C7 → C4/C8), while the afternoon scenario focuses on outbound flows (C4/C8 → C3/C7), enabling assessment of adaptive control under realistic directional traffic imbalances. For each strategy, DDQN and MAPPO agents were trained and evaluated in the SUMO simulator [6]. Their performance was assessed using key traffic metrics, including average queue length (AQL), average waiting time (AWT), average pedestrian halting (APH), and travel time (TT), under a traffic demand of 2600 vehicles and 1000 pedestrians. This study further incorporates the Strategic Anti-Blocking Phase Adjustment (SAPA) module, which refines the green phase durations selected by the RL agent. By dynamically adjusting green times according to upstream queue lengths and downstream occupancy, SAPA prevents spillback, maximises queue clearance, and enhances overall network coordination through adaptive priority weighting across neighbouring intersections.

Table 1. Key Performance Indicators for evening peak hour scenario.

	AQL (vehicles)	APH (ped)	AVS (km/h)	AWT (s)	TT (min)
DDQN-SAPA	6.77	0.99	36.9	8.44	3.58
DDQN	10.83	0.99	32.25	10.15	6
MAPPO-SAPA	9.55	1.29	35.24	7.2	4.87
MAPPO	11.28	0.85	31.76	7.74	5.76
Fixed Control	17.48	5.1	30.9	25.22	6.5

Table 2. Key Performance Indicators for morning peak hour scenario.

	AQL (vehicles)	APH (ped)	AVS (km/h)	AWT (s)	TT (min)
DDQN-SAPA	5.85	1.55	37.51	7.6	3.2
DDQN	10.8	1.94	32.22	9.42	5.88
MAPPO-SAPA	7.39	1.34	36.79	6.99	3.74
MAPPO	14.19	1.59	30.37	11.58	6.45
Fixed Control	16.8	5.1	31.11	24.5	6.35

The evaluated models include DDQN and MAPPO, with and without the SAPA block, across both Radial Out and Radial In strategies. The addition of the SAPA block yielded consistent improvements in both models: DDQN-SAPA reduced queue lengths by 42 %, increased average speed by 15 %, and reduced waiting and travel times by 18 % and 42 %, respectively; MAPPO-SAPA achieved reductions of 32 % in queue length, 16 % increase in average speed, 23 % and 29 % in waiting and travel times. Among the SAPA-enhanced models, DDQN-SAPA outperforms MAPPO-SAPA in terms of vehicle queue length,

average speed, and travel time. However, this improvement comes at the expense of slightly higher pedestrian waiting times. These results demonstrate the trade-off between maximizing vehicular traffic efficiency and maintaining pedestrian service levels, highlighting the importance of adaptive optimization of both signal phase selection and green phase duration.

6. Conclusions

This work presents a MARL-based framework that dynamically optimizes both signal phase selection and green phase duration using real-time traffic information in a fully connected VLC-enabled environment. In the current study, the VLC subsystem and the RL-based traffic control framework were evaluated independently, assuming ideal and instantaneous VLC communication. Results show that the SAPA-enhanced DDQN model outperforms MAPPO, achieving superior vehicular performance while exhibiting a slight increase in pedestrian halting and waiting times. These findings demonstrate the effectiveness and scalability of the proposed framework for complex urban traffic networks. Future work will focus on integrating the laboratory VLC subsystem with the SUMO-RL framework and evaluating the impact of realistic VLC communication conditions, including partial vehicle penetration rates, on traffic control performance.

Acknowledgements

This research received support from FCT–Fundação para a Ciência e a Tecnologia, through the Research Unit CTS–Center of Technology and Systems, with references UID/0066/2025 and by the Fundação Santander Portugal and Instituto Superior de Engenharia de Lisboa (ISEL) through the IPEX2025/INUV-LIGHT_ISEL project and 2025.01957.BD grant.

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Visible Light Communication-Based Traffic Management for Autonomous Guided Vehicles in Automated Warehouses

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Summary: This study proposes an integrated cyber-physical framework fusing Visible Light Communication (VLC) and Multi-Agent Reinforcement Learning (MARL) to resolve the "last-meter" coordination problem for Autonomous Guided Vehicles (AGVs) in Industry 4.0 warehouses. Traditional radio-frequency (RF) systems increasingly suffer from spectrum congestion and electromagnetic interference in high-density intralogistics environments. Our system utilizes ubiquitous LED lighting infrastructure for dual-purpose illumination and intelligent fleet management. By leveraging tetrachromatic LEDs (R, G, B, V), the system establishes four critical V2X communication links (L2V, V2V, V2I, and I2V) to provide high-accuracy localization and real-time state sharing. A Deep Q-Network (DQN) architecture, utilizing a 164-input state vector populated by these VLC links, works in tandem with the Strategic Anti-Blocking Phase Adjustment (SAPA) module to manage traffic dynamically. Simulation results indicate that while traditional fixed-time baselines reach critical congestion at low arrival rates, resulting in a peak accumulation of approximately 70 halting vehicles, the proposed VLC-MARL framework maintains an optimized flow for traffic demands up to 350 AGVs/h. Quantitative simulated comparisons against fixed-time control logic suggest potential reductions of up to 61 % in queue lengths and 59 % in average waiting times. This approach offers a low-cost, scalable, and interference-resilient solution for modern autonomous industrial environments.

Keywords: Visible light communication, Autonomous guided vehicles, Multi-agent reinforcement learning, Intelligent transportation systems, Industry 4.0.

1. Introduction

The ongoing digital transformation of industrial production and logistics has accelerated the deployment of Autonomous Guided Vehicles (AGVs), which have become essential enablers of flexible and efficient intralogistics systems [1]. Since their introduction, AGVs have evolved from simple line-following machines into sophisticated robotic systems integrating advanced sensing and communication capabilities, significantly improving operational efficiency and reducing costs in sectors such as e-commerce and pharmaceuticals.

However, as AGV deployment scales toward high-density fleets, efficient coordination becomes increasingly critical [2]. In modern warehouses, multiple vehicles share narrow aisles and intersections, often leading to congestion and reduced throughput when traditional traffic management strategies are employed. Most contemporary fleets rely on radio-frequency (RF) systems, which are increasingly susceptible to spectrum congestion and electromagnetic interference (EMI) in dense industrial settings. Furthermore, standard control logic, such as fixed-time signaling or First-Come-First-Serve (FCFS), lacks the adaptability required for the stochastic nature of high-density warehouse demand, often leading to systemic gridlock.

To address these challenges, Visible Light Communication (VLC) has emerged as a promising

alternative, leveraging the dense LED lighting infrastructure for dual-purpose illumination and high-speed data transmission [3, 4]. Unlike RF, VLC provides immunity to electromagnetic interference and high spatial resolution for indoor positioning. Recent developments have shifted toward integrating VLC with Deep Reinforcement Learning (DRL) to handle complex vehicle flows [5].

The objective of this work is to investigate the feasibility and performance of an integrated VLC-MARL framework for AGV fleet coordination. This study identifies the "frontier" of warehouse traffic management by accounting for the physical constraints of VLC (such as Line-of-Sight requirements and potential ambient noise) through a robust algorithmic solution for dynamic intersection control, laying the groundwork for future resilience testing against dynamic obstacles.

2. Methodology: Integrated VLC-MARL Model

The proposed methodology for coordinated Autonomous Guided Vehicle (AGV) traffic management is based on a collaborative cyber-physical system that integrates optical wireless communication and distributed artificial intelligence. The workflow consists of microscopic modeling, real-time sensing via Visible Light Communication (VLC), and adaptive

control using Multi-Agent Reinforcement Learning (MARL).

2.1. VLC Physical Layer and Positioning

The physical layer employs tetra-chromatic white LEDs (incorporating 620 nm red, 530 nm green, 470 nm blue, and 405 nm violet emitters) mounted in ceiling luminaires and AGV headlamps [6]. At the receiving end, specialized a-SiC:H/a-Si:H multilayer photodiodes with selective spectral sensitivity are used to record the signals. This hardware enables the filtering of low-frequency noise from ambient light sources through the adjustment of the internal electric field [7]. Fig. 1 depicts the communication architecture.

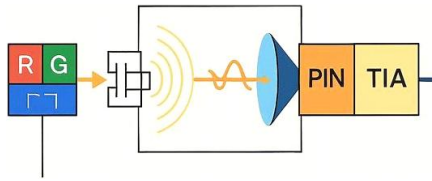


Fig. 1. Overview of visible light communication architecture.

Propagation is characterized using a Lambertian model, where the optical channel gain is determined by the emitter geometry, photodetector area, and incidence angles.

Geo-localization is implemented via the Lamp-to-Vehicle (L2V) channel. The spatial superposition of signals from four LEDs creates a navigation cell composed of nine distinct optical footprints, enabling sub-cell positional resolution. Localization data is transmitted using a 64-bit digital frame that includes the Cell ID, footprint position, and task-specific messages [8].

The framework establishes four critical communication links: L2V for positioning, V2V for state sharing between vehicles, V2I for intersection crossing requests, and I2V for traffic signaling.

The following links constitute the communication backbone:

- Lamp-to-Vehicle (L2V): Provides geo-referenced optical signals for indoor positioning and navigation unit cell identification;
- Vehicle-to-Vehicle (V2V): Facilitates state sharing (position, velocity, maneuvers) between AGVs to enhance local awareness;
- Vehicle-to-Infrastructure (V2I): Enables AGVs to transmit IDs and speeds to intersection controllers for crossing requests;
- Infrastructure-to-Vehicle (I2V): Delivers traffic signaling (green/red phases) and movement authorizations.

To address the limitations of On-Off Keying (OOK) in industrial settings, the receiver employs adaptive thresholding and optical filtering. This mitigates the shot noise and saturation effects inherent in background illumination, ensuring reliable signal recovery.

2.2. Warehouse Traffic Scenario

AGV dynamics are modeled using the Simulation of Urban Mobility (SUMO) platform, adapted for indoor industrial environments [9].

The simulated environment features five intersections (CP0 to CP4) with asymmetric link lengths (400 m and 200 m) to introduce realistic complexity. AGVs operate at a maximum speed of 1.2 m/s (4 km/h), with loading/unloading operations taking approximately 32 seconds (Fig. 2).

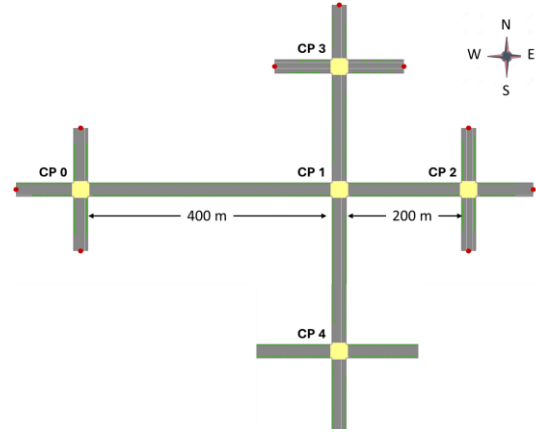


Fig. 2. Layout of the horizontal and vertical axis of the AGVs flow inside the warehouse.

The AGVs in this simulation operate at a maximum speed of 1.2 m/s, which aligns with standard values found in scientific literature and industrial practices for AGVs transporting heavy loads (typically 1.0–1.5 m/s) [10, 11]. While this speed results in traversal times of approximately 167 s and 333 s for the link lengths provided, these dimensions (200 m and 400 m) represent a scaled abstract network rather than a specific warehouse layout. This configuration was intentionally designed to evaluate the framework's robustness and scalability in high-density scenarios. The extended segments allow for the accumulation of significant vehicle fleets and the formation of substantial queues, providing a rigorous environment to test the system's saturation limits, up to 350 AGVs/h, and the effectiveness of the SAPA module in preventing systemic gridlock at critical intersections.

To validate the intelligent model, the framework is benchmarked against a traditional cyclic fixed-time signaling baseline. In this model, primary phases

(North–South and West–East) are static at 40 seconds, while secondary phases last 20 seconds.

2.3. Intelligent Network Architecture

The agents in the proposed framework are inherently cooperative, following the Centralized Training with Decentralized Execution (CTDE) paradigm. Cooperation is achieved through a shared reward function – trained to minimize the global accumulated waiting time across all intersections – and facilitated by real-time state sharing via V2V and V2I links. This ensures that, although each intersection manager operates its own policy, they act towards a common goal of maximizing fleet fluidity.

Each intersection manager is controlled by a neural network that processes a 164-input state vector (covering AGV positions, velocities, and waiting times collected via VLC). The architecture comprises two hidden layers with 400 neurons each, utilizing ReLU activation. For the MARL training and execution, a simplified VLC channel model was implemented to balance physical realism with computational efficiency. Rather than simulating bit-level transmission errors for every state update, the model abstracts the communication layer by conditioning data availability on the geometric overlap between the AGVs and the VLC footprints. This ensures that agents only receive state updates (position, velocity, and waiting times) when within a valid coverage zone, thereby preserving the spatial constraints and intermittent nature of VLC links without the prohibitive overhead of a full physical-layer simulation during the reinforcement learning process.

The agents are trained to minimize the accumulated total waiting time of AGVs in queues, promoting maximum traffic fluidity.

The Strategic Anti-Blocking Phase Adjustment (SAPA) module dynamically refines the green-light durations (between 8 s and 40 s) selected by the DQN. By evaluating downstream lane occupancy, SAPA restricts green phases if the next segment is congested (e.g., occupancy >40 %), preventing congestion spillback and systemic gridlock.

3. Simulation Results and Quantitative Analysis

3.1. Performance Comparison against Baselines

In simulated comparisons against traditional fixed-time control methods, the VLC-MARL framework demonstrated superior stability, achieving a 61 % reduction in queue lengths and a 59 % reduction in average waiting times. The proposed system significantly extended the operational ceiling; while the traditional baseline reached its failure point at an accumulation of 70 halting vehicles, the VLC-MARL framework sustained an optimized regime up to an

arrival rate of 350 AGVs/h. Fig. 3 displays the AGV status at the critical crossing point (CP1) under low, medium, and high demand scenarios.

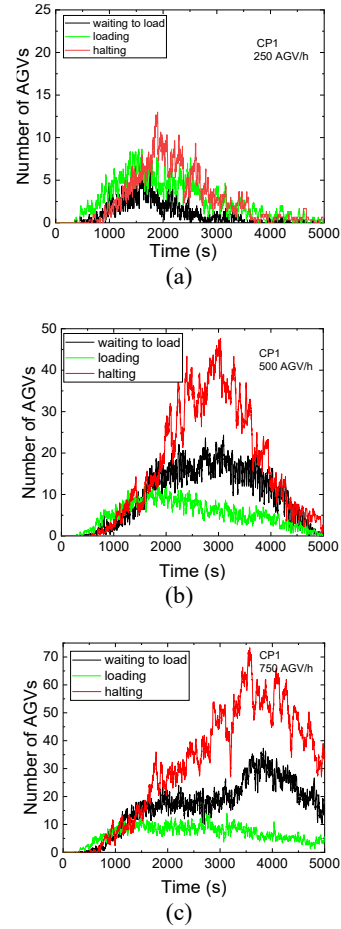


Fig. 3. Number of AGVs waiting to load, loading and halting at the crossing point CP1 with: (a) low, (b) medium, and (c) high AGV scenario.

3.2. Saturation Limits and Scalability

Simulation results confirm that the system maintains an optimized fluid regime up to a flow of 350 AGVs/h. The system transitions into a saturation regime between 400 and 450 AGVs/h. Technical analysis identifies the central intersection (CP1) as the critical bottleneck. As a shared crossing point for both horizontal and vertical axes, CP1 represents a point where arrival rates eventually exceed the physical service capacity of the infrastructure, causing the MARL agent to shift from flow optimization to congestion mitigation.

3.3. Training Efficiency

Reward analysis shows that agents progressively reduce penalties across training episodes. CP1 was identified as the most complex control point due to its higher operational demand and length, requiring more

episodes to stabilize the decision policy compared to peripheral intersections.

4. Conclusion and Future Work

The proposed framework demonstrates the feasibility of using warehouse lighting for joint localization and adaptive traffic control. By combining VLC-based state sharing with distributed MARL, it reduces communication bottlenecks caused by RF interference and limited wireless bandwidth while remaining scalable to large industrial environments. Future work will explore explicit inter-agent negotiation protocols and asynchronous communication strategies to further enhance resilience to dynamic Line-of-Sight blockage caused by mobile obstacles and complex stochastic noise profiles, building upon the footprint-based connectivity model established in this study.

Acknowledgements

This work was funded by FCT (CTS UID/0066/2025; grant 2025.01957.BD) and by Fundação Santander Portugal and ISEL (IPEX2025/INUV-LIGHT_ISEL).

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Effect of Ambient Conditions on Hydrogen Response of Graphene-Based Chemiresistor

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Summary: Graphene-based gas sensors offer room-temperature operation due to their high surface area and lower electrical conductivity, unlike conventional metal oxide sensors that require high power for elevated temperatures (~350 °C). However, pristine graphene exhibits weak interaction with gas molecules, necessitating functionalization or doping to enhance both sensor response (%) and selectivity. Metal doped graphene demonstrates significantly improved hydrogen sensing performance. Despite these advantages, ambient temperature and humidity strongly influence their performance, causing significant changes in response. This study investigates the effects of environmental conditions on the hydrogen sensing behaviour of graphene-based chemiresistive sensors; highlighting the need for ambient compensation to ensure reliable performance in real-world application.

Keywords: Chemiresistor, Graphene, Hydrogen sensor, Humidity, Temperature.

1. Introduction

Hydrogen sensors have potential applications across a wide range of fields, including energy and fuel systems, industrial processes, aerospace, defense, power generation, transportation, medical sectors, and environmental monitoring [1-4]. Although hydrogen offers significant advantages as a clean and efficient energy carrier, its use is associated with certain limitations, particularly its high flammability and risk of explosions [5, 6]. Hydrogen gas has an exceptionally wide flammability range of approximately 4 % to 75 % in air and requires very low ignition energy, making it highly prone to accidental ignition [7]. Furthermore, hydrogen is colorless, odorless, and tasteless, rendering it undetectable by human senses. Therefore, continuous monitoring using hydrogen sensors is essential to ensure safety and prevent incidents [8].

A wide range of materials have been explored for the development of hydrogen sensors, including metal oxide nanostructures, conducting polymers, carbon nanotubes, graphene, and hybrid materials formed by combining these components [9-12]. Among these, metal oxide semiconductors and Pt-based pellistors are commonly employed as active materials in resistive and catalytic hydrogen sensors due to their high sensitivity and rapid response times. However, a significant limitation of these materials is their requirement for high operating temperatures (300-550 °C), leading to increased power consumption [13]. One of the key considerations for practical hydrogen sensing applications is the ability to operate effectively at low temperatures, as this is crucial for

minimizing the risk of ignition and ensuring safe operation.

In recent years, graphene-based gas sensors have demonstrated remarkable performance in the detection of harmful and toxic gases at room temperature, exhibiting very high sensitivity [14-16]. This exceptional sensitivity is primarily attributed to graphene's ultra-high surface-to-volume ratio and its excellent physisorption properties. Numerous studies have reported the high sensitivity of pristine graphene-based gas sensors. However, despite this advantage, graphene sensors suffer from poor selectivity, because they tend to respond similarly to a wide range of gases, making it difficult to distinguish between different gas species. Additionally, environmental factors such as temperature and humidity can significantly influence sensor performance [17, 18], leading to poor accuracy. Therefore, it is essential to functionalize or dope the graphene surface with suitable additives to enhance both sensitivity and selectivity [19, 20], while also gaining a deeper understanding of the sensor response under varying environmental conditions. B. Alfano *et al.* investigated the influence of dry and humid environments on the sensor response and long-term stability of the sensing material [21]. Our earlier study demonstrated the room-temperature hydrogen sensing behavior of Pd-doped graphene at various hydrogen concentrations [22]. As an extension of this work, the present investigation focuses on a comparative and quantitative assessment of pristine and Pd-doped graphene for hydrogen detection across a wide concentration range. In addition, the effects of temperature and relative humidity on sensor response are comprehensively evaluated to gain deeper insight

into the role of environmental conditions in determining sensing performance.

2. Experimental Details

2.1. Sensor Fabrication

Graphene devices were fabricated by Paragraf Ltd using proprietary direct-deposition techniques on a metal oxide substrate. The graphene was patterned into a channel approximately 94 μm wide, with electrical contacts formed through passivated metal tracks. Individual dies were mounted onto custom-designed printed circuit boards (PCBs) and electrically connected using epoxy-coated wire bonds (Fig. 1). For hydrogen sensing studies, both pristine and Pd-loaded graphene chemiresistors were evaluated. Palladium was deposited by e-beam evaporation at a rate of 1 $\text{\AA}/\text{s}$ to a thickness of 1 nm, enabling a direct comparison of the sensing performance of pristine and Pd-functionalized devices.



Fig. 1. Photograph of the Pd-doped graphene chemiresistor mounted on a carrier printed circuit board (PCB), used for gas-sensing response analysis.

2.2. Gas Sensor Measurements

The graphene sensors were evaluated in a custom-built gas sensing chamber, where a constant current was applied across the source-drain channel and the corresponding resistance was monitored. The automated gas testing system, controlled through a National Instruments (NI) LabVIEW program, allowed simultaneous testing of up to eight devices. Gas concentrations, flow rates, and humidity levels were precisely regulated via LabVIEW. The sensor signals were conditioned and recorded using an NI USB-6343 Data Acquisition System (DAQ), which was used to determine key electrical parameters, including resistance and current.

3. Results and Discussion

3.1. Effect of H_2 Concentration

The sensing performance of both pristine and Pd decorated graphene was investigated over a hydrogen concentration range of 0.025 to 1 % at room temperature. Fig. 2a shows the dynamic response, showing the variation in sensor resistance upon exposure to different H_2 concentrations.

The results indicate that pristine graphene exhibits no response across the entire concentration range, whereas the Pd decorated graphene shows a pronounced and well-defined response. The exposure time for hydrogen was fixed at 5 minutes for each concentration. The sensor response % (SR) was calculated using the following expression:

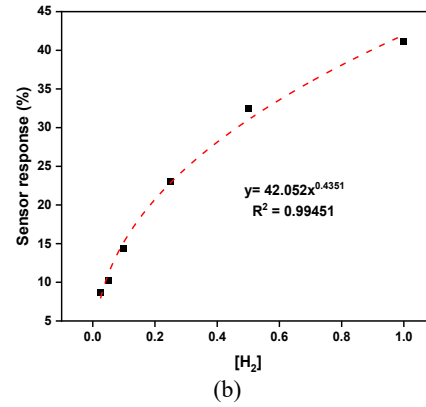
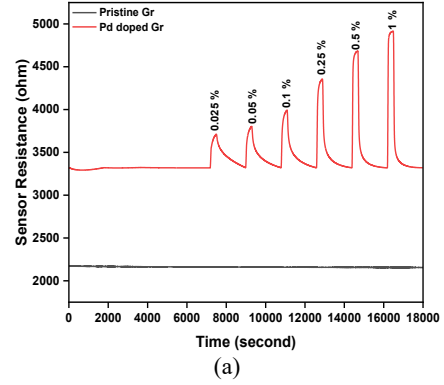


Fig. 2. (a) Time-dependent resistance profiles of pristine and Pd-decorated graphene sensors under different hydrogen concentrations; (b) plot of sensor response (%) versus hydrogen concentration at room temperature.

$$SR (\%) = \left[\frac{R_g - R_a}{R_a} \right] \times 100, \quad (1)$$

where R_a is the resistance value measured in air and R_g is the resistance measured in the presence of H_2 .

As observed in Fig. 2b, the resistance of the Pd decorated graphene increases non-linearly with increase in hydrogen concentration indicating p-type semiconducting behavior.

3.2. Effect of Humidity and Temperature

To evaluate the effect of temperature on hydrogen sensing, Pd-doped graphene sensors were tested at room temperature, 50 $^{\circ}\text{C}$, and 75 $^{\circ}\text{C}$. As shown in Fig. 3a, the sensor response (SR) increased with hydrogen concentration at all temperatures and improved with increasing temperature, reaching the highest value at 75 $^{\circ}\text{C}$.

The influence of humidity was examined using humid hydrogen mixtures. Fig. 3b shows that increasing relative humidity (%RH) causes a slight change in resistance, indicating that humidity affects the sensing behavior of the Pd-doped graphene sensor.

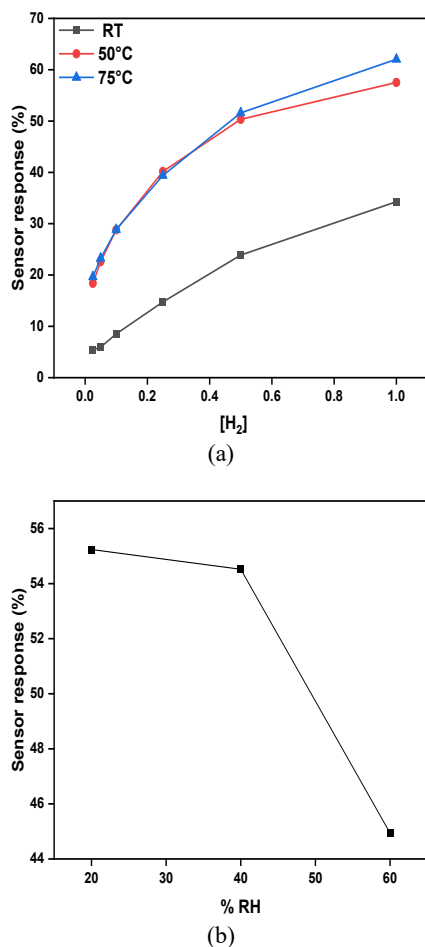


Fig. 3. (a) SR of Pd-doped graphene against different concentrations of H₂ measured at room temperature (RT), 50 °C, and 75 °C. (b) SR values at 0.5 % H₂ under different % RH levels.

At higher humidity levels, sensor response decreases and becomes slower due to water molecules adsorbing on the graphene surface. These molecules compete with hydrogen for active sites on Pd nanoparticles and graphene, reducing hydrogen adsorption and charge transfer.

Moisture also alters surface conductivity by forming a thin water layer that affects electron transport. Nevertheless, the sensor maintains a stable and detectable response under all humidity conditions, highlighting its suitability for practical applications.

4. Conclusions

This study highlights the substantial influence of temperature and humidity on the response of a doped

graphene chemiresistor. Increased humidity was found to reduce and slow the sensor response while increase in temperature modulates SR. Despite these effects, Pd-doped graphene maintains stable and detectable responses at sub-4 % (lower explosive limit) concentrations needed for the detection of hydrogen gas leaks.

Acknowledgements

This research was supported by the Engineering and Physical Sciences Research Council grant EP/W024284/1.

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FPGA Implementation of Zonotopic Estimation for Linear Systems: Algorithmic Structure and Hardware-Oriented Design

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Summary: In exact arithmetic, zonotopic set-membership estimation provides guaranteed state enclosures for linear systems with unknown-but-bounded disturbances, but repeated dense linear-algebra operations and generator growth limit embedded real-time deployment. This work presents an SoC-FPGA implementation on the AMD Kria KR260 in which prediction, sequential strip-based correction, and bounded-order reduction are mapped to a unified Vitis HLS accelerator, while the ARM Cortex-A53 processing system handles control and data movement. IEEE 754 single-precision arithmetic and a fixed generator budget provide deterministic storage and execution. On a 24-state, 12-measurement, 200-step benchmark, three correction strategies are evaluated. At a common 110 MHz clock, FPGA batch latency ranges from 2.8709 to 5.2371 ms, providing up to 15.15 $\times$ speedup over Python and 4.93 $\times$ over C++. The Volume strategy also achieves the lowest estimated energy, 9.96 mJ per batch, and a best board-validated latency of 1.5443 ms under frequency scaling.

Keywords: FPGA acceleration, Zonotopic state estimation, Set-membership estimation, SoC-FPGA, High-level synthesis.

1. Introduction

In exact arithmetic, set-membership estimation propagates sets that are guaranteed to contain the true state when disturbances and measurement errors are described by bounds rather than probability distributions. Zonotopes are attractive for this purpose because their centre-generator representation is closed under linear maps and Minkowski sums, while bounded measurements can be incorporated through strip intersections [1, 2]. The resulting recursion, however, repeatedly applies matrix-vector products, matrix-matrix products, dot products, rank-one updates and generator reduction. Sequential measurement updates also append generators, causing both arithmetic cost and memory use to grow unless the zonotope order is actively controlled.

The underlying set-estimation framework is well established. Early zonotopic state-bounding observers demonstrated how bounded process and measurement uncertainties can be propagated without assuming complete probability distributions [5], while subsequent work developed guaranteed zonotopic state-estimation formulations and systematic measurement-update procedures [1, 2]. Zonotope-order reduction is also a standard mechanism for controlling the growth of generator matrices while retaining an outer approximation [4].

From the implementation perspective, high-level synthesis provides a systematic path from algorithmic descriptions to FPGA datapaths, but its effectiveness depends strongly on kernel structure, memory organisation, and scheduling [3]. FPGA acceleration has also been demonstrated for other computationally

intensive numerical and optimisation workloads, including real-time optimisation algorithms [6] and dynamic neural-network solvers [7]. These studies motivate the hardware-oriented decomposition adopted here, where repeated matrix-vector, matrix-matrix, rank-one update, and reduction operations are exposed explicitly to programmable logic.

This work investigates a hardware-oriented implementation of this established estimator rather than proposing a new estimation method. The contribution is the decomposition of prediction, strip correction and reduction into regular FPGA kernels; their integration into a Vitis HLS accelerator on the AMD Kria KR260 SoC-FPGA; and an experimental evaluation covering latency, resource utilisation, post-route power and frequency headroom. The same estimator structure is implemented in Python, C++ and programmable logic to enable direct cross-platform comparison.

2. Estimator and Hardware Mapping

For a linear system $x_{k+1} = A_k x_k + B_k u_k + w_k$, $y_k = C_k x_k + v_k$, the state set is represented by the zonotope $X_k = p_k \oplus H_k [-1, 1]^m$. Prediction propagates the centre and generators as

$$\tilde{p} = A_k p_k + B_k u_k + p_k^w, \tilde{H} = [A_k H_k H_k^w] \quad (1)$$

Each scalar measurement defines a strip $|C^T x - y| \leq \phi$. Its intersection with the predicted set is outer-approximated by

$$\hat{p} = \tilde{p} + \lambda(y - c^T \tilde{p}), \hat{H} = [(I - \lambda c^T) \tilde{H} \phi \lambda], \quad (2)$$

In exact arithmetic, this construction encloses the zonotope–strip intersection for any λ [1, 2]. The three implemented gain rules are made explicit as

$$\lambda_{\text{fix}} = c, \quad (3)$$

$$\lambda_{\text{seg}} = \frac{HH^T c}{c^T HH^T c + \phi^2}, \quad (4)$$

$$\lambda_{\text{vol}} = \frac{\|c^T H\|_2^2}{\|c\|_2^2 (\|c^T H\|_2^2 + \phi^2)} c, \quad (5)$$

where H denotes the generator matrix entering the current strip update. Segment reduces the extent along the measurement direction, whereas Volume uses a volume-related surrogate [1, 2]. Small denominator guards of 10^{-12} are applied when required. These closed-form rules expose a hardware-friendly sequence of dot products, AXPY operations, row-times-matrix products, rank-one updates and column appends. Because every strip update introduces a generator, bounded-order reduction is applied using a fixed budget s . Following the standard Girard-style zonotope reduction family [1, 4], generator columns are ranked by squared Euclidean norm; the largest $s - n$ are retained and the discarded contribution is enclosed by an n -column diagonal row-sum block. Omitting the square root preserves the ranking while avoiding an unnecessary hardware operation. Reduction is conditionally performed after prediction and obligatorily after all measurement updates, ensuring bounded storage before the next time step.

More explicitly, if H_{disc} denotes the discarded generator columns, their contribution is enclosed by the diagonal row-sum matrix

$$d_i = \sum_j |(H_{\text{disc}})_{ij}|, H_{\text{box}} = \text{diag}(d) \quad (6)$$

Since n generator slots are required for this diagonal enclosure, only $s - n$ original generators are retained. For the present configuration, $n = 24$ and $s = 32$, so the eight highest-ranked original generators are retained and the remaining contribution is represented by 24 diagonal generators. Generator ranking is implemented using the squared Euclidean norm

$$q_j = \sum_{i=1}^n H_{ij}^2, \quad (7)$$

with deterministic selection of the largest scores. The square root is not evaluated because it does not change the ordering of the generators.

Two reduction points are used within each estimation step. An early reduction is conditionally applied after prediction when the predicted generator count exceeds s , while a final reduction is always applied after the complete sequence of n_y measurement updates. This keeps the generator count bounded before the next prediction and provides fixed upper bounds on array storage and loop execution.

The complete recursion is encapsulated in one AXI-connected HLS kernel. The ARM Cortex-A53 processing system prepares data, launches one accelerator invocation for the full batch and manages memory transfers, while the programmable logic executes the arithmetic kernels. All variants use IEEE 754 single-precision floating point, maximum generator storage $m_{\text{max}} = 64$, and reduction budget $s = 32$. The floating-point implementation follows the exact-arithmetic recursion but does not use directed outward rounding; therefore, a formal machine-level enclosure guarantee under IEEE 754 arithmetic is not claimed here. The implementation is instead assessed for cross-platform numerical consistency and hardware performance. The common comparison point is 110 MHz. This partition follows the general HLS approach of exposing regular computational kernels to deeply pipelined FPGA datapaths [3]. The complete PS/PL execution flow is shown in Fig. 1.

Target Platform and Design Configuration

The accelerator is implemented on the AMD Kria K26 SoM (Zynq UltraScale+ MPSoC) using Vitis HLS 2025.2. Fixed-gain, Segment, and Volume are generated under the same initial 110 MHz HLS target clock to provide a common implementation constraint for comparison. The configuration uses state dimension $n = 24$, measurement dimension $n_y = 12$, batch length $N = 200$, maximum generator storage $m_{\text{max}} = 64$, and reduction budget $s = 32$.

The three correction strategies are implemented as separate accelerator variants while sharing the same top-level HLS kernel structure, memory-interface layout, numeric representation, and runtime execution flow. Their principal architectural difference is therefore the hardware required to compute the correction vector λ .

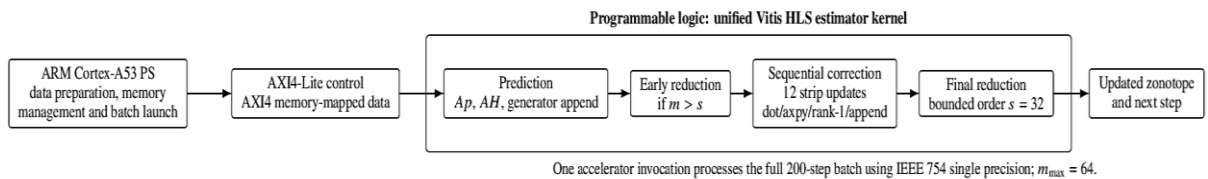


Fig. 1. SoC-FPGA mapping and kernel-level execution flow of the zonotopic estimator.

Kernel Decomposition

The dominant computational kernels are prediction, sequential correction, and bounded-order reduction. Prediction requires a matrix–vector product for the centre and a matrix–matrix product for the active generator matrix. Each measurement-strip update requires a centre projection, correction-vector computation, a row-times-matrix operation, a rank-one update, and the appending of one measurement generator. Reduction then scores generator columns, selects the largest retained generators, and aggregates the discarded contribution into a diagonal row-sum enclosure. These kernels dominate the arithmetic cost of each estimation step. Their computational workload depends primarily on the state dimension n , active generator count m , number of measurement channels n_y , and reduction budget s . Prediction is dominated by matrix–vector and matrix–matrix products, while sequential correction grows with both the active generator count and the number of measurement strips. Reduction combines generator-wise scoring and row-sum aggregation with a top- s selection stage. Consequently, bounding m is important not only for memory allocation but also for maintaining predictable execution complexity.

These operations are integrated into the top-level HLS kernel `zonotope_batch_kernel_axi`. A single invocation processes all 200 estimation steps, thereby reducing host-side invocation overhead and keeping the dominant arithmetic workload inside programmable logic.

End-to-End Estimator Flow

Algorithm 1 summarises the complete estimator recursion and the principal kernels executed in programmable logic.

Algorithm 1 Hardware-oriented zonotopic estimator

Require: $p, H, A, C, \{y_k\}, H^w, \{\phi_i\}, s$

```

1: for  $k = 1$  to  $N$  do
2:    $\tilde{p} \leftarrow Ap + p^w$ 
3:    $\tilde{H} \leftarrow [AH \ H^w]$ 
4:   if  $m > s$  then
5:      $\tilde{H} \leftarrow \text{Reduce}(\tilde{H}, s)$ 
6:   end if
7:   for  $i = 1$  to  $n_y$  do
8:      $c \leftarrow C_{i,:}$ 
9:     compute  $\lambda$  using Fixed, Segment, or Volume
10:     $r \leftarrow y_{k,i} - c^T \tilde{p}$ 
11:     $\tilde{p} \leftarrow \tilde{p} + \lambda r$ 
12:     $t^T \leftarrow c^T \tilde{H}$ 
13:     $\tilde{H} \leftarrow \tilde{H} - \lambda t^T$ 
14:     $\tilde{H} \leftarrow [\tilde{H} \ \phi_i \lambda]$ 
15:   end for
16:    $H \leftarrow \text{Reduce}(\tilde{H}, s)$ 
17:    $p \leftarrow \tilde{p}$ 
18: end for

```

3. Experimental Results

Benchmark System

The experiments use a 24-state linear system composed of six identical four-state damped-oscillator blocks. The state-transition matrix is

$$A = \text{blkdiag}(A_{\text{osc}}, A_{\text{osc}}, A_{\text{osc}}, A_{\text{osc}}, A_{\text{osc}}, A_{\text{osc}}), \quad (8)$$

where

$$A_{\text{osc}} = \begin{bmatrix} c & -s_\omega & 0.1 & 0 \\ s_\omega & c & 0 & 0.1 \\ -0.1 & 0 & c & -s_\omega \\ 0 & -0.1 & s_\omega & c \end{bmatrix}, \quad (9)$$

with

$$c = e^{-\zeta\Delta t} \cos(\omega\Delta t), s_\omega = e^{-\zeta\Delta t} \sin(\omega\Delta t) \quad (10)$$

The parameters are $\omega = 0.5$ rad/s, $\zeta = 0.05$, and $\Delta t = 0.1$ s. The control input is zero, with $B = 0 \in \mathbb{R}^{24 \times 1}$. The measurement matrix selects the first two states of each oscillator block:

$$C = I_6 \otimes \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} \in \mathbb{R}^{12 \times 24}, \quad (11)$$

so that each subsystem is only partially measured and the remaining state components must be reconstructed through the system dynamics and zonotopic correction. The process and measurement generator matrices are $H^w = 0.05I_{24}$ and $H^v = 0.1I_{12}$, respectively, and the initial set is centred at $x_0 = [1, 0, \dots, 0]^T$ with $H_0 = 0.2I_{24}$. A fixed random seed generates the common 200-step input bundle used by all implementations. Python 3.12.3/NumPy 1.26.4 and native C++ compiled with g++ 13.3.0 -O2 run under Ubuntu 24.04.3 on WSL2 on an AMD Ryzen 9 7945HX host. Their timing covers the estimator batch only and excludes synthetic true-state propagation and measurement generation. Each FPGA latency is the mean of runs 2–20 from 20 consecutive on-board executions, with run 1 excluded as a cold-start execution.

Table 1. Common experimental configuration.

Parameter	Symbol	Value
State dimension	n	24
Measurements	n_y	12
Sampling interval	Δt	0.1 s
Natural frequency	ω	0.5 rad/s
Damping ratio	ζ	0.05
Batch length	N	200
Process-noise radius	r_w	0.05
Measurement-noise radius	r_v	0.1
Initial radius	r_0	0.2
Reduction budget	s	32
Maximum generators	m_{max}	64
Common PL clock	f_{PL}	110 MHz

The qualitative estimation behaviour is illustrated in Fig. 2, where the estimated centre follows the true-state trajectory while the zonotopic enclosure represents the bounded state uncertainty over the 200-step workload.

For the Segment strategy, the Python, C++, and SoC-board implementations exhibit closely matching temporal behaviour, as shown in Fig. 3.

A separate implementation-level comparison of the software and HLS C-simulation outputs gives maximum centre differences of 2.12×10^{-6} for Python–C++, 2.30×10^{-6} for Python–HLS, and 1.79×10^{-6} for C++–HLS over the complete 200-step workload. The centre-error traces are used as a behavioural comparison rather than as evidence of bit-exact equivalence, because floating-point operation ordering and hardware scheduling differ across the software and FPGA implementations.

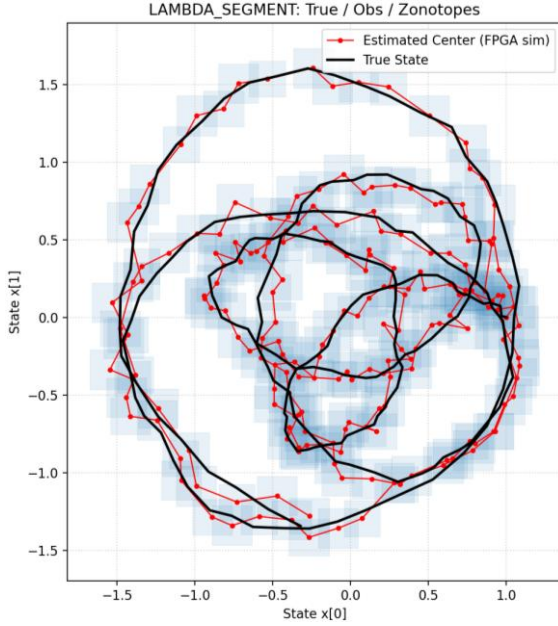


Fig. 2. True trajectory, estimated centre, and zonotopic enclosure for the Segment strategy.

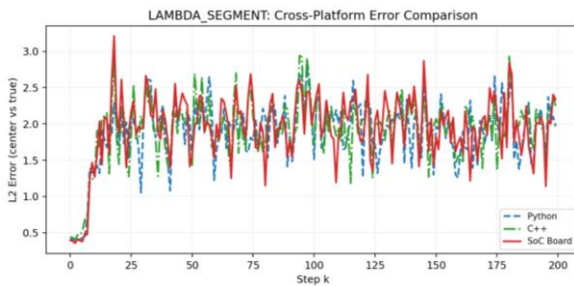


Fig. 3. Cross-platform centre-to-true-state error for the Segment strategy.

Cross-Platform Verification

All implementations process the same stored input bundle, including the system matrices, initial zonotope, measurement sequence, disturbance sequence, and reduction configuration. Verification is performed progressively from the Python reference to native C++, HLS C-simulation, and finally physical-board execution.

The comparison considers estimated centre vectors, interval radii, generator counts, reduction behaviour, and the absence of NaN or infinite values. Exact bitwise equality is not required because floating-point operation ordering and scheduling differ between the software and FPGA implementations. Instead, numerical differences are evaluated directly from estimator outputs, while trajectory and centre-error traces provide complementary behavioural checks.

Table 2 summarises the principal 110 MHz results. The Volume variant gives the lowest batch latency, 2.8709 ms ($14.355 \mu\text{s}/\text{step}$), corresponding to $15.15\times$ speedup over Python and $4.93\times$ over C++. Fixed-gain and Segment also provide clear acceleration over both software baselines. Although Volume requires more arithmetic in the correction-vector calculation, it is mapped more efficiently in the present HLS implementation, likely because its scalar-gain structure forms a more regular datapath and allows greater exploitation of DSP-based parallelism. Its lower latency should therefore be interpreted as an implementation-level result of the present architecture rather than as evidence that the Volume rule is intrinsically cheaper in algorithmic terms.

Table 2. Measured latency and speedup for the common 200-step workload at 110 MHz.

Method	Python (ms)	C++ (ms)	FPGA (ms)	Py./FPGA ($\times$)	C++/FPGA ($\times$)
Fixed-gain	37.216	12.157	4.8125	7.73	2.53
Segment	62.164	17.230	5.2371	11.87	3.29
Volume	43.482	14.163	2.8709	15.15	4.93

Table 3 shows that Fixed-gain requires the fewest LUTs and flip-flops, while Segment has the highest LUT and FF usage because of its full vector gain computation. Volume uses the largest number of DSP blocks, increasing from 220 to 280, but its more regular arithmetic structure is mapped efficiently by HLS. All three variants use 80 BRAMs because they share the same state dimensions, generator-storage limits, and batch-buffer organisation.

Table 3. Post-synthesis resource utilisation at the common 110 MHz target.

Method	LUT	FF	DSP	BRAM
Fixed-gain	77,829	70,647	220	80
Segment	92,454	86,977	220	80
Volume	83,735	77,215	280	80

As shown in Table 4, the Segment implementation has the highest total and dynamic power estimates, while Fixed-gain has the lowest total power. The estimated static component is approximately 0.305 W

for all three variants. Energy is calculated from the estimated total on-chip power and the measured FPGA batch latency. Consequently, Volume achieves the lowest estimated energy despite not having the lowest instantaneous power, requiring 9.96 mJ per 200-step batch, or 49.78 μ J per step. The Vivado power reports have Medium confidence because internal switching activity is only partially specified; therefore, the reported values are post-route implementation estimates rather than direct board-level power measurements.

Runtime frequency scaling was additionally used to evaluate the board-level operating-frequency margin. A frequency point was considered valid when the accelerator completed the full 200-step workload and returned finite centre and generator values without NaN, infinity, corrupted state, or an invalid generator count. Repeated board executions were also used to confirm that the accelerator completed normally at the tested operating point. In this paper, “verified” refers specifically to successful board-level functional execution under these criteria, rather than to formal post-route timing closure at every tested frequency.

Table 4. Post-route power and estimated energy at 110 MHz.

Method	Total (W)	Dynamic (W)	Energy/batch (mJ)	Energy/step (μ J)
Fixed-gain	3.370	3.066	16.22	81.09
Segment	3.600	3.294	18.85	94.27
Volume	3.468	3.163	9.96	49.78

As shown in Table 5, the highest board-validated PL clocks were 214.284 MHz, 166.665 MHz, and 187.498 MHz for Fixed-gain, Segment, and Volume, respectively. Incorrect execution was observed at the next tested operating points of 249.998 MHz, 187.498 MHz, and 214.284 MHz, respectively. The common 110 MHz results are retained for the primary cross-method comparison, while the scaling experiment reports the peak experimentally validated board-level performance.

Table 5. Peak board-validated operating points.

Method	Highest valid PL clock (MHz)	Best latency (ms)
Fixed-gain	214.284	2.2598
Segment	166.665	3.1545
Volume	187.498	1.5443

4. Discussion

The three correction strategies exhibit different hardware trade-offs. Fixed-gain has the simplest correction-vector computation and consequently requires the fewest LUTs and flip-flops. Segment computes a full geometry-dependent gain vector and therefore introduces additional arithmetic and data

dependencies, resulting in the largest LUT/FF utilisation and the lowest validated clock margin. Volume uses more DSP resources, but its scalar gain structure forms a regular datapath that is scheduled efficiently by HLS, yielding the lowest latency and estimated energy.

The results also highlight the importance of bounded generator management. Without reduction, each prediction appends process-noise generators and each sequential measurement correction appends an additional generator, causing the generator matrix to grow continuously. By enforcing a budget of $s = 32$, the implementation maintains fixed storage bounds and predictable loop limits, which are necessary for a static FPGA architecture.

The reported performance values should be interpreted as implementation-specific results for the considered 24-state benchmark and KR260 platform rather than universal performance bounds. In addition, the use of IEEE 754 single precision without directed outward rounding means that the theoretical enclosure guarantee of the exact-arithmetic estimator is not established at machine level in the current implementation.

A further extension is to consider richer set representations. Constrained zonotopes can represent intersections and additional linear constraints more compactly than standard zonotopes in some estimation problems [8]. Recent work has also developed set operations and order-reduction procedures specifically for constrained zonotopes [9]. Their FPGA implementation would introduce additional constraint management and linear-algebra kernels, but could provide tighter set representations for future embedded estimators.

5. Conclusions

The results demonstrate that zonotopic set-membership estimation can be mapped effectively to a heterogeneous SoC-FPGA architecture while keeping generator storage bounded and execution predictable. On the common 110 MHz implementation, all three variants outperform both software baselines, with the Volume strategy reaching 2.8709 ms per 200-step batch and the lowest estimated energy. Frequency scaling reduces its validated latency further to 1.5443 ms. These results support FPGA acceleration for embedded applications requiring deterministic, low-latency set-based estimation. Future work will investigate more parallel reduction mechanisms, adaptive correction rules, fixed- or mixed-precision arithmetic, and richer set representations such as constrained zonotopes [8, 9].

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Comparative Neural Forecasting of Automated Process Dynamics in Microelectronics

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Summary: This article presents a leakage safe neural forecasting framework for predictive analysis of automated microelectronics processes using temperature and pressure signals. The study applies causal feature engineering, chronological validation and sliding window modelling to compare persistence, GRU, Transformer and N-BEATS forecasting models. The used dataset contained 3957 observations from 29 tools and 11 tool families sampled every 32 seconds. A 30-sample input window and a 5-step prediction horizon were used. Results show that N-BEATS produced the lowest 5 step forecasting errors, reducing temperature MAE from 6.78 °C for persistence to 3.78 °C and pressure MAE from 0.212 to 0.129. The findings support neural forecasting as a practical layer for early process risk awareness.

Keywords: Forecasting, N-BEATS, GRU, Transformer, Temperature, Pressure, Semiconductor.

1. Introduction

Microelectronics manufacturing requires stable process conditions, rapid detection of abnormal behaviour and accurate anticipation of future sensor trajectories. Classical model predictive control (MPC) predicts future system behaviour over a finite horizon and applies the first element of an optimized control sequence, repeating the procedure at each sampling instant [9, 10]. While MPC is effective when the process model is reliable and its industrial value comes from explicit handling of constraints and multi-variable interactions, semiconductor production often involves nonlinear, time-varying and tool-dependent dynamics. Specifically, processes such as plasma etching, chemical vapour deposition, rapid thermal processing and chemical mechanical planarization are affected by nonlinear kinetics, equipment ageing, measurement delays, and inter-tool variability. These conditions motivate data driven and hybrid modelling approaches. Temperature and pressure are especially important because they are routinely available in many automated tools and can reveal both gradual drift and sudden instability. Neural networks have become important for industrial sequence modelling because they learn nonlinear mappings from historical sensor traces. LSTM networks were introduced to address long delay learning problems in recurrent systems [4], while GRU based encoder-decoder models simplified gated recurrence for sequence representation [2]. Temporal convolutional networks provide parallel and dilated sequence modelling [1] and Transformer uses self-attention to capture dependencies without recurrence [11]. For forecasting, N-BEATS offers a deep residual basis expansion structure designed specifically for time series prediction [8]. For example, N-BEATS has recently been extended to unsupervised anomaly

prediction in multivariate semiconductor time series using graph neural networks [12]. In semiconductor manufacturing, these methods relate closely to Virtual metrology and predictive monitoring, where sensor data are used to estimate hidden quality or risk states before direct metrology is available [5, 7]. Neural network has become important for industrial sequence modelling because they learn nonlinear mappings from historical sensor traces [3]. Therefore, the objective in this article is to evaluate whether these neural time series models can forecast short-term temperature and pressure dynamics more accurately than a simple persistence baseline while preserving causal, online compatible validation suitable for microelectronics automation.

2. Forecasting Framework

The experimental dataset consists of 3957 rows collected from 29 tools and 11 tool families. The primary raw variables are temperature (measured in °C) and pressure (measured in **mbar**), sampled at 32 second intervals. An input window of $L = 30$ samples is used and the forecast horizon $H = 5$ samples. The analysis follows a chronological split into training (70 %), validation (15 %) and test (15 %) subsets for each tool. Scalers are fitted only on training data and applied to validation and test data to prevent future leakage. Causal features were computed using only information available at or before the current time. The feature set includes raw temperature and pressure, first differences, rolling means, standard deviations, exponentially weighted moving averages and expanding z-scores.

$$\Delta x_t = x_t - x_{t-1}, \quad (1)$$

$$\mu_{t,w} = \frac{1}{w} \sum_{i=0}^{w-1} x_{t-i}, \quad (2)$$

$$\sigma_{t,w} = \sqrt{\frac{1}{w} \sum_{i=0}^{w-1} (x_{t-i} - \mu_{t,w})^2}, \quad (3)$$

$$EWMA_t = \alpha x_t + (1 - \alpha)EWMA_{t-1} \quad (4)$$

For each time step t , the model input is a sliding window of causal features:

$$X_t = [f_{t-L+1}, \dots, f_t], \quad L = 30 \quad (5)$$

The forecasting target is the future trajectory of temperature and pressure:

$$Y_t = [y_{t+1}, \dots, y_{t+H}], \quad H = 5 \quad (6)$$

The neural network maps the input window to the predicted future trajectory: $\hat{Y}_t = M_\theta(X_t)$, where M_θ is the neural network model with trainable parameter θ . Models were trained to minimize mean squared error:

$$\mathcal{L}(\theta) = \frac{1}{N} \sum_{i=1}^N \|\hat{Y}_i - Y_i\|^2 \quad (7)$$

2.1. Model Configuration and Training

The following model architectures were evaluated:

- GRU: 2 stacked recurrent layers with 128 hidden units per layer;
- Transformer: 3 encoder layers, 4 attention heads, 64 dimensions embedding and 128 feed-forward dimensions;
- N-BEATS: 3 blocks with 128 theta dimensions and 4 hidden layers per block.

All models were implemented using PyTorch 2.0.1 in python 3.9 and trained on NVIDIA RTX 3090 GPU. Adam optimizer [6] was used with a learning rate of 0.001 and a batch size of 32 for a maximum of 120 epochs with early stopping (patience = 15) based on validation loss.

Leakage safe validation was strictly enforced by:

- I. Fitting all data scalers exclusively on the training set and applying the same fitted parameters to validation and test sets;
- II. Ensuring the chronological split preserves time order so no future data is used to predict past data;
- III. Constructing sliding windows using only observations strictly preceding the forecast point.

The forecasting metrics used, are mean absolute error (MAE) and root mean squared error (RMSE) at each horizon step:

$$MAE_h = \frac{1}{N} \sum_{i=1}^N |\hat{y}_{i,h} - y_{i,h}|, \quad (8)$$

$$RMSE_h = \sqrt{\frac{1}{N} \sum_{i=1}^N (\hat{y}_{i,h} - y_{i,h})^2}, \quad (9)$$

3. Results

Fig. 1 shows the standardized 20 sample rolling means of temperature and pressure for the ANNEAL_01 tool, allowing both variables to be compared on a common axis. The signals exhibit gradual shifts and localized perturbations typical of thermal processing steps.

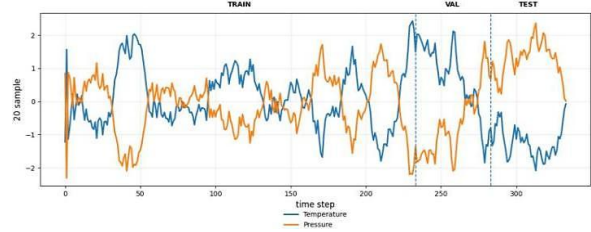


Fig. 1. Temperature and pressure dynamics for ANNEAL_01 (standardized 20 sample rolling means).

Table 1 presents the forecasting errors for both temperature and pressure on the ANNEAL_01 test segment. N-BEATS achieved the lowest error, outperforming all the other models on both metrics. At horizon 5, it reduced temperature MAE by approximately 44.2 %, dropping from 6.78 °C (persistence) to 3.78 °C. It also reduced pressure MAE by approximately 39.2 %, from 0.212 to 0.129. Transformer and GRU models improved on persistence but remained slightly weaker than N-BEATS in this experiment. Persistence baseline performed competitively at the first horizon because temperature and pressure often change gradually, but its error increased sharply at longer horizons. Fig. 2 presents temperature forecasting error comparison across all models, while Fig. 3 shows the corresponding pressure error comparison.

The results demonstrate that neural forecasting improves short horizon process prediction when validation is performed chronologically and feature engineering is causal. The gradual increase in forecast error over the horizon is expected, as uncertainty grows further from actual observations. Pressure errors showed stronger relative variability than temperature errors, suggesting that pressure dynamics may contain faster disturbances, sensor noise or regime changes not fully captured by the current deterministic point forecasting setup. Therefore, the ability to forecast temperature and pressure trajectories provides useful early information for operator warnings, intensified monitoring, recipe verification or preventive maintenance planning.

4. Conclusions

This study demonstrates that leakage safe neural forecasting can significantly improve the prediction of temperature and pressure dynamics in automated

microelectronics processes. Using 30 historical samples and a 5 step horizon, N-BEATS achieved the strongest forecasting performance among the evaluated models (GRU, Transformer and persistence) on ANNEAL_01 test segment. The method is suitable for supervisory predictive control support, especially

where direct actuator records are absent but sensor streams are readily available. Future work should extend the experiment to probabilistic forecasting and uncertainty-aware alarm systems and validate the findings across multiple tools to further enhance decision making in semiconductor fabrication.

Table 1. Forecasting errors for temperature (°C) and pressure (mbar) on ANNEAL_01 test segment.

Model	Temp MAE h1	Temp MAE h5	Temp RMSE h1	Temp RMSE h5	Press MAE h1	Press MAE h5	Press RMSE h1	Press RMSE h5
Persistence	2.34	6.78	4.68	8.45	0.087	0.212	0.112	0.278
GRU	1.87	4.23	2.56	5.67	0.065	0.143	0.089	0.192
Transformer	1.79	4.01	2.48	5.34	0.061	0.138	0.085	0.185
N-BEATS	1.65	3.78	2.31	5.02	0.057	0.129	0.079	0.174

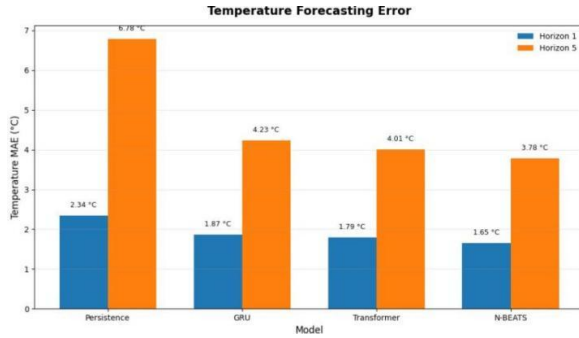


Fig. 2. Temperature forecasting error comparison across all models.

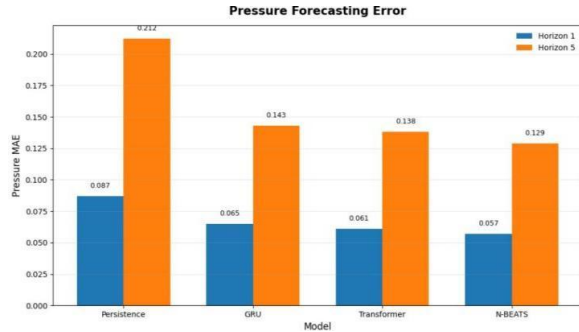


Fig. 3. Pressure forecasting error comparison across all models.

Acknowledgements

We would like to thank the research teams at MIET for their support in data collection and processing infrastructure.

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Application of Non-equilibrium Green's Functions (NEGF) to Study Optical Properties of Semiconductor Lasers based on Quantum Wells

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Summary: The non-equilibrium Green's function (NEGF) formalism has become an important theoretical framework for describing quantum transport and light-matter interactions in nanoscale optoelectronic devices. Unlike semiclassical drift-diffusion approaches, NEGF can treat quantum confinement, tunneling, carrier-phonon and carrier-photon interactions, and nonequilibrium carrier distributions within a unified framework. Recent applications have extended NEGF from conventional quantum-well photovoltaics and light-emitting diodes (LEDs) toward two-dimensional materials, photodetectors, nanophotonic structures, and atomically thin devices.

Here, we describe a procedure for evaluating material gain of quantum well-semiconductor laser structures based on NEGF formalism. Our approach does not require phenomenological parameters. It is based on a self-consistent solution of the Dyson equation with the 1D Poisson equation. Our formalism allows us to determine spectra of local (in position) gain. We report on the determined spatial distribution of material gain. We show that it is highly nonuniform.

Keywords: Nonequilibrium Green's function formalism, Optoelectronics, Semiconductor lasers, Quantum wells.

1. Introduction

The rapid development of nanoscale optoelectronic devices has created a need for theoretical methods capable of describing quantum transport together with optical processes. The nonequilibrium Green's function formalism provides such a framework. Originally developed for nonequilibrium many-body systems, NEGF is now widely used to calculate quantum transport in semiconductor nanostructures and devices. Its central advantage is that it can describe open systems connected to contacts while incorporating scattering and interactions through appropriate self-energies [1], [2], [3],[4],[5].

In optoelectronics, this capability is particularly valuable because charge transport and optical processes are strongly coupled. Photovoltaic devices, for example, involve photon absorption, generation of nonequilibrium carriers, scattering, recombination, and extraction. Similarly, LEDs require a consistent description of carrier injection, transport, nonradiative processes, and photon emission. NEGF provides a microscopic description of these processes through the retarded, advanced, lesser, and greater Green's functions, together with self-energies describing contacts, phonons, photons, impurities, and other interactions.

Modelling of semiconductor optoelectronic devices plays an increasingly important role. It allows for the shortening of time for getting products to the market. In practical modelling, simplified models based on various approximations are often used. This is due to the fact that they run very fast and therefore the complete engineering characteristics can be quickly created. However, they require many

parameters which limit their abilities to accurately describe new devices. Microscopic models, on the other hand, with a reduced number of phenomenological parameters offer better predictive power but require long running times.

Optical gain of QW structure is an important quantity of practical devices; see the book by Coldren-Corzine [6] for a comprehensive summary. There are many approaches published devoted to its evaluation using methods of various complexities. The comparison of the microscopic and standard (phenomenological) approaches has been reported by Hader [7]. They demonstrated shortcomings of some approximations used to calculate material gain and other parameters. They showed that replacing electron-electron and electron-phonon scattering processes by a phenomenological dephasing time leads to significant errors.

2. Formalism

Our microscopic approach is computationally very demanding. We therefore restricted ourselves to a two-band model where we considered only conduction electrons and one type of holes. Dimensions transverse to the growth direction (z) are assumed to be infinite with periodic boundary conditions.

We are interested in a steady-state approximation which replaces all double time functions $f(t_1, t_2)$ by $f(t_1 - t_2)$, which allows us to perform a temporal Fourier transform. To remove transverse coordinates from the equation, we expand Green's functions in a k_p basis and then in a nonorthogonal first-order finite element basis.

Green's function can be viewed as a substitute for a wave function. It allows for the inclusion of many-body interactions using perturbation techniques.

Green's functions are defined as

$$G^>(1,2) = \mp \frac{i}{\hbar} \langle \hat{\psi}_{\bar{H}}(1) \hat{\psi}_{\bar{H}}^\dagger(2) \rangle \quad (1)$$

$$G^<(1,2) = \frac{i}{\hbar} \langle \hat{\psi}_{\bar{H}}^\dagger(2) \hat{\psi}_{\bar{H}}(1) \rangle, \quad (2)$$

where $\hat{\psi}_{\bar{H}}^\dagger$ and $\hat{\psi}_{\bar{H}}$ are creation and annihilation operators in the Heisenberg picture. Here, index i refers to space and time coordinates as $i = (\mathbf{r}_i, t_i)$.

In the practical calculations the advanced $G^A(1,2)$ and retarded $G^R(1,2)$ functions are preferred. They are introduced as

$$G^R(1,2) = G^t(1,2) - G^<(1,2) \quad (3)$$

and

$$G^A(1,2) = G^<(1,2) - G^{\bar{t}}(1,2) \quad (4)$$

Central point of this method is the Dyson equation

$$\left(i\hbar \frac{\partial}{\partial t_1} - H(\mathbf{r}_1) \right) G^R(1,2) = \delta(1-2) + \int d3 \Sigma^R(1,3) G^R(2,3) \quad (5)$$

and

$$G^<(1,2) = \int d3 \int d4 G^R(1,3) \Sigma^<(3,4) [G^R(4,2)]^\dagger \quad (6)$$

All many-body interactions are expressed in self-energies $\Sigma^<$ and Σ^R , which are, in general, functions of G^R and $G^<$. Self-energies are given by infinite series which are usually truncated after the first term. One can determine carrier and current densities as

$$n(1) = -i\hbar G^<(1,1^+) \quad (7)$$

and

$$j(1) = \frac{\hbar^2}{2m} [\nabla_{\mathbf{r}} - \nabla_{\mathbf{r}'}] G^<(1,1^+) \quad (8)$$

Next we perform spatial Fourier transform with respect to transverse wave vector. The central equation in our considerations is discretized Dyson equation in nonorthogonal basis [8, 9].

$$G^R(\mathbf{k}, E) = (E\mathbf{S} - \mathbf{H}(\mathbf{k}) - \Sigma^R(\mathbf{k}, E))^{-1} \quad (9)$$

$$\mathbf{G}^\geq(\mathbf{k}, E) = G^R(\mathbf{k}, E) \Sigma(\mathbf{k}, E) \mathbf{G}^A(\mathbf{k}, E) \quad (10)$$

Here

$$S_{ai,bj} = \delta_{ab} \int dz w_i(z) w_j(z), \quad (11)$$

where $w_i(z)$ are the basis functions used to expand slowly varying functions (changing on the large scale).

All matrices are numbered with band number and spatial position in z direction, $\mathbf{S}$ matrix is an overlap matrix for our nonorthogonal basis, which in case of orthogonal basis becomes identity matrix, and $\mathbf{H}$ is a k p Hamiltonian discretized with finite element basis.

Dyson equation is supplemented with 1D Poisson equation which are then solved self-consistently

$$\frac{\partial}{\partial z} \varepsilon(z) \frac{\partial}{\partial z} \phi(z) = e(n(z) - p(z) + N_D(z) - N_A(z)) \quad (12)$$

Using Green's functions we calculate so-called greater and lesser transverse polarization function using formula

$$P^\geq(x_i, \hbar\omega) = -\frac{i\mu_0 e^2}{m_0^2} \int \frac{dk}{2\pi} k \int \frac{dE}{2\pi} \times \sum_{c,c'} \sum_{v,v'} G_{ic,ic'}^\geq(k, E + \hbar\omega) G_{iv,iv'}^\leq(k, E) p_{cv'} p_{c'v}^* \quad (13)$$

In above equation $p_{c'v}^*$ is momentum matrix element between two zone-centre Bloch functions.

Using lesser and greater transverse polarization functions one can calculate electric susceptibility and then material gain can be calculated in a standard way as imaginary part of susceptibility. Since we evaluate quantities which are nonuniform, our final equation for material gain is defined per distance and it takes the form

$$g(x_i, \hbar\omega) = \frac{c}{2i\omega\sqrt{\epsilon_\infty}} (P^>(x_i, \hbar\omega) - P^<(x_i, \hbar\omega)) \quad (14)$$

3. Results

We considered a single GaAs quantum well embodied in $\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$ p-i-n junction with the details specified in Table 1.

Table 1. Heterostructure used in the calculations.

Thickness	Material	Doping [m ⁻³]	Description
infinite	$\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$	p-10 ²⁵	Left lead
15 nm	$\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$	p-10 ²⁵	Device
7.2 nm	$\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$	-	Device
8 nm	GaAs	-	Device
7.2 nm	$\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$	-	Device
15 nm	$\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$	n-10 ²⁵	Device
infinite	$\text{Al}_{0.2}\text{Ga}_{0.8}\text{As}$	n-10 ²⁵	Right lead

Contrary to most popular gain calculation methods [10] which allow only to calculate gain averaged over quantum well, with this formalism one can calculate gain at any point in the system (both in QW and outside).

Using the above formalism, in Fig.1 we showed material gain per cm as a function of position in the z direction over quantum well region and outside for applied bias $V=1.5$ V.

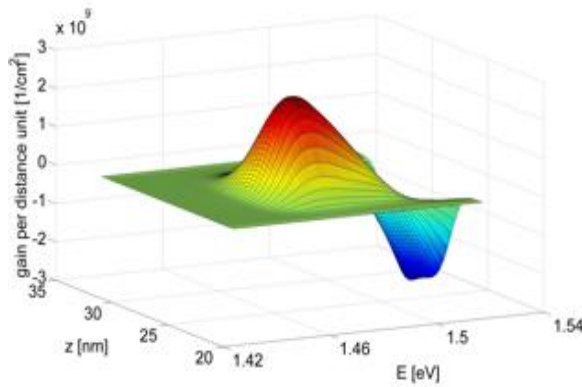


Fig. 1. TE material gain spectra for $V=1.5$.

4. Conclusions

We described a procedure for evaluating material gain of quantum well-semiconductor laser structures based on NEGF formalism. Our approach does not require phenomenological parameters. It is based on a self-consistent solution of the Dyson equation with the 1D Poisson equation. Our formalism allows us to determine spectra of local (in position) gain. We report on the determined spatial distribution of material gain. We show that it is highly nonuniform.

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